International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-3 Issue-6, August 2014

Embedded Spiking Neural Network

Roshni Kishan, Siri A, Meghana G. R, Meghana S

Abstract*— NEURAL networks are computational models of the brain. These networks are excellent at solving problems for which a solution seems easy to obtain for the brain, but requires a lot of efforts using standard algorithmic techniques. Examples of such problems are pattern recognition, perception, generalization and non-linear control. In the brain, all communication between neurons occur using action potentials or spikes. In classical neural models these individual spikes are averaged out in time and all interaction is identified by the mean firing rate of the neurons. Recently there has been an increasing interest in more complex models, which take the individual spikes into account. This sudden interest is catalyzed by the fact that these more realistic models are very well suited for hardware implementations, more specifically embedded systems. In addition they are computationally stronger than classic neural networks.

Index Terms*—embedded systems, neural network, neurons, spikes.

I. INTRODUCTION

Spiking neural networks (SNNs) fall into the third generation of neural network models, increasing the level of realism in a neural simulation. In addition to neuronal and synaptic state. SNNs also incorporate the concept of time into their operating model. The idea is that neurons in the SNN do not fire at each propagation cycle, but rather fire only when a membrane potential – an intrinsic quality of the neuron related to its membrane electrical charge – reaches a specific value. When a neuron fires, it generates a signal which travels to other neurons which in turn, increase or decrease their potentials in accordance with this signal. Spiking neural networks are better suited for hardware implementations due to two facts: inter-neuron communication consists of single bits and the neurons themselves are actually only weighed leaky integrators. Because only single bits of information need to be transmitted, a single wire is sufficient for connection between two neurons. Thereby the routing of neural interconnection on a 2D chip is implied. In this paper, we will explain the implementation of spiking neural networks on a re-configurable hardware. More specifically it will concentrate on embedded devices because they have the advantage that a processor is closely linked to the neural model, which can coordinate learning, reconfiguration, etc. This paper is organized as follows, Section 2 explains the concept of Spiking Neural networks .

Manuscript published on 30 August 2014.
* Correspondence Author (s)
Roshni Kishan, Department of Telecommunication Engineering, BMSCE, Bangalore, India.
Siri A, Department of Telecommunication Engineering, BMSCE, Bangalore, India.
Meghana G. R, Department of Telecommunication Engineering, BMSCE, Bangalore, India.
Meghana S, Department of Telecommunication Engineering, BMSCE, Bangalore, India.

Section 3 explains about the implementation of neural network model on a embedded platform. Section 4 explains about the applications of embedded spiking neural network. Finally some conclusions are given in section 4.

II. SPIKING NEURAL NETWORK

In machine learning and related fields, artificial neural networks (ANNs) are computational models inspired by an animal's central nervous systems(in particular the brain) which is capable of machine learning as well as pattern recognition. Artificial neural networks are generally presented as systems of interconnected "neurons" which can compute values from inputs. An artificial neuron is a mathematical function conceived as a model of biological neurons. The artificial neuron receives one or more inputs (representing dendrites) and sums them to produce an output (representing a neuron's axon). Usually the sums of each node are weighted, and the sum is passed through a non-linear function known as an activation function or transfer function. The transfer functions usually have a sigmoid shape.

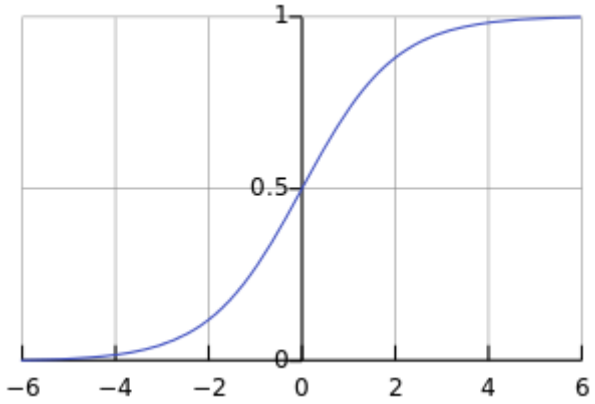

Fig. 1 Sigmoid Shaped Transfer Function

Spiking Neural Networks (SNNs), or Pulse Coded Neural Networks (PCNNs), differ from many other neural networks in that inter-neural communication is reduced to temporally separated spikes or pulses. Spiking neural networks offer various advantages over traditional sigmoidal artificial neural networks. They are not only biologically plausible but they can potentially reproduce the computational dynamics observed in a biological brain. SNNs are designed to be phenomenological models of biological neurons; reflecting natural action-potential generation, post-synaptic potential shaping, and refractory periods. In the case of ANNs information processing happens in a much simpler manner: an iterative series of calculations based on neuron outputs and layers. In an SNN, neurons emit pulses or spikes through their synapses whenever their membrane potential reaches its threshold value.

Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)

This happens due to incoming spikes from other presynaptic neurons. Each spike has an amplitude of 100 mV and lasts approximately 1-2 ms. Since all the spikes in the network have the exact same form, information is encoded in the chronological order of the spikes, or the so-called spike train. Spiking neural network model usually uses 'Integrate an fire model' where the neurons are nothing but a leaky integrator, which fire an reset a neuron when a threshold is reached.

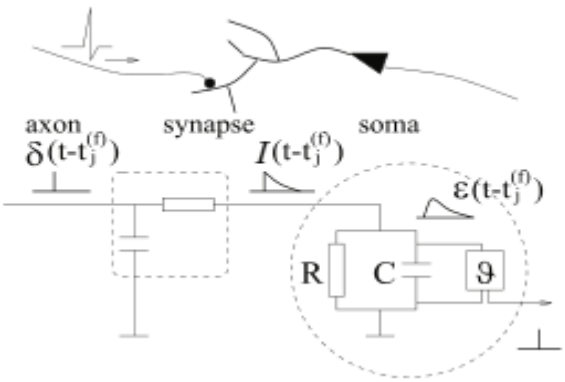

Fig. 2 An Integrate an Fire Neuron

A leaky integrator equation is a specific differential equation, used to describe a component or system that takes the integral of an input, but gradually leaks a small amount of input over time as shown in the diagram below.

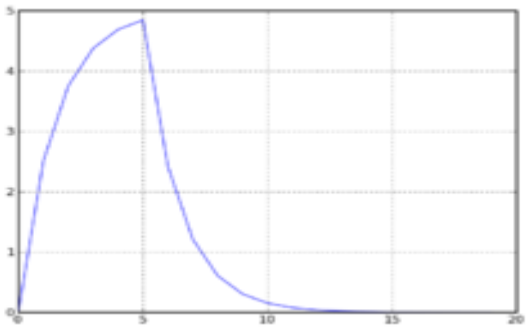

Fig. 3 Input-Output Graph of a Leaky Integrator

Integrate and fire model is one of the earliest models of a neuron which was first investigated in 1907 by Louis Lapicque. A neuron is represented in time by

$$I(t) = C_{\mathrm{m}} \frac{dV_{\mathrm{m}}}{dt} \qquad (1)$$

which is just the time derivative of the law of capacitance, Q = CV. When an input current is applied, the membrane voltage increases with time until it reaches a constant threshold Vth, at which point a delta function spike occurs and the voltage is reset to its resting potential, after which the model continues to run.

III. IMPLEMENTATION OF SPIKING NEURAL NETWORKS ON EMBEDDED SYSTEMS

Now we will focus on the embedded side of the story. A current trend is to equip lots of devices with extra logic to make them interact more intelligently with their environment (ambient intelligence). This intelligence is provided by an embedded system. Such an embedded system normally consists of a general purpose processor, some memory, interface hardware and some custom hardware executing very time critical tasks. Recently the hardwired custom hardware gets replaced by a reconfigurable hardware component.

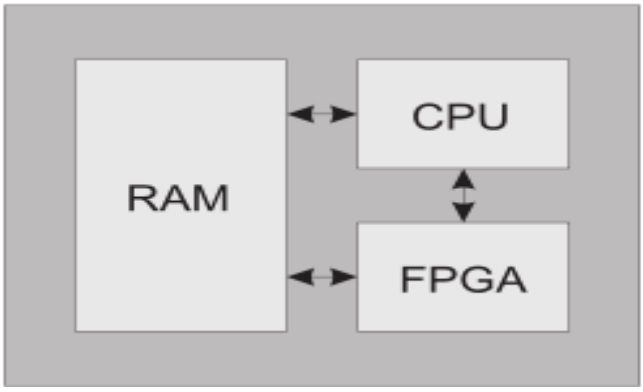

Fig. 4 An Embedded Architecture with FPGA Closely Linked to the Memory and the CPU

This way the function of that component can be redefined after design and manufacturing. To this date only very limited learning algorithms for spiking neural networks are available. This is mainly because this field of neural network research is pretty young. Through the use of runtime re configurable hardware it is possible to split large networks into smaller sub modules, which can be implemented separately in hardware. Folding them out in time can thus run very large networks. This splitting of neural networks is actually a space versus time consideration. Due to the fact that a processor is coupled with the neural hardware, it is possible to implement the additional learning phases on this processor. This way training can be done on a model in memory, and afterwards this model is translated to the actual hardware implementation. Implementing a neural network system on a hardware system is done by the following process. The neuron models is implemented in digital hardware. Speed and area requirements of the neuron model is evaluated. FPGA is used to speed up simulation and evaluation significantly. Several different approaches are possible for the interconnection of different neurons like hardwired interconnections, reconfigurable hardware connections, message passing on a bus-structure, etc. Research on how it is possible to implement a group of topologies as large as possible on the re configurable hardware without asking much resources or introducing a big delay is made. In the last step the neuron model and interconnection strategy are combined to form a neural hardware module. Research on reconfiguration bandwidth, memory architecture, pipelining, on-chip learning and space/time-considerations is needed. There will also be special care in making the neural module as reusable as possible and therefore testability and the use of standard system-on-a-chip busses will be considered .As a result we will have a hardware neural network, implemental in digital re configurable hardware and suitable for embedded applications. It will be space/time-scalable, so that it can be easily adapted to the user requirements.

Published By:
Blue Eyes Intelligence Engineering
and Sciences Publication (BEIESP)

IV. APPLICATIONS

All areas where embedded devices are used in complex changing environments, the neural network approach could amount for the adaptive and intelligent behavior. Due to the fact that the neural network is implemented in reconfigurable hardware it is possible to load the network only when it is needed. It is now possible to solve complex problems in a hybrid way: partially by a neural network and partially by classic algorithmic techniques. Both techniques can thus be used on the sub problems where they are best. Neural networks can for example be used to do pure pattern recognition on data, which is already pre processed using classic techniques (for example Fourier transformation). The results of the neural network can then be fed to the processor, which can perform further computations. A classic problem where we are faced with a complex, changing environment is biometrics. This term identifies all techniques used to measure human or animal features, for example voice, handwriting or iris recognition. All these human properties evolve during their lives and are very noisy. Hybrid techniques use neural networks to do low level pattern recognition (detecting single syllables) while algorithmic techniques are used in the higher levels (forming words and sentences with the syllables using dictionaries and statistical techniques). Another application is adaptive non-linear control. Most, if not all, machines are subject to significant wear and tear. Complex non-linear machines are locally linearized(in a working point) to enable control with standard techniques (like PID). Due to wear, the working point of the machine tends to shift so that an incorrect linear approximation is used and decent control gets impossible. Neural networks have proven to be very good at controlling highly non-linear systems. Because these neural networks can be trained during operation, they can be adapted to changing situations like wear. Because this neural model can be implemented on an embedded device it is possible to place the control hardware very close to the detectors and actuators. This way delay is minimized, which normally is a big nuisance.

V. CONCLUSION

When it comes to perception at a deeper level the human brain outwits the computer. Human brain is adept at understanding things like perception, pattern recognition, generalization and non-linear control. The computer scientists want to tap this extraordinary potential of human brain and expedite alongside enhancing the quality of some computational procedures. Neural networks tap the concept of functioning of human brain. Spiking Neural Networks and the concepts of embedding is a relatively young one. A rigorous research is going on and still much has to be done in the field. Spiking Neural Networks comes up with a promise of transforming the work environment with efficient and intelligently interactive communicating systems.

REFERENCES

[1] C. M. Bishop. Neural Networks for Pattern Recognition. Claren- don Press, Oxford, 1995.
[2] W. Maass and C. M. Bishop. Pulsed Neural Networks. Bradford Books/MIT Press, Cambridge, MA, 2001.
[3] W. Gerstner and W. Kistler. Neurons, Populations, Plasticity. Cambridge University Press, Cambridge, 2002.
[4] J-Y. Mignolet, S. Vernalde, D. Verkest, and R. Lauwereins. En- abling Hardware-Software Multitasking on a Reconfigurable Com- puting Platform for Networked Portable Multimedia Appliances. In Proceedings. The 2002 International Conference on Engineer- ing of Reconfigurable Systems and Algorithms. June 2002.
[5] H. Chang, L. Cooke, M. Hunt, G. Martin, A. McNelly, and L. Todd. Surviving the SOC Revolution. Kluwer Academic Pub- lishers, Dordrecht, 1999.
[6] B. Gold and N. Morgan. Speech and Audio Signal Processing: Processing and Perception of Speech and Music. John Wiley and Sons, New York, NY, 2000.
[7] M. S. Ahmed. Neural net based MRAC for a class of nonlinear plants. Neural Networks, 13:111–124, 2000. Spiking Neuron Models: Single
[8] Biologically Sound Neural Networks for Embedded Systems Using OpenCL By István Fehérvári, Anita Sobe and Wilfried Elmenreich1.
[9] Design and FPGA implementation of an embedded real-time biologyically plausible spiking neural network processor by M.J.Pearson , C.Melhuish, A.G.Pipe, M.Nibouche, I.Gilhesphy, K.Gurney, B.Mitchinson
[10] Embedded spiking neural networks By Benjamin Schrauwen,Korea University, Sŏul, Seoul, South Korea [4] Embedded spiking neural networks By Chandra Mohanty

Roshni Kishan, studying Bachelor of Engineering in Telecommunication engineering in BMS College of Engineering .Current CGPA is 8.75.Interested in pursuing higher studies in the field of Electronics and later do research and contribute to technology greatly. Areas of interest are Embedded systems ,VLSI and digital communication..

Siri A, studying Bachelor of Engineering in Telecommunication engineering in BMS College of Engineering .Current CGPA is 9.00.Interested in pursuing higher studies in the field of Electronics and later do research and contribute to technology greatly. Areas of interest are Embedded systems ,VLSI and digital communication..

Meghana G R, studying Bachelor of Engineering in Telecommunication engineering in BMS College of Engineering .Current CGPA is 8.55.Interested in pursuing higher studies in the field of Electronics and later do research and contribute to technology greatly. Areas of interest are Embedded systems ,VLSI and digital communication..

Meghana S, studying Bachelor of Engineering in Telecommunication engineering in BMS College of Engineering .Current CGPA is 9.216.Interested in pursuing higher studies in the field of Electronics and later do research and contribute to technology greatly. Areas of interest are Embedded systems ,VLSI and digital communication..