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A 9-Bit, 200MS/s Low Power CMOS Pipeline ADC

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Abstract*— *This paper describes 9-bit, 200MS/s Pipeline analog to digital converter implemented in 0.18µm CMOS process consuming 48.97mW power from 1.8v supply. To improve the linearity of pipeline ADC is designed which has three stages, 3-bit/stage architecture. Operational transcconductance amplifier is adopted in all pipeline stage to give good power efficiency. The converter is optimized for low voltage, low power application by optimizing opamp and 3- bit flash at circuit level.

Index Terms*— *Operational Transconductance Amplifier (OTA), Thermometric Codes, Flash ADC, Pipeline ADC.

I. INTRODUCTION

Analog-to-digital converters (ADCs) are very important building blocks in signal processing and communication systems. Applications like wireless communications and digital audio and video communication have created the need for higher speed and resolution, cost-effective data converters. The evolution in digital signal processors possesses great challenge for analog designers to continuously improve and develop new ADC and DAC architectures. Many good ADC architectures viz. flash ADC, two-step ADC, pipeline ADC, successive approximation register (SAR) ADC, delta-sigma ADC, integrating ADC etc have been invented to satisfy different requirements in different applications. Generally Analog to Digital Converters (ADC) is classified in two: high speed and high resolution. Converters with a speed (or sampling rate) greater than 10MHz are considered high speed ADCs. They are used in applications such as imaging, ultrasound, digital cameras, communications, baseband digitization, etc. One of the issues of the high speed ADCs is their moderate resolution, in other words low dynamic range. In applications such as ultrasound, high speed and high resolution ADCs are needed. Among various ADC architectures, the pipelined ADC has the attractive feature of maintaining high accuracy at high conversion rate with low complexity and power consumption. Successive Approximation Register based ADC still holds that section of applications which requires lower sampling rates and applications requiring sampling rates (a few hundred MS/s or higher) are still obtained using flash ADCs. The Pipelined ADC has become the most popular ADC architecture for sampling rates from a few mega-samples per second (MS/s) up to 100+MS/s. Nonetheless, pipelined ADCs of various forms have improved greatly in speed, resolution, dynamic performance, and low power consumption in recent years.

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Gigabit Ethernet and code conversion for flat panel displays [6] are few applications that require sampling rate of about 100MS/s or above. For such application it is very crucial to reduce power consumption along with maintaining high speed of operation [1]. A survey on present A/D converter research reveals that a majority of effort has been directed to four different types of architectures [2-3]:

A) Flash-type / Parallel ADC,
B) Successive approximation ADC
C) Oversampled / Sigma-Delta ADC and
D) Pipeline ADCs

Each has its own benefits and spans the spectrum of high speed and resolution. Flash ADCs are the fastest of all but uses series of comparators (OPAMP). An n-bit flash ADC uses 2^n comparators and hence as no of bits increases, hardware needed for flash ADC increases and hence becomes difficult to use flash ADCs for higher no of bits. On the other end, Sigma-Delta ADCs uses oversampling technique to achieve higher resolution but are relatively slower because of the same reason of oversampling the input signal.SAR based ADCs are best suited for higher resolution applications but has tradeoff with accuracy of the data produced by it. A Pipeline ADC combines the advantages of all above mentioned ADCs to produce a higher resolution output with good conversion speed and accuracy. Divide and Rule is the concept behind Pipeline ADC architecture. Pipeline ADCs as shown in Figure-1 are the architecture of choice for ADCs used in wireless communication systems, and are ideally suited for realizing 8–16 bits of resolution, 70–80 dB of SNR, at 100–300 MS/s, while dissipating less than 1W of power [4]. Additionally, to reach a higher operation frequency, OPAMPs need high gain–bandwidth product, reflecting an increase on power consumption. Different alternative solutions for building sub-blocks of pipeline ADC have been proposed, namely, open-loop amplification, comparator based, zero-crossing based and dynamic source follower (SF) based [5-8].

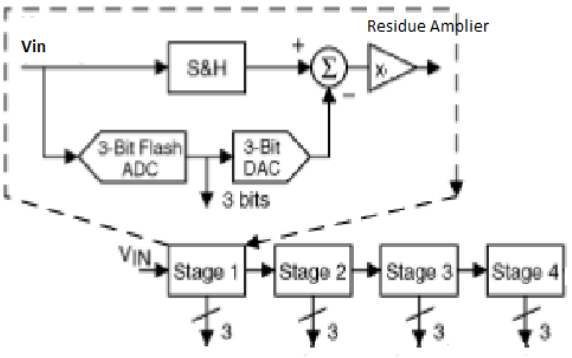

Figure 1. Conceptual Block Diagram of 4-Stage Pipeline

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However, their energy and area efficiency values are function of their optimum resolution per stage. High Performance monolithic pipelined ADCs are still built in Bi-CMOS or bipolar processes, the mainstream of pipelined ADC design has already shifted to CMOS process for lower cost and power [9]. Each stage operates on the residue passed down from the previous stage, thereby allowing for fast conversions. While the residue of the first stage is being operated on by the second stage, the first stage is free to operate on the next samples. Each stage of a pipeline is divided into two main parts. The first is the gain-stage. The gain-stage contains the operational trans-conductance amplifier (OTA) and the sample and hold (S/H) block. The second part is the combination of a sub-ADC and the sub-DAC. Both sub-ADC and sub-DAC are low-resolution A/D and D/A converters respectively. An analog signal input to a stage is given onto the S/H circuitry at the front end. The analog signal is sent to the sub-ADC and gain-stage simultaneously. The sample is then converted into a low-resolution digital word by the sub- ADC. The sub-DAC then converts this digital word into an analog signal. This analog signal is subtracted from the initial sample creating a residue. This residue is sent to the following stage and the process is repeated. Each stage provides a 3 bit digital word Section 1 is about designing OTA and Sample and Hold Circuit, while section 2 includes design of 3 Bit Flash ADC, which forms one single stage of pipeline ADC and 9-bit pipeline ADC. Section 3 consists of final simulation results and conclusion of 9-bit pipeline ADC.

II. DESIGN OF OTA AND SAMPLE AND HOLD CIRCUIT

OTA are basically of 4 types [6], viz., Telescopic OPAMP, Folded-cascode OPAMP, Gain-Boosted OPAMP and Two-Stage OPAMP. Each of above mentioned OPAMP architecture has its own set of advantages and disadvantages. Both telescopic and Folded Cascode designs employ cascaded transistors to boost the OPAMP gain, they have many differences. The telescopic OPAMP has the advantages of higher speed and lower power consumption and folded cascade OPAMP has large output signal swing and large input common mode range. Here two stage op-amp is choosen since it provides higher gain, highest output swing and is less prone to noise as compared to other OPAMP architectures. Figure 2 explains the basic circuit for employed in two stage OPAMP.The first stage is a Differential amplifier which is responsible for high gain and this stage is follwed by a source follower amplifier which provides better output swing. The design of MOS W/L ratios and compensation network was adopted from [3].

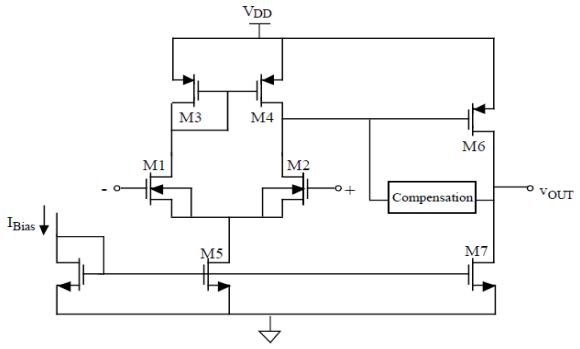

Figure 2. Operational Transconductance Amplifier

Design steps for OTA were adopted; Care should to be taken while designing so that all transistors operate in saturation region. The aspect ratio for each transistors obtained from hand calculation needs to be iterativly adjusted so as to meet desired specification. Below table lists the aspect ratio for each MOS transistor.

TABLE 1 Aspect Ratio of MOS in OTA

Transistor	Aspect Ratio (W/L)	Width(W),L=500nm
M1,M2	200	100 µ m
M3,M4	26	13 µ m
M5,M8	6	3 µ m
M6	1150	575 µ m
M7	115	57.5 µ m

Once the OTA is ready, a sample and hold circuit can be designed with the help of an hold capacitor and a switch which operates at sampling frequency. Transmission gate(TG) is used as a switch and a hold capacitor value is 10pF value. The idea behind using transmission gate (TG) as switch is to get maximum sampling frequency. Generally, upper limit on sampling frequency is depended on the type of switch used, and with TG as switch we can get to around 100-200Mhz of sampling frequency without affecting the output much.

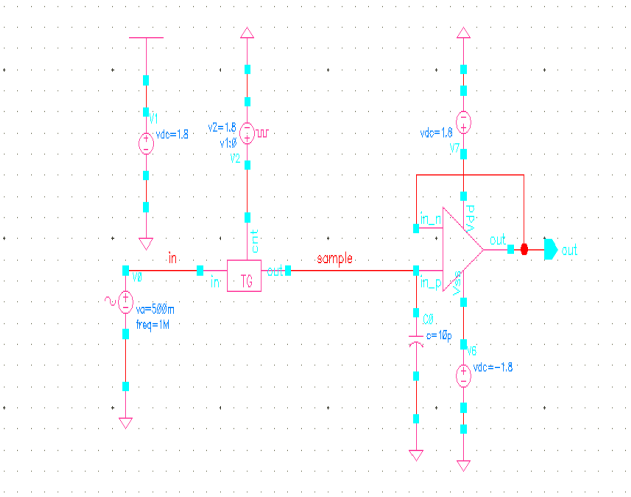

Figure 3. Sample and Hold Circuit

According to Nyquist Sampling Theorem, sampling frequency must be equal to or greater then twice the input signal frequency for perfect sampling to achieve. Oversampling can also be done to achieve higher sampling frequency. Capacitor charges and follows the input signal when switch is closed and it holds on this value when switch is open. Designed OTA is used as a voltage follower, which follows the capacitor voltage value stored on it during hold stage. OTAC was designed keeping in mind following set of specification.

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TABLE 2 OTA Specification

Gain at DC (Av(0))	>70dB
Gain-Bandwidth Product (GBP)	>100MHz
Slew Rate (SR)	>5V/µsec
Load capacitance	<2pF
Output voltage swing	-1.4 V to +1.5V
Input common mode voltage (Vin(min))	-1V
Input common mode voltage (Vin(max))	1.6V
Vdd power supply	1.8V
Vss power supply	-1.8V

III. SUB 3-BIT FLASH ADC AND 9-BIT PIPELINE ADC

Sub ADCs used in pipeline ADC does not require to be of high resolution. The choosen flash type ADC work as sub ADC because it is fast and hence inter-stage delay can be reduced which internn reduces the delay to generate final digital output. Flash type ADC uses a series of comparators whose output is either high(logic high (V_{DD})) or logic low(ground) depending upon the relation between input signal and the reference voltage at a given point of time. If Vref is smaller then Vin then logic high value is outputed by comparator else a logic low vaule is obtained.

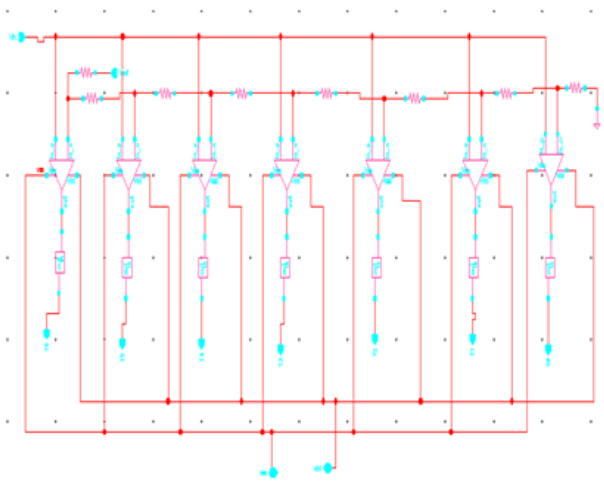

Figure 4. 3-Bit Flash Adc Schematic

Designed OTA is used as comparator with input analog signal given to non inverting terminal of each OTA while a reference voltage is given to inverting terminal of each OTA. Reference voltage given to each OTA is derived from a string of resistor which acts as a voltage divider.For n-bit flash ADC, we need $2^{(n)}$-1 comparator and 2^n resistors of same value. So for 3-bit flash, 7 comparators and 8 resistors of 1KΩ are used. 7 comparators produces 7 output bits. This 7 bits are called thermometric codes, just because it consists of consecutive '1's followed by consecutive '0's at a perticular instant of time.7:3 encoder is designed using 4, 2:1 multiplexer.. Transimission gates are used for building a multiplexer. Multiplexer can be build by using numerous techniques but using transmission gates(TG) is advantageous perticularly because of its characteristic to generate output signal (both logic vaules) without any degradation.

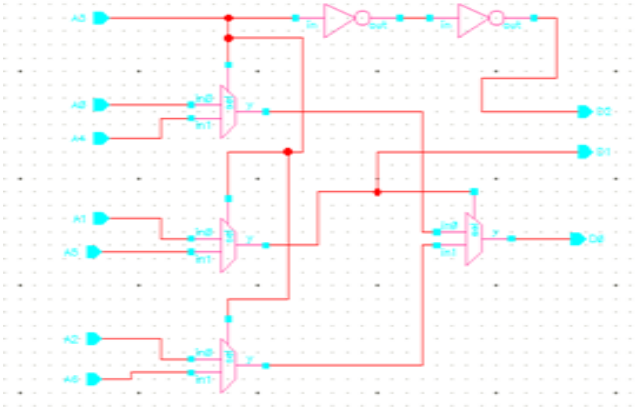

Figure 5. 7:3 Thermometric Encoder Schematic Using Mux Technique

DAC output and the output from sample and hold circuit are subtracted using OTA as a subtractor. Then the output of this subtractor generally called as "residue" is fed to residue amplifier. Residue Amplifier is built again by using OTA. By connecting each stage in cascade, we can build n-stage pipeline ADC. The no. of stages to be incorporated depends on number of bits required for a particular application and the acceptable delay between feeding input and generating digital output.

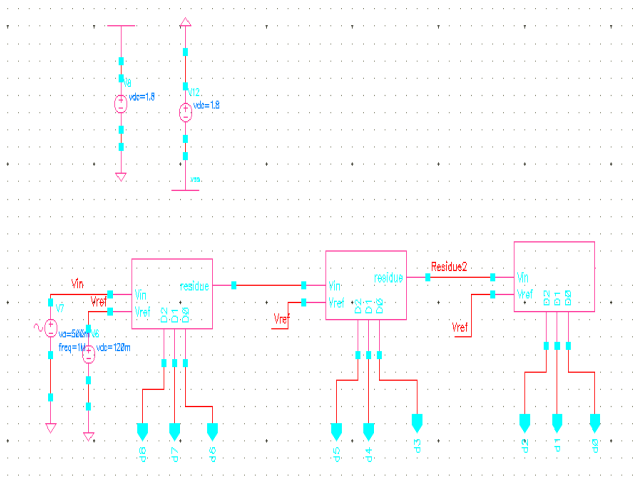

Figure 6. 9-Bit Pipeline ADC Schematic

IV. SIMULATION RESULT

All simulations were carried out in Cadence Virtuoso Software in gpdk180nm CMOS technology.

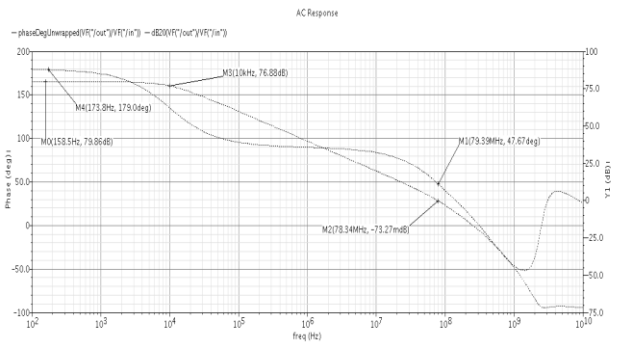

Figure 7. AC Response of Designed OTA

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OTA being heart of the design, major efforts were dedicated on design of OTA. Post simulation result for OTA is shown in table 3.

TABLE 3 OTA Measured Parameters

Gain Bandwidth Product	~ 78.34MHz
DC Gain (Av(0))	79.86dB
Phase Margin	~ 47.67 º
Common Mode Rejection Ratio(CMRR)	88.46dB
'+'Power Supply Rejection Ratio(P-PSRR)	83.78dB
'-' Power Supply Rejection Ratio(N-PSSR)	113.3dB
DC Offset Voltage(Average)	-328.9mV
'+'Slew Rate	9.57 V/µsec
'-'Slew Rate	9.93 V/µsec
Settling Time	.116 µsec

Table no. 4 enlists the power consumption required for each component used in building a 9-bit pipeline ADC

TABLE 4 Power Dissipation of Sub-Blocks

Circuit block	DC Power	Transient Power
Two stage OTA (inverting,openloop,i/p AC magnitude = 1mV)	2.0272 mW	2.355mW
Sample and Hold Circuit (500mV, 1MHz i/p signal, Fs=20MHz)	1.8313mW	1.8240 mW
7:3 Encoder(all input high)	66.4 pW	66.4 pW
3-bit ADC (500mV, 1MHz i/p analog signal, Vref=300mV) (single stage)	1.0344 mW	1.1072 mW
9-Bit Pipeline ADC	15.45 mW	48.97 mW

V. CONCLUSION

Designing an analog circuit requires patience and perseverance. No hardcore rule is defined by which we get desired result at first trail. In this paper the design and measurements of a power scalable 9-bit pipeline ADC is designed using SUB- 3bit flash ADC. Thermometric to binary encoder circuit used in 3- bit flash ADC is designed using MUX based concept. The ADC operates with a sampling frequency of 200MS/s with low power consumption of 48.97mW. All simulations where performed in Cadence Virtuoso ADE on gpdk180 nm CMOS technology.

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