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Efficient Compression of Image by Lifting Based Technique

P. Veera Swamy, B. Venkateswara Reddy, N. B. S. Naveen

Abstract— Images contain large amounts of information that requires much storage space, large transmission bandwidths and long transmission times. Therefore it is advantageous to compress the image by storing only the essential information needed to reconstruct the image. Discrete Wavelet Transform (DWT) is most popular transformation technique adopted for image compression In this work" LIFTING BASED-DWT" technique is proposed and is implemented on FPGA Instead of using ROM as a cache memory we are using FIFO as an storage device by which throughput can be increased.

Index Terms— Image compression, FIFO, Xilinx, lifting base DWT

I. INTRODUCTION

Technological growth of semiconductor industry has led to unprecedented demand for low power, high speed complex and reliable integrated circuits for medical, defence and consumer applications. Today's electronic equipment comes with user friendly interfaces such as keypads and graphical displays. As images convey more information to a user, it is many of the equipment today have image displays and interfaces. Image storage on these smaller, handled devices is a challenge as they occupy huge storage space; also image transmission requires higher bandwidth. Hence most of the signal processing technologies today has dedicated hardwares that act as co-processors to compress and decompress images. In this work, a reliable, high speed, low power DWT-IDWT processor is designed and implemented on FPGA which can be used as a co-processor for image compression and Decompression. The Discrete Wavelet Transform (DWT) has become a very versatile signal processing tool over the last decade. In fact,it has been effectively used in signal and image processing applications ever since Mallat [1] proposed the multiresolution representation of signals based on wavelet decomposition. The advantage of DWT over other traditional transformations is that it performs multiresolution analysis of signalswith localization both in time and frequency. The DWT is being increasingly used for image compression today since it supports features like progressive image transmission (by quality, by resolution), ease of compressed image manipulation, region of interest coding, etc. In fact,it is the basis of the new JPEG2000 image compression standard which has been shown to have superior performance compared to the current JPEG standard [2].

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***** Correspondence Author (s)
P. Veera Swamy, studying M.Tech Embedded Systems in Vikas College of Engineering &Technology, Hyderabad, India.
Mr. B. Venkateswara Reddy, Working as Assoc. Prof. & Head of the Department in ECE, Vikas College of Engineering & Technology, Hyderabad, India.
N. B. S. Naveen, working as Asst. Prof., in ECE Department Vikas College of Engineering and Technology, Hyderabad, India.

DWT has traditionally been implemented by convolution or FIR filter bank structures. Such implementations require both a large number of arithmetic computations and a large storage—features that are not desirable for either high speed or low power image/video processing applications. Recently, a new mathematical formulation for wavelet transformation has been proposed by Swelden [3] based on spatial construction of the wavelets and a very versatile scheme for its factorization has been suggested in [4]. This new approach is called the lifting-based wavelet transform or simply lifting. The main feature of the lifting-based DWT scheme is to break up the high-pass and low-pass wavelet filters into a sequence of upper and lower triangular matrices, and convert the filter implementation into banded matrix multiplications [4]. This scheme often requires far fewer computations compared to the convolution based DWT [3, 4] and offers many other advantages, as described later in Section 2. The popularity of lifting-based DWT has triggered the development of several architectures in recent years. These architectures range from highly parallel architectures to programmable DSP-based architectures to folded architectures. In this paper we present a survey of these architectures. We provide a systematic derivation of these architectures and commenton their hardware and timing requirements.

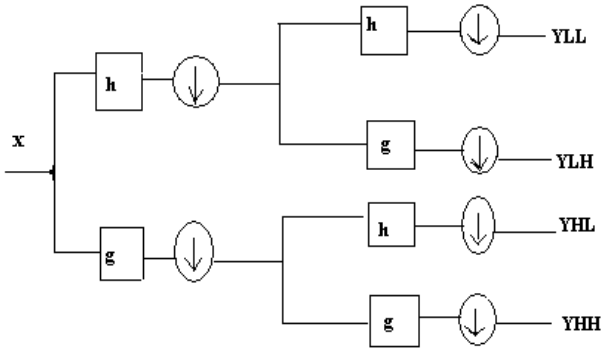

Fig. 1 DWT Compression

II. EXISTING TECHNIQUE

2.1 Distributive Arithmetic-DWT

"Discrete Wavelet Transform" consists of complexities due to huge arithmetic operations in the image compression to overcome these complexities DA-DWT technique is designed in which consists of four "Look Up Tables" (LUTs), each of the LUTs are accessed by the even and odd samples of input matrix simultaneously.

Odd and even input samples are divided into 4 bits of LSB and 4 bits of MSB, each 4-bit data read the content of four different LUTs that consist of partial products of filter values computed and stored as per the DA logic. Input samples are split into even and odd in the first stage, the data is further loaded sequentially into the serial in serial out shift registers, top four shift register store MSB bits and bottom four shift register stores the LSB bits. It requires 40 clocks cycles to load the shift register contents. At the end of 40th clock cycle, the control logic configures the shift register as serial in parallel out, thus forming the address for the LUT. The partial products stored in the LUT are read simultaneously from all the four LUTS and are accumulated with previous values available across the shift register in the output stage. The output stage consisting of adders, accumulators and right shift registers are used to accumulate the LUT contents and thus compute the DWT output. This architecture has a latency of 44 clock cycles in computing the first high pass and low pass filter coefficients, and has a through put of 4 clock cycles. The block representation of DA-DWT technique is as shown in below Fig.2.

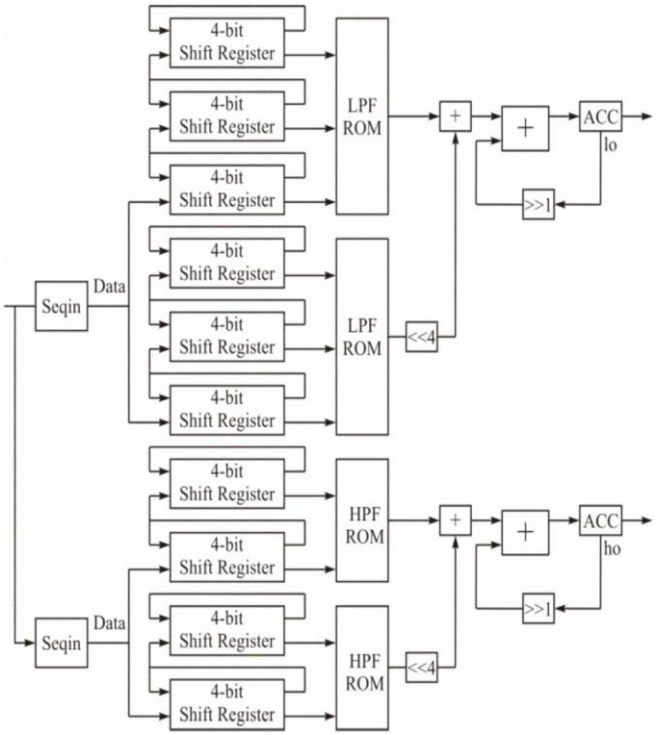

Fig. 2 Distributive Arithmetic-DWT Technique

III. PROPOSED TECHNIQUE

3.1 Lifting Based Technique

The lifting scheme is a new method to construct wavelet basis, which was first introduced by Swelden's. The lifting scheme entirely relies on the spatial domain, has many advantages compared to filter bank structure, such as lower area, power consumption and computational complexity. The lifting scheme can be easily implemented by hardware due to its significantly reduced computations. Lifting has other advantages, such as "in-place" computation of the DWT; integer-to-integer wavelet transforms which are useful for lossless coding. The lifting scheme has been developed as a flexible tool suitable for constructing the second generation wavelets. It is composed of three basic operation stages: split, predict and update. Fig.3. shows the lifting scheme of the wavelet filter computing one dimension signal. The three basic steps in Lifting based DWT are.

Split Step: where the signal is split into even and odd points, because the maximum correlation between adjacent pixels can be utilized for the next predict step. For each pair of given input samples x (n) split into even x (2n) and odd coefficients x (2n+1).

Predict Step: The even samples are multiplied by the predict factor and then the results are added to the odd samples to generate the detailed coefficients (dj).Detailed coefficients results in high pass filtering.

Update Step: The detailed coefficients computed by the predict step are multiplied by the update factors and then the results are added to the even samples to get the coarse coefficients (sj).The coarser coefficients gives low pass filtered output. The basic block represent of the Lifting Based-DWT is as shown in below Fig.3.1.1.

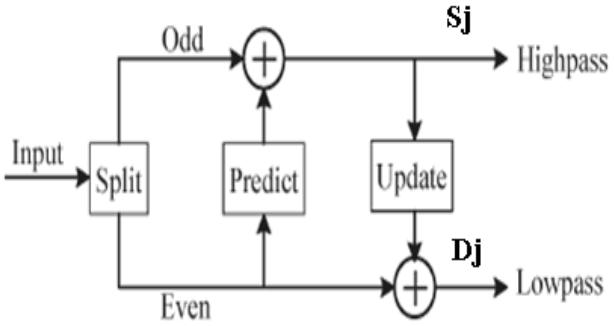

Fig. 3.1.1 Basic Block for Lifting Based Technique

In our proposal technique we are constructing the 1D-DWT block using basic block of Lifting Based technique in which the input value is stored in every storage device "D" and then it is given to accumulator as an input with feedback then it is again stored in the memory storage which is temporary. External coefficients are given to the multiplier as input with the previous storage memory output as input to multiplier, these two inputs are multiplied then result is stored in another temporary storage memory. Then all these multipliers output is given to accumulator to sum all these coefficients and then it is given to permanent memory device. The block representation is as shown in below Fig.3.1.2.

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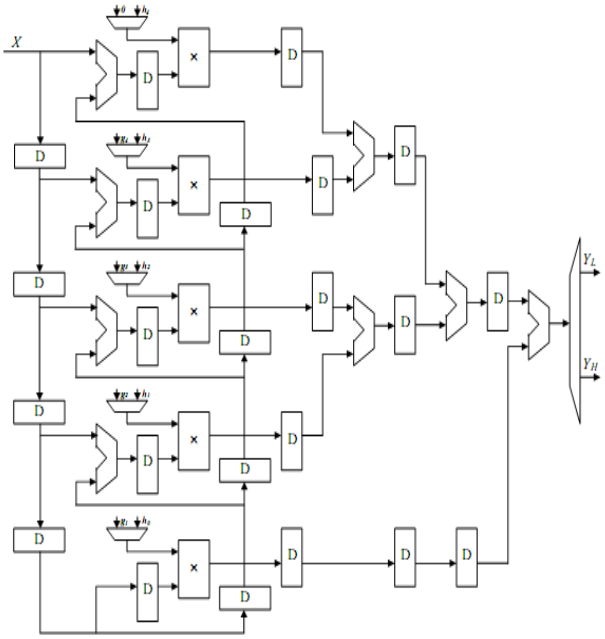

Fig. 3.1.2 1D-DWT Lifting Based Technique

IV. FPGA IMPLEMENTATION

The developed model is simulated using test bench. The HDL model is synthesized using Xilinx ISE targeting Vertex 5-pro FPGA. The proposed design is implemented and the synthesis report is generated. The results obtained are presented in Table as shown below. The proposed design implemented on FPGA occupies 12% of the total slices on FPGA, thus the proposed architecture has the higher area utilization and throughput. Thus the synthesis report is as shown below in table.1.

Table 1 Synthesis Report

LOGIC UTILIZATION	EXISTING METHOD			PROPOSED METHOD		
Selected Device	Vertex 2(Xc2vp30ff896-7)			Vertex 5 (Xc4vlx15-10ff676)		
	USED	AVAILABLE	UTILIZATION	USED	AVAILABLE	UTILIZATION
Number of Slices	832	13696	6%	2603	21,504	12%
Number of LUT'S	1186	27392	4%	1855	21,504	8%
Number of flip flops	634	27392	2%	1214	27392	4%
Number of IOB'S	19	416	4%	81	448	18%

V. VERIFICATION OF RESULTS

The whole design of Lifting Based technique is simulated using XILINX software.

5.1 Area Utilization Using Lifting Based Simulation Results

Simulation results for the proposed design is as shown in the below Figures 5.1. Using this technique we have increased the area utilization on the VERTEX 5 FPGA as twice the existing technique.

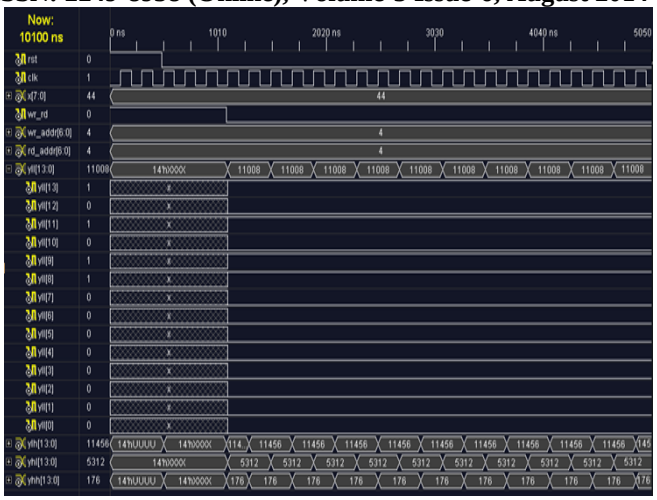

Fig. 5.1 Lifting Based-DWT Output

5.2. Simulation Result of Using FIFO

Instead of using ROM as a memory we have used "First In First Out" technique as an cache memory to overcome the through and latency problem. From the output we can see that for one clock cycle both read and write operations are done through which throughput is increased as the latency decreased. the simulation result is as shown in below Fig5.2.

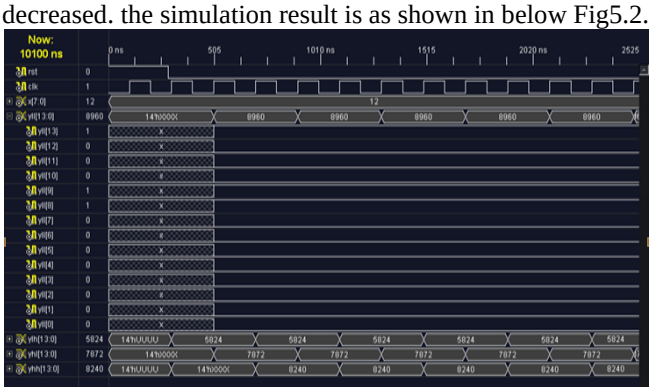

Fig. 5.2 FIFO Output

VI. CONCLUSION

In this paper, we proposed a design of Lifting Based technique. In this area utilization is more than the existing model and the synthesis report says that the logical utilization of Lifting Based technique is twice that of the existing technique on the VERTEX 5 FPGA. Instead of ROM we have used FIFO to increase the throughput. Hope this Lifting Based technique meets the modern compression needs. The design has great flexibility, high integration. Because of using FIFO data loss is avoid

VII. ACKNOWLEDGMENTS

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P. Veera Swamy, studying M.Tech Embedded Systems in Vikas College of Engineering &Technology. I attend the seminars on Embedded Systems in varies colleges.

Mr. B. Venkateswara Reddy, Working as Associate Professor & Head of the Department in ECE, Vikas College of Engineering & Technology. He Is Pursuing Ph.D From JNTU Hyderabd In Image Processing. So far he published 3 International Journals & Attended 2 national conferences. He is a life member in ISTE.

N. B. S. Naveen, working as Assistant Professor in ECE Department Vikas College of Engineering and Technology. Completed M.Tech in Embedded System from Gudlavalleru Engg. College with Distinction and published paper on VLSI based project.

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