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Image Compression Using Fuzzy Enhancement

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Abstract-Fuzzy logic is a way to embed an engineer's experience into the system. It mathematically emulates human reasoning, provides an intuitive way to design function blocks for intelligent control systems, advanced fault detection and other complex applications. The fuzzy logic, unlike conventional logic system, is able to model inaccurate or imprecise models. The fuzzy logic approach offers a simpler, quicker and more reliable solution that is clear advantages over conventional techniques. It can significantly improve response so we are actively incorporating fuzzy logic into many real time applications. Image processing is one of the area where fuzzy can be utilized for the image enhancement. Image compression is one of the major image processing techniques that is widely used in medical, automotive, consumer and military applications. In this project fuzzy technique has been used in image compression with Discrete Wavelet Transforms (DWT) technique. Discrete wavelet transforms is the most popular transformation technique adopted for image compression. Complexity of DWT is always high due to large number of arithmetic operations. In order to minimize the complexity of DWT, modified DA split architecture has been proposed and implemented on FPGA.

Key Words: DA split architecture, Discrete wavelet transforms (DWT), Fuzzy logic, Image processing

I. INTRODUCTION

Every day, we encounter an enormous amount of information that is stored, processed, and transmitted digitally. Today's electronic equipment comes with user friendly interfaces such as keypads and graphical displays. As images convey more information to a user, it is many of the equipment today have image displays and interfaces.
Image storage on these smaller, handled devices is a challenge as they occupy huge storage space; also image transmission requires higher bandwidth. In particular, there is an ever increasing use of digital images, especially in the internet. This has led to the development of image compression techniques that enable more economical use of storage space and faster data transfer. For example, if one image, in an uncompressed file format is transmitted, such as the popular BMP format, then the file size can be huge and image transmission over the internet will be take too long to complete. Specifically, an image with a pixel resolution of 1024 by 1024 pixels, and 24-bit color resolution will take up 1024 * 1024 * 24 / 8 = 3,145,728 (3MB) of storage space, and 7 minutes for transmission, utilizing a high speed of 64Kbit/s, in an ISDN line. On the other hand, if the image is compressed at a 10:1 compression ratio, then the storage space requirement is reduced to 300KB only and the transmission time drops to under 6 seconds. Thus, the necessity for compression is obvious.

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Image compression addresses the problem of reducing the amount of data required to represent a digital image. From the information theory viewpoint, the image compression is the removal of redundant information, explicitly, by keeping the not definite information, and removing the determined information. From the mathematical viewpoint, image compression is the transformation of a 2-D pixel array into a statistically uncorrelated data set. The transformation is applied to storage or transmission of the image. At some rate, the compressed image is decompressed to reconstruct the original image or an approximation of it. There exist a number of universal data compression algorithms that can compress almost any kind of data, of which the best known are the family of Ziv-Lempel algorithms. These methods are lossless in the sense that they retain all the information of the compressed data. However, they do not take advantage of the 2-dimensional nature of the image data; Images have certain statistical properties, which can be exploited by encoders especially designed for them. Also, some of the finer details in the image can be sacrificed for the sake of saving a little more storage space and bandwidth. This means lossy image compression technique can be used in this area. The Discrete Wavelet Transform (DWT) is being increasingly used for image coding. This is because the DWT can decompose the signals into different sub-bands with both time and frequency information. It also supports features like progressive image transmission, compressed image manipulation, and region of interest coding. In wavelet transforms, the original signal is divided into frequency resolution and time resolution contents. In this work, a reliable, high speed, low power DWT IDWT processor is designed for image compression and decompression and implemented on FPGA.

II. PROBLEM DEFINITION

Technological growth of semiconductor industry has led to unprecedented demand for low power, high speed complex and reliable integrated circuits for medical, defence and consumer applications. Today's electronic equipment comes with user friendly interfaces such as keypads and graphical displays. As images convey more information to a user, it is many of the equipment today have image displays and interfaces. Image storage on these smaller, handled devices is a challenge as they occupy huge storage space; also image transmission requires higher bandwidth. Hence there is a need of best image compression technique for reducing bandwidth and storage space and it has to perform the compression and decompression at faster rate without the loss of information.

III. METHODOLOGY

Initially a large size of image has been resized into 100 by 100 pixel image. A pixel values are stored into the memory.

The stored values of pixels from the memory read out serially and stored into the splitted look up table within each clock pulse, then based on DWT and Distributed architecture compression and decompression has been performed.
The recovered Pixel values have been written back to RAM. Once the whole process gets over, the generated bit file is dumped into a FPGA. Through VGA port both the original and recovered image can be seen in the monitor.

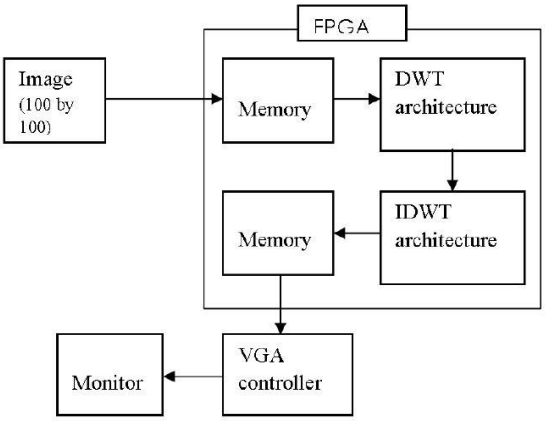

Fig.1. Block Diagram
Figure 1 shows the flow of whole project.

A. DISCRETE WAVELET TRANSFORM

The Wavelet Series is just a sampled version of continuous wavelet transform and its computation may consume significant amount of time and resources, depending on the resolution required. The Discrete Wavelet Transform (DWT), which is based on sub-band coding is found to yield a fast computation of Wavelet Transform. It is easy to implement and reduces the computation time and resources required.
In the case of DWT, a time-scale representation of the digital signal is obtained using digital filtering techniques. The signal to be analyzed is passed through filters with different cutoff frequencies at different scales.

B. DWT ARCHITECTURE

Image consists of pixels that are arranged in two dimensional matrixes, each pixel represents the digital equivalent of image intensity. In spatial domain adjacent pixel values are highly correlated and hence redundant. In order to compress images, these redundancies existing among pixels needs to be eliminated. DWT processor transforms the spatial domain pixels into frequency domain information that are represented in multiple sub-bands, representing different time scale and frequency points. Human visual system is very much sensitive to low frequency and hence, the decomposed data available in the lower sub-band region and is selected and transmitted, information in the higher sub-bands regions are rejected depending upon required information content. In order to extract the low frequency and high frequency sub-bands DWT architecture shown in figure below is used. As shown in the figure, input image consisting rows and columns are transformed using high pass and low pass filters. The filter coefficients are predefined and depend upon the wavelets selected. In this work, 9/7 wavelets have been used for constructing the filters.
First stage computes the DWT output along the rows, the second stage computes the DWT along the column achieving first level decomposition. Low frequency sub-bands from the first level decomposition is passed through the second level and third level of filters to obtain multiple level decomposition as shown in Figure 2

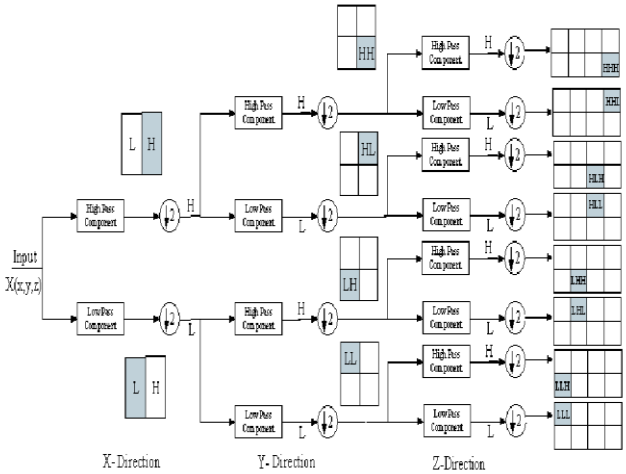

Fig.2. DWT Architecture

There are several architectures used for realizing the DWT shown in Figure 2. Most popular one is the DA-DWT scheme that is suitable on FPGA, as it consumes fewer resources and has high throughput. In this project modified DA split LUT architecture has been proposed as shown in the figure 3. DA-DWT scheme that is suitable on FPGA, as it consumes fewer resources and has high throughput. DA-DWT architecture based on pipelining and parallel processing logic is realized and implemented on FPGA. In this number of LUTs and number of shift registers are reduced by exploiting the symmetric property of the 9/7 wavelet filters. Efficient fixed point number representation scheme is identified to accurately represent the 9/7 filter values and are stored in the LUT memory space on FPGA. A control logic designed loads the input data into the FPGA from the external memory, LUT contents are read out based on the input samples as address to LUT. DWT outputs are computed every clock cycle. In the computation process fuzzy arithmetic operators and fuzzy neuro D-flip-flop has been used in order to increase the computation speed which is very essential in compression.

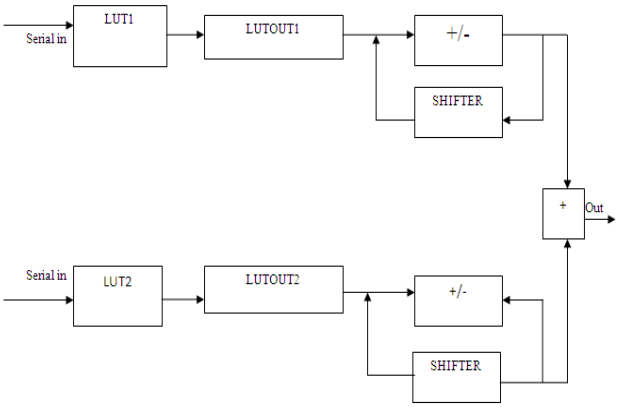

Fig.3. DA Split LUT Architecture

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C. IP BLOCK

In electronic design a semiconductor intellectual property core, IP core, or IP block is a reusable unit of logic, cell, or chip layout design that is the intellectual property of one party. IP cores may be licensed to another party or can be owned and used by a single party alone. The term is derived from the licensing of the patent and source code copyright intellectual property rights that subsist in the design. IP cores can be used as building blocks within ASIC chip designs or FPGA logic designs.
In this project IP core has been used for both the memory read and memory write operations. Hence reduces the coding complexity involved in the whole process and optimized design can be achieved.

IV. MODEL DESIGN

Image compression is done using DA-DWT. Input image is rescaled into 100×100 and is processed using DWT and IDWT algorithm. Decomposed sub-band components are selected to achieve different compression ratios. In this case, bits per pixels are used to express the compressed data. Based on these results, the hardware reference model is designed and developed.

V. FPGA IMPLEMENTATION

Virtex FPGAs are programmed using Verilog HDL; a popular hardware description language . The language has capabilities to describe the behavioral nature of a design, the data flow of a design, a design's structural composition, delays and a waveform generation mechanism. Models written in this language can be verified using a Verilog simulator. As a programming and development environment, Xilinx ISE Foundation Series tools have been used to produce a physical implementation for the Virtex FPGA. Field programmable gate arrays (FPGAs) provide a new implementation platform for the discrete wavelet transform.
The Design makes the maximal utilization of the lookup table (LUT) architecture of Virtex FPGAs by reformulating the wavelet transform computation in accordance with the distributed arithmetic algorithm. Distributed arithmetic makes extensive use of look-up tables, which makes it ideal for implementing the discrete wavelet transform functions onto the LUT-based architecture of Virtex FPGAs. Moreover, distributed arithmetic is suitable for low power portable applications because it allows replacement of costly multipliers with shifts and look-up tables. Indeed, one of the unique features of our discrete wavelet transform implementation is exploiting the natural match between the Virtex architecture and distributed arithmetic.

VI. SIMULATION RESULTS

Simulation result for the proposed design is shown in figurer 5. Input vectors that were obtained from MATLAB test inputs were used for validating the HDL results. Input vectors are stored in an ROM and are read into the modified DADWT architecture. The decomposed outputs are stored back and are also displayed using simulation waveforms.

Fig.4. Simulation Result

Figure 4 shows the compressed and decompressed output in terms of pixel values.
The original image and the reconstructed image can be seen in the monitor.

Fig.5.Original and Reconstructed Image

VII. CONCLUSION

An image compression algorithm was simulated using Verilog to comprehend the process of image compression. It offers a better reproduction of image at its edges. It also supports faithful reproduction of the image, keeping the size of the transform coefficient matrix equal to the image size. For the VLSI implementation of an image compression encoder, Verilog HDL was chosen. The relative area and speed efficiencies of DA turn out to be good on hardware implementation on FPGA. An implementation process included fuzzy arithmetic operators which make the computation quite faster and fuzzy helps to enhance the image better way in the presence of noise.

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The reconstructed image has got better edges in this design compared to the previous work. In the implementation results it is clear that DA based architectures have an area, speed and simplicity advantage over any other method based on implementations. It is in this context, we can say that DA implementations are superior when targeting FPGAs.

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