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Design and Analysis of Conventional CMOS and Energy Efficient Adiabatic Logic for Low Power VLSI Application

Anamika Mishra, Anju Jaiswal, Ankita Jaiswal, A.K.Niketa

Abstract*— *In recent years, low power circuit design has been an important issue in VLSI design areas. Adiabatic logics, which dissipate less power than static CMOS logic, have been introduced as a promising new approach in low power circuit design. energy. This paper proposes an Adder circuit based on energy efficient two-phase clocked adiabatic logic. A simulative investigation on the proposed 1-bit full adder has been implemented with the proposed technique and hence compared with standard CMOS, Positive Feedback Adiabatic Logic (PFAL) and Two-Phase Adiabatic Static Clocked Logic (2PASCL) respectively. Comparison has shown a significant power saving to the extent of 70% in case of proposed technique as compared to CMOS logic in 10 to 200MHz transition frequency range. Comparative results has also been shown by a histogram which represents the least power dissipation of proposed technique. In this paper all circuits are analyzed in terms of power using 0.35um technology and simulated using Pspice .

Keywords*—*Adiabatic logic , energy recovery ,power supply ,low power ,Full adder ,Positive feedback adiabatic logic ,2PASCL

I. INTRODUCTION

New generation of processing technology are being developed while present generation of devices are at very safe distance from fundamental physical limits. Need for low power VLSI chips arise from evolution forces of integrated chips. VLSI design is a modular technology originated by Carver Mead and Lynn Conway for saving microchip area by minimizing the interconnect fabric area. Low power is needed because of desirability of portable devices like cell phones batteries and in biomedical field like in heart pacemakers, however large power dissipation requires larger heat sinks hence increased area.So the main purpose is to provide new low power solutions for VLSI designers [1]. Especially, this work focuses on the reduction of power dissipation, which is showing an ever-increasing growth with the scaling down of the technologies. Various techniques at different levels of design process have been implemented to reduce power dissipation at the circuit, architectural and system level.

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Furthermore, the number of gates per chip area is constantly increasing while gate switching energy does not decrease at the same rate, so the power dissipation rises and heat removal becomes more difficult and expensive. Alternative solutions to limit power dissipation at each level of abstraction are proposed in this work[2]. The term adiabatic comes from the thermodynamics used to describe a process in which there is no exchange of heat with the environment. The adiabatic logic structure dramatically reduces power dissipation. The adiabatic switching technique can achieve very low power dissipation but at the expense of complexity. Adiabatic logic offers a way to use the energy stored in load capacitors rather than the traditional way of discharging load capacitor to the ground and wasting this energy.[4] Here we are using full adder as adiabatic logic circuit and comparing its power consumption with different logic circuits. Power minimization is one of the primary concerns in today VLSI design methodologies because of two main reasons one is the long battery operating life requirement of mobile and portable devices[6] and second is due to increasing number of transistors on a single chip leads to high power dissipation and it can lead to reliability and IC packaging problems. One of the main causes o energy dissipation in CMOS circuits is due to the charging and discharging of the node capacitances of the circuits, present both as a load and as parasitic.[7] The process of charging and discharging the node capacitances is carried out in a way so that a small amount of energy is wasted and a recovery of the energy stored on the capacitors is achieved.

This paper has been segmented into five sections. The section II describes the working of adiabatic logic, section III describes about the adiabatic logic families whereas section IV and V are all about the simulation results and conclusions.

II. ADIABATIC SWITCHING

Conventional Switching There are three major sources of power dissipation in digital CMOS circuits those are dynamic, short circuit and leakage power dissipation. The dominant component is dynamic power dissipation and is due to charging, discharging of load capacitance. The equivalent circuits of CMOS logic for charging and discharging is shown in Fig.1. The expression for total power dissipation is given by:

$$P_{tot} = \alpha .CL .V .Vdd. fclk + Isc .Vdd + Ile .Vd \quad (1)$$

Equation (1), the first term represents the dynamic power, where CL is the loading capacitance, fclk is the clock frequency, and α is the switching activity.

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In most cases, the voltage swing V is the same as the supply voltage Vdd however, in some logic circuits, the voltage swing on some internal nodes may be slightly less. The second term is due to the direct-path short circuit current Isc which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current Ile which can arise from substrate injection and sub threshold effects is primarily determined by fabrication technology considerations.[8] [9].

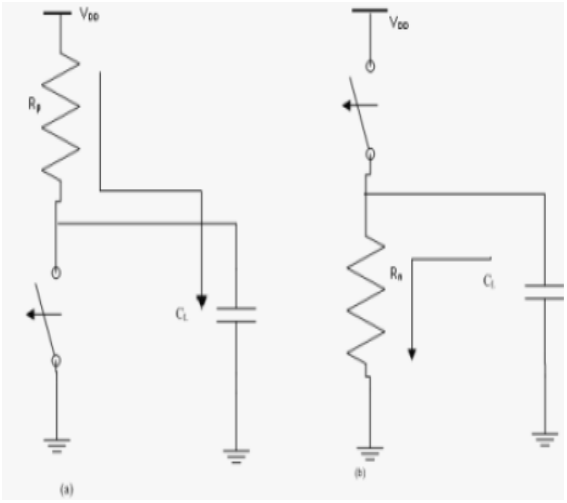

Fig. 1Conventional CMOS (a) Charging (b) Discharging

Adiabatic switching can be achieved by ensuring that the potential across the switching devices is kept arbitrarily small. This can be achieved by charging the capacitor from a time-varying voltage source or constant current source as shown in Fig. 2. Here, R represents the on resistance of the PMOS network. Also note that a constant charging current corresponds to a linear voltage ramp. Assuming that the capacitance voltage VC is zero initially, the variation of the voltage as a function of time can be found as

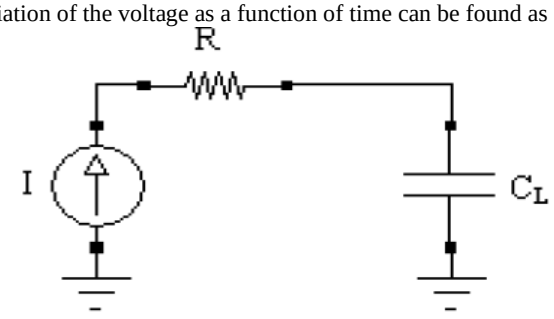

Fig. 2 Schematic for adiabatic charging process

$$Vc(t) = Is \cdot t / 2 \quad (2)$$

Hence the charging current can be expressed as a function of Vc and time t

$$Is = C.Vc(t) / 2 \quad (3)$$

The amount of energy dissipated in the resistor R from t = 0 to *t* = T can be found as

$$Ediss = R. \int_T Is^2 dt = R \cdot Is^2.T \quad (4)$$

Combining (3) and (4), the dissipated energy during this charge-up transition can also be expressed as

$$Ediss = (RC/T).C.\ Vc^2\ (T) \quad (5)$$

From (5) we can say that the dissipated energy is smaller than for the conventional case if the charging time T >>2RC and can be made small by increasing the charging time. A portion of the energy thus stored in the capacitance can also be reclaimed by reversing the current source direction, allowing the charge to be transferred from the capacitance back into the supply[10]. Adiabatic logic circuits thus require non-standard power supplies with time-varying voltage, also called pulsed power supplies. The additional hardware overhead associated with these specific power supply circuits is one of the design trade-off. Practical supplies can be constructed by using resonant inductor circuits. But the use of inductors should be limited from integrated circuit point because of so many factors like chip integration, accuracy, efficiency etc. An alternative to using pure voltage ramps is to use stepwise supply voltage waveforms, where the output voltage of the power supply is increased and decreased in small increments during charging and discharging. Since the energy dissipation depends on the average voltage drop across the resistor by using smaller voltage steps the dissipation can be reduced considerably. The total dissipation using step wise charging is given by (6).

$$Etdiss = (1/n).\ C.\ Vdd^{2}/\ 2 \quad (6)$$

Where n is number of steps used to charge up capacitance to Vdd. In literature, adiabatic logic circuits classified into two types: full adiabatic and quasi or partial adiabatic circuits. Full-adiabatic circuits have no non-adiabatic loss, but they are much more complex than quasi-adiabatic circuits. Quasi-adiabatic circuits have simple architecture and power clock system.[11] There are two types of energy loss in quasi adiabatic circuits, adiabatic loss and non adiabatic loss. The adiabatic loss occurs when current flows through non-ideal switch, which is proportional to the frequency of the power-clock.

III. ADIABATIC LOGIC

A. PFAL

The structure of Positive Feedback Adiabatic Logic PFAL logic is shown in figure 3. Two n-trees realize the logic functions. This logic family also generates both positive and negative outputs. The two major differences with respect to ECRL are that the latch is made by two PMOSFETs and two NMOSFETs, rather than by only two PMOSFETs as in ECRL, and that the functional blocks are in parallel with the transmission PMOSFETs.[12] Thus the equivalent resistance is smaller when the capacitance needs to be charged. The ratio between the energy needed in a cycle and the dissipated one can be seen in figure 3. During the recovery phase, the loaded capacitance gives back energy to the power supply and the supplied energy decreases. The partial energy recovery circuit structure so called Positive Feedback Adiabatic Logic (PFAL), has good robustness against technological parameter variations. It is a dual rail circuit; the core of all the PFAL circuit is adiabatic amplifier, a latch made up by the two PMOS and two NMOS that avoids a logic level degradation on the output nodes. The two n-tree release the logic functions. The functional blocks are in parallel with P-MOSFETs and form a transmission gate.

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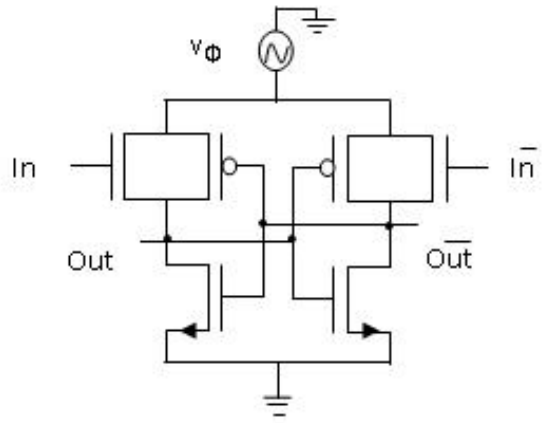

Fig. 3 PFAL Logic Circuit

B. 2 PASCL:

Fig 4. shows circuit diagram of Two Phase Adiabatic Static Clocked Logic(2PASCL).In the logic families which include diode in charging path suffer from output amplitude degradation. To deal with this problem, Anuar et al proposed a new logic family named as two phase clocked adiabatic static CMOS logic . This logic family like other families discussed here, we have used MOSFET as diode by shorting gate and drain of MOSFET together does not include diode in charging path, so that output amplitude degradation does not occur. The 2 phase clocked adiabatic static CMOS logic uses a two phase clocking split level sinusoidal power supply. One is in phase while the other is inverted. The voltage level of Vclk exceeds that of Vclk by VDD/2. By using these two split – level sinusoidal waveforms, which have peak to peak voltages of 0.9V, the voltage difference between the current carrying electrodes can be minimized and subsequently, power consumption can be suppressed. It uses two diodes- one diode is placed between output node and power clock, Vclk and the other diode is placed adjacent to nmos logic circuit and connected to other power clock Vclk . Both the diodes are used to recycle the charge from output node and to improve the discharging speed of internal nodes.

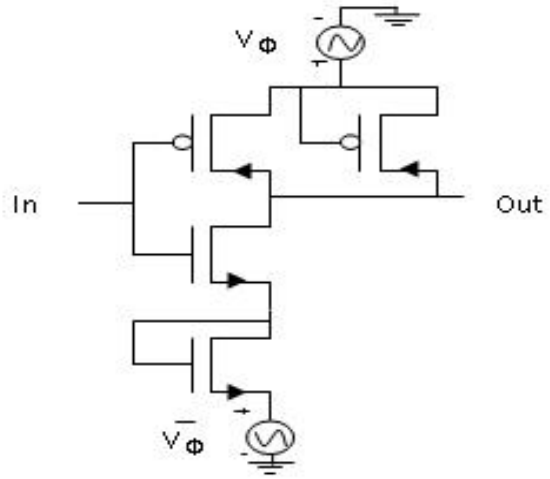

Fig. 4 Two Phase Adiabatic Static Clocked Logic (2PASCL)

C. PROPOSED ADIABATIC LOGIC INVERTER:

The basic inverter circuit is shown in above figure 6 of this circuit is an adiabatic amplifier, a latch made by the two PMOS *M1* and *M2* and two NMOS *M5* and *M6*, that avoids the logic level degradation at Out and Out, the logic circuit *M3* and *M4* are in parallel with *M1* and *M2* and forms transmission gate [13]. This circuit uses two-phasesplit level sinusoidal power supplies which are denoted as VΦ and VΦ, where VΦ & VΦ can vary from 1.3 to 1.6V & 0.3 to 0V respectively.

The circuit operates in two phases, evaluation and hold, in evaluation phase, VΦ swings up and VΦ swings down, and in hold phase, VΦ swings up and VΦ swings down. Let us assume, during evaluation phase the input (In) is high and input (In) goes low accordingly, consequently *M3* is conducting and output (Out) follows the power supply VΦ, and at the same time *M1* gets turned *ON* by output (Out) and thus reduces the charging resistance. Being in parallel with M3 and during hold phase, charge stored on the load capacitance C_L flows back to power supply through M1 so that power dissipation is reduced [14]. The proposed technique uses the two MOS diodes, one is connected to Out and VΦ and other diode is connected between common source of M5-M6 and other power supply VΦ bar, both the MOS diodes are used to increase the discharging rate of internal nodes.

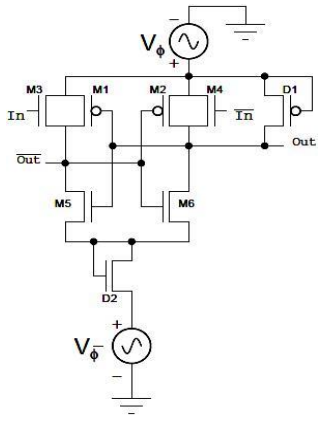

Fig. 6 Proposed Adiabatic Logic Inverter Circuit

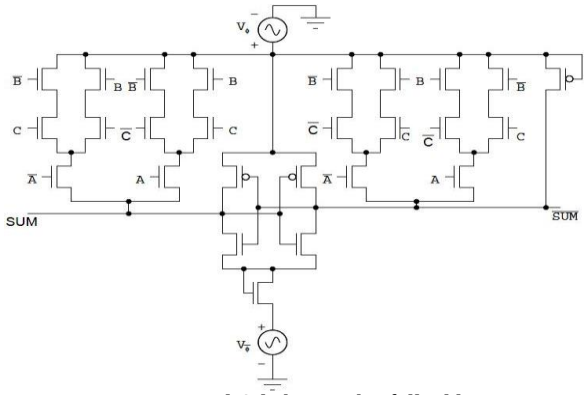

Fig. 7 Proposed Adiabatic 1-bit full adder sum

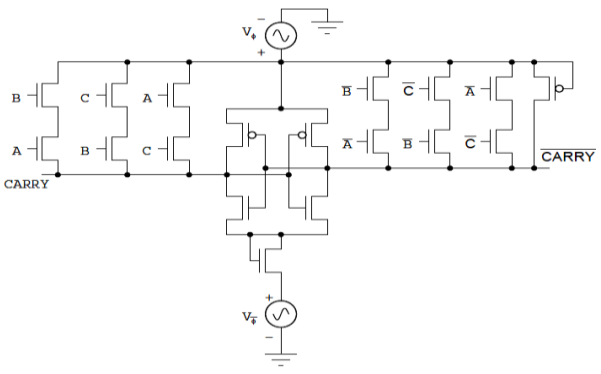

Fig.8 Proposed Adiabtic 1-bit full adder carry

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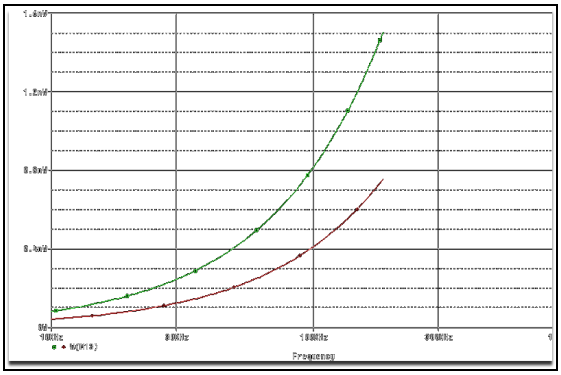

Fig 9 (a) Sum and carry of proposed Adiabatic technique.

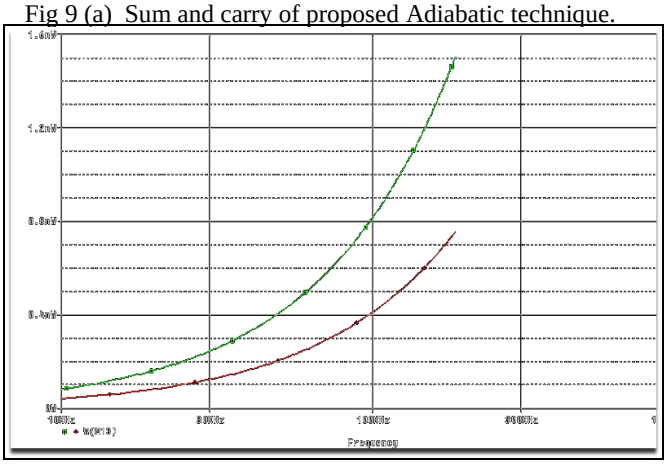

Fig. 9 (b) Power Dissipation between 1-bit full adder and PFAL

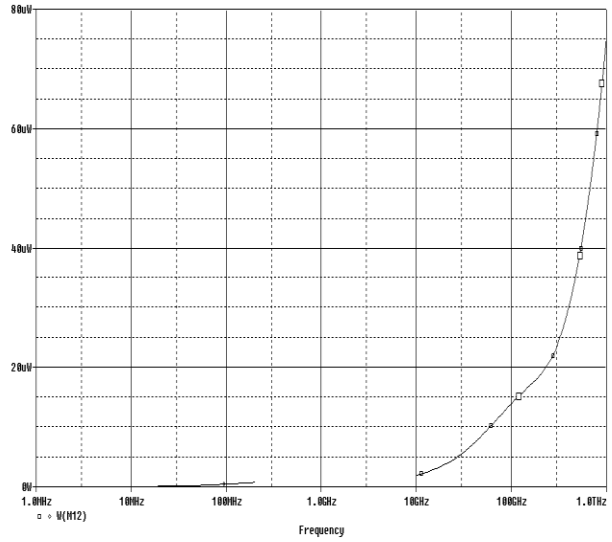

Fig. 9 (c) Power Dissipation between 1-bit full adder and 2PASCL

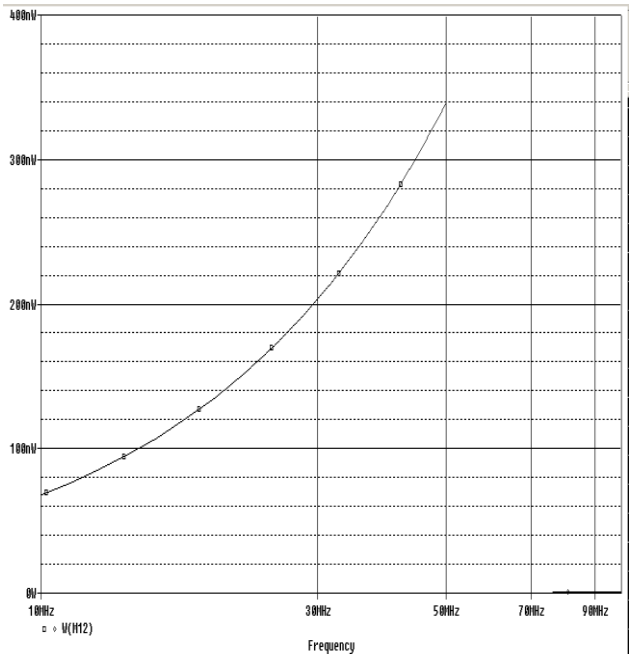

Fig. 9 (d). Power dissipation between 1-bit full adder and Standard

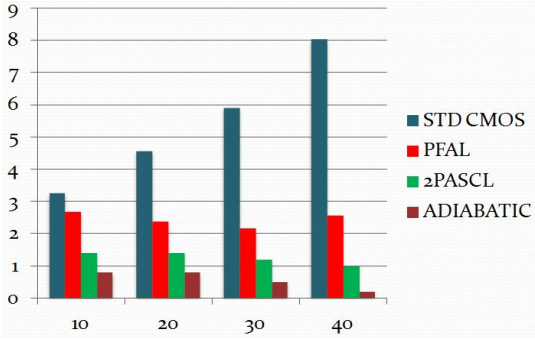

Fig. 10. Histogram showing comparison between power dissipation and transition frequency.

IV. SIMULATION RESULTS AND ANALYSIS

Output waveform: The spice simulation results obtained for proposed adiabatic 1-bit full adder with PFAL,2PASCL and Standard CMOS is shown in Fig.9(a), Fig.9(b) Fig.9(c) & Fig.9(d) showing comparison between power dissipation and transition frequency.Fig.10 shows a histogram (drawn between power dissipation and transition frequency) which shows comparison between proposed adiabatic 1-bit full adder,PFAL,2PASCL and Standard CMOS.

V. CONCLUSION

A simulation result obtained from the proposed inverter and 1-bit full adder have got strong validation and gives a low power dissipation at low frequency range. The comparison of the proposed circuit with other traditional methodologies has proved that power consumption with the proposed logic is for less as compared to CMOS ,PFAL and 2PASCL based techniques.

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For instance, when the input frequency varies from 10 to 150MHz, the proposed inverter and 1-bit full adder circuits dissipate minimally as only 12% and 21% power of the total power of a static CMOS based logic circuit. In conclusion, an energy efficient adiabatic technique that would reduce the power consumption. The histogram shows the power dissipation of proposed technique is least as compared to other logic circuits.

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