A 2.8 GHz Low Power High Tuning Voltage Controlled Ring Oscillator

M. Sai Sarath Kumar, M. Aarthy

Abstract—This work describes a two-stage CMOS Voltage Ring Oscillator (VCRO) using differential delay cells are analyzed. The main aim of the paper is to increase the tuning range of the circuit and obtain a good phase noise at the cost of design complexity and power consumption. Two-stage VCRO implemented in 90 nm Technology realizes a tuning range of 53.40% and a phase noise of -156.328 dBc/Hz for a power consumption of 9.85mW. The phase noise of the VCRO is bettered by cascading more number of stages to trade off power consumption. A four-stage VCRO is implemented and achieved a tuning range of 62.15% and a phase noise of -116.608 dBc/Hz. However the power consumption of the circuit increased to 16.45mW.

Keywords—Voltage Ring Oscillator, Phase Noise, Tuning Range

I. INTRODUCTION

The Phase Locked Loop (PLL) is one of the most common functional blocks used in communication systems such as in modern transceivers for wireless communication. Phase locked loop (PLL) is one of the main blocks in RFIC design, which contains voltage controlled oscillator. The Voltage Controlled Oscillator (VCO) is an important building block in PLL because it directly provides the output signal of the PLL. A CMOS VCO can be built using ring structures, relaxation circuits or an LC circuits. LC circuits exhibit much better phase noise with high quality factor (Q) but using high quality inductors increases the complexity of the circuit design. It also involves problems of eddy currents and cost of the circuit. In contrast, ring oscillators on other side require less die area. Ring Oscillators can be integrated on chip without any extra steps. With 2n number of delay cells, ring oscillators provide good phase noise, in-phase outputs and wide tuning range. A VCO is a positive feedback control system circuit. Differential architectures tend to be preferred over single ended designs because it provides immunity to common mode noise. It also provides improved spectral purity and 50% duty cycle at the output.

This work illustrates the VCO architecture proposed in [1] and modified the circuit using GPDK 90nm technology in Cadence Virtuoso Analog Design Environment.

II. RING OSCILLATOR

The topology of VCRO proposed in [1] is analyzed and redesigned in this work. Differential architectures tend to be preferred over single ended designs because of they include better immunity to common mode noise. And their improved spectral purity and 50% duty cycle at the output. The block diagram of a N-Stage Differential ring oscillator is shown.

Fig. 1 Block diagram of VCRO

When even number of stages is being used the required phase shift ‘π’ can be achieved by reversing one of the connections in the architecture introducing a DC phase inversion. Different delay cell designs have been proposed by many authors. The Delay cell proposed in this work has better tuning range when compared to the design in [1]. Power consumption of the proposed cell is improved to that of schematics proposed in [1] and [2]. The work done in [1] is 0.18µm and hence technology enhancement is done and performance analysis is done using 90nm CMOS technology. The schematic of the proposed delay cell is analyzed using GPDK 90nm technology in Cadence Virtuoso Analog Design Environment.

Fig. 2 Circuit schematic of Delay Cell

The circuit cell consists of two NMOS transistors (NMOS1 and NMOS2), for oscillation there are two PMOS transistors (PMOS2 and PMOS3) which act as positive feedback, at the top there is one PMOS transistor (PMOS5) for better frequency tuning and two diode-connected PMOS transistors (PMOS1 and PMOS4). This design is mainly proposed for better phase noise and tuning range. Low power consumption is also achieved in this work.
The two-stage voltage controlled ring oscillator is implemented and analyzed in this work and to extension to that four-stage is also implemented and performance analysis is done.

To increase the transconductance to capacitance ratio \( \frac{g_m}{C} \) NMOS pair is used so as to obtain high frequency range of operation. As the capacitors considered here are only parasitic capacitors, there will be decrement in power consumption and bulk area. The \( g_m \) value of the diode connected PMOS transistors (PMOS1 & PMOS4) by which wider tuning range can be achieved is varied by PMOS5, which is used to control the current flow through those transistors (PMOS1 & PMOS2) hence controlling the frequency. The PMOS transistors (PMOS2 & PMOS4) are connected to the supply voltage for maximum output swing and to reduce the noise power for better phase noise performance.

The oscillating frequency of the ring oscillator given in [1] is

\[
F_{osc} = \frac{1}{2\pi} \sqrt{\frac{g_{m1}-g_{m2}+g_{L}}{C_L}} \tag{1}
\]

In the above expression, \( g_m \) is the transconductance of the transistors and \( C_L \) is the capacitance load and \( G_L \) is the conductance load.

By adjusting the transconductance \( g_m \) of the PMOS transistors (PMOS1 & PMOS4) oscillating frequency can be tuned. The oscillating frequency range i.e. maximum frequency and minimum frequency can be achieved by using the below expressions.

\[
F_{max} = \frac{1}{2\pi} \sqrt{\frac{g_{m1}-g_{m2}}{C_L}} \tag{2}
\]

\[
F_{min} = \frac{1}{2\pi} \sqrt{\frac{g_{m1}+g_{m2}}{C_L}} \tag{3}
\]

From the above equations operating frequency of the proposed cell is obtained at 2.8GHz. The design parameters for the proposed cell is given below in Table 1.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W/L</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMOS1 &amp; PMOS4</td>
<td>20µ/200n</td>
</tr>
<tr>
<td>PMOS2 &amp; PMOS3</td>
<td>20µ/200n</td>
</tr>
<tr>
<td>NMOS1 &amp; NMOS2</td>
<td>7µ/200n</td>
</tr>
<tr>
<td>PMOS5</td>
<td>16µ/200n</td>
</tr>
</tbody>
</table>

In proposed cell parameters instead of 90nm as gate length 200nm is taken so as to minimize the effect of flicker noise which is the major source for phase noise. Sizing of the transistor is done accordingly and implemented in GPDK 90nm technology.

### III. SIMULATION RESULTS

The proposed ring oscillator is simulated in GPDK 90nm technology using CADENCE virtuoso analog design environment. In this work transient analysis, operating frequency, tuning range, power dissipation and phase noise analysis is performed. In Table 2 overall analysis is mentioned. Oscillating frequency, tuning range, phase noise and power dissipation is analyzed by varying the supply voltages. For a supply voltage of 1.5, frequency range is between 1.413 to 3.03 GHz, which corresponds to a tuning range of 53.46%. At a supply voltage of 2.0 oscillating frequency is 1.795 to 3.341GHz which gives a tuning range of 46.27%. Figure 3 shows the transient response of the VCO at 2.8GHz and Figure 4 shows the power analysis of VCO at different voltages.

<table>
<thead>
<tr>
<th>Vdd(volt)</th>
<th>1.5</th>
<th>2.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>( F_{osc} ) (GHz)</td>
<td>1.413 ~ 3.03</td>
<td>1.795 ~ 3.341</td>
</tr>
<tr>
<td>Tuning range(%)</td>
<td>53.46</td>
<td>46.27</td>
</tr>
<tr>
<td>Phase Noise</td>
<td>-156.32</td>
<td>-117.99</td>
</tr>
<tr>
<td>Power(mW)</td>
<td>9.02 ~ 10.20</td>
<td>21.04 ~ 23.96</td>
</tr>
</tbody>
</table>

![Figure 3 Transient response of VCRO at 2.8GHz.](image)

Figure 3 Transient response of VCRO at 2.8GHz.

![Figure 4 Power analysis for various supply voltages](image)

Figure 4 Power analysis for various supply voltages.

![Figure 5 Operating frequency for different voltages](image)

Figure 5 Operating frequency for different voltages.
IV. ANALYSIS OF RESULTS

The performance analysis of proposed VCRO is analyzed and is compared with the other papers with different design parameters and is presented in table 3.

The delay cell proposed can operate at a frequency of 2.8GHz for a supply voltage of 1.5 which is less compared to [1], [2]. The tuning range of this work is improved by 4.06% than other works in [1] and [2]. The gate length used in this work is 200nm compared to that of 400nm [1] and 600nm [2] respectively. Due to this the chip area gets reduced. The power consumption of this work is also less compared to [1] and [2].

Table.III Comparision of Results

<table>
<thead>
<tr>
<th>Design</th>
<th>[1]</th>
<th>[2]</th>
<th>Present work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.18µm</td>
<td>0.5µm</td>
<td>90nm</td>
</tr>
<tr>
<td>Output frequency (GHz)</td>
<td>0.737–1.456</td>
<td>0.660–1.270</td>
<td>1.413– 3.03</td>
</tr>
<tr>
<td>Tuning range(%)</td>
<td>49.4</td>
<td>48</td>
<td>53.40</td>
</tr>
<tr>
<td>Power Dissipation (mW)</td>
<td>14.8</td>
<td>15.5</td>
<td>9.02</td>
</tr>
<tr>
<td>Phase Noise</td>
<td>-103.3</td>
<td>-106</td>
<td>-156.328</td>
</tr>
<tr>
<td>Supply Voltage (Volt)</td>
<td>2.0</td>
<td>2.5</td>
<td>1.5</td>
</tr>
<tr>
<td>No.of stages</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>

The phase noise of the VCRO can be improved by cascading more number of stages with a trade off to power consumption and chip area. Four-stage ring oscillator with same topology is simulated using 90nm technology in CADENCE. A tuning range of 62.15% is achieved by the circuit. The power consumption of the circuit is increased to 16.45mW. The phase noise of the four stage ring oscillator circuit is -116.608 dBc/Hz.

V. CONCLUSION

A two-stage ring oscillator with a supply voltage of 1.5 and operating frequency of 2.8GHz is implemented in 90nm CMOS technology. The VCRO has a wide tuning range of 1.413 to 3.03GHz which corresponds to 53.40%. The ring oscillator used provides less power consumption of 9.02mW and a phase noise of -156.328. Furthermore four-stage ring oscillator is also simulated to obtain better phase noise and tuning range at the cost of power consumption.

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REFERENCE


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