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Efficient Timing Recovery Technique for Software Defined Radio Receiver using FPGA

Sabah SHehd Abdulabas

Abstract- This paper presents the timing recovery in software defined radio receiver as a widely used technique nowadays. Software defined radios (SDR) is the more configurable hardware platforms that provide the technology for realizing the fast growing third and new generation digital wireless communication structure. The more complex duty performed in a high data rate wireless system is the synchronization. The timing synchronization in SDRs using FPGA based signal processors is introduced. The 16-QAM loop for performing coherent demodulation were described and reported on the suggestion of FPGA automation. A matched filter control system is used to provide and addressed the symbol timing recovery technique. To explain the operations of the timing recovery loop and reflection, much approach is adopted and outlined for FPGA performance.

Keyword- Timing Recovery, SDR, FPGA

1. Introduction

The radio system has migrated to digital implementation in last few years. The migration of digital part in the receiver along the signal conditioning chain ever closer to antenna is the most important techniques in SDR. The high performance of digital communication systems is making a possibility to advance the semiconductor process technology which allowed the idea of system on chip to be real word. The hardware has to carry out the difficulty of coding, modulation, multiple access synchronization [1].

The main role in digital communication hardware is represented in Field programmable gate array (FPGA). Though, nowadays, the FPGA technology has been undergone radical change. The challenge duty in a communication system is the symbol timing recovery. To solve the timing recovery problems, large time is spent many hardware and software is developed to support the synchronization in SDR. [2] [3].

2. SDR Synchronization Technology

The synchronization will be defined as a process of align the frequency and phase of set of remote oscillators [4]. The conventional modulator and demodulator is illustrated in Figure 1.

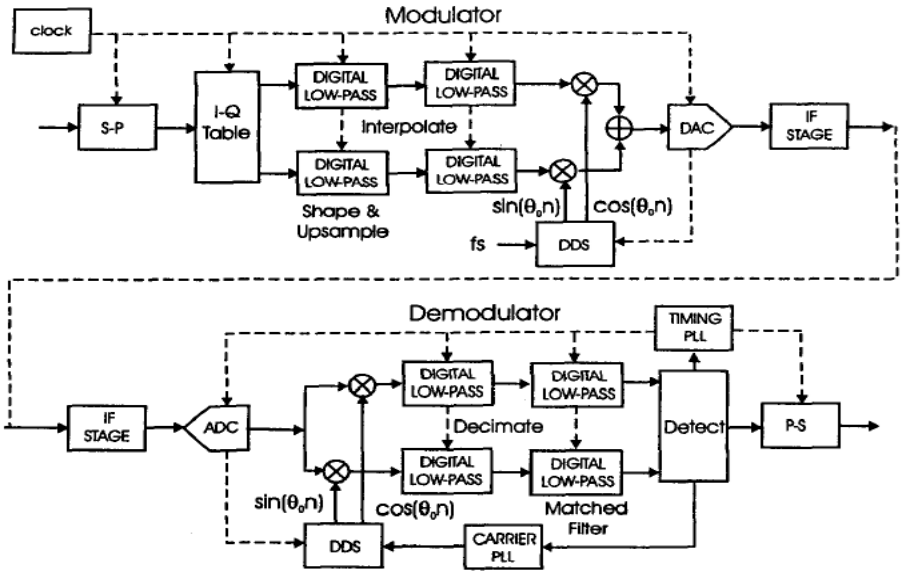

Figure 1: Communications Modulator and demodulator for QAM

Since the sine and cosine are orthogonal, so it's two independent carriers in the same frequency band. While, the cosine and sine waveforms are each assigned, the modulation is called 16-QAM. The waveform duration extends over many symbol durations. Though, the waveforms are overlapped and the modulated waveform is the sum of set of time shift [1].

The samples of the heterodyned signal are converted to a waveform by a digital to analog converter (DAC) and low pass filter and most often up converted again by additional analog processing. In the DSP based receiver the sampled signal is down converted from its digital carrier by samples of the sine and cosine carrier formed by the output of a local sine wave generator and then filtered by product-sums matched to the known transmitted wave shapes. The first task of forming a frequency and phase-matched replica of the local oscillator for the down conversion operation is called carrier acquisition.

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The second task of collecting a set of input samples time aligned with the replica template is called (symbol) timing recovery. The demodulator must perform a task not performed at the modulator; by mining clues embedded in the **re**ceived signal, it must replicate the carrier and symbol clocks associated with the signal in order to process the received signal. [5].

1. Timing Recovery Synchronization in FPGA Design

The modern approach in FPGA design under SDR technology is illustrated in Figure 2. The signals are sampled before the digital matched filter. Though, the timing recovery required feedback between the analogue and digital domains which complicate the overall designs [3].

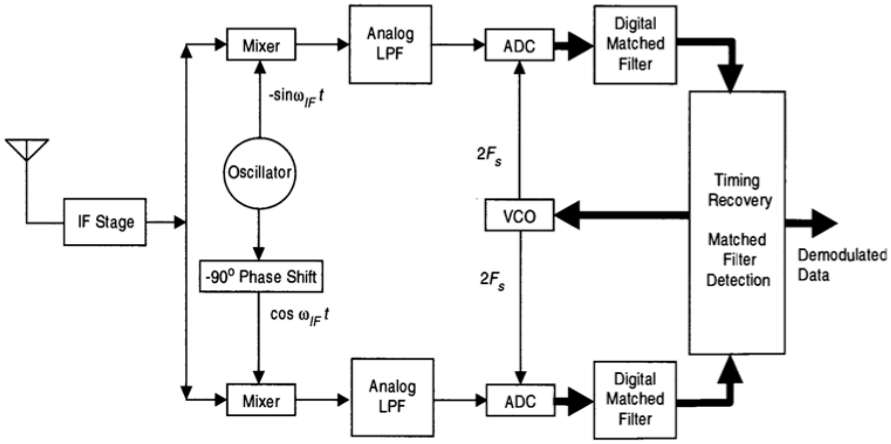

Figure 2: Timing Recovery in digital receiver

A multirate digital signal processing can be used to avoid the feedback with ADC. This approach state that the digitalized signal is interpolated by polyphase filter and sample point with maximum energy as show in Figure 3 [6].

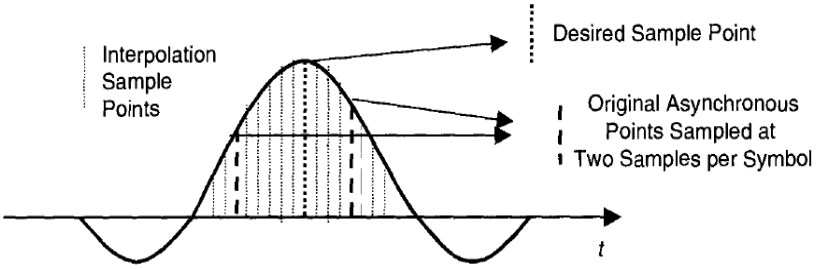

Figure 3. Interpolation of Nyquist pulse

The sampling process is performed at two samples per symbol and the polyphase matched filter interpolates the digitized signal to higher sampling rate. The right sample is chosen from the interpolated signal and the data stream is then down-sampled to sample rate by selecting the optimal point in the symbol. The objective of symbol synchronization is to sample the pulse at its peak value. This peak value can be determined by estimating the derivative of sampled signal. The early –late gate derivative measurement for the polyphase output at constant time can be computed from the output filter stage as show in Figure 4.

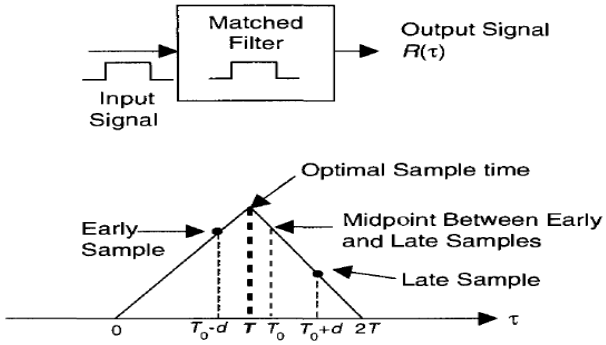

Figure 4: Matched filter process

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The decision here is the product of the number of polyphase filter stage and its derivative to decide the symbol value independently. Driving this product to zero by mean of a feedback loop leads to maximum likelihood timing recovery. The optimal timing is obtained when R(t) typically has a symmetric shape (neglecting distortion and noise). This case will happen when R(t) is sampled at t=T. However, the error signal to a timing recovery loop is equal to R(T+d) – R (T-d).

The DSP receiver that used polyphase filter for timing recovery is illustrated in Figure 5. There is no feedback between the digital and analog domains.

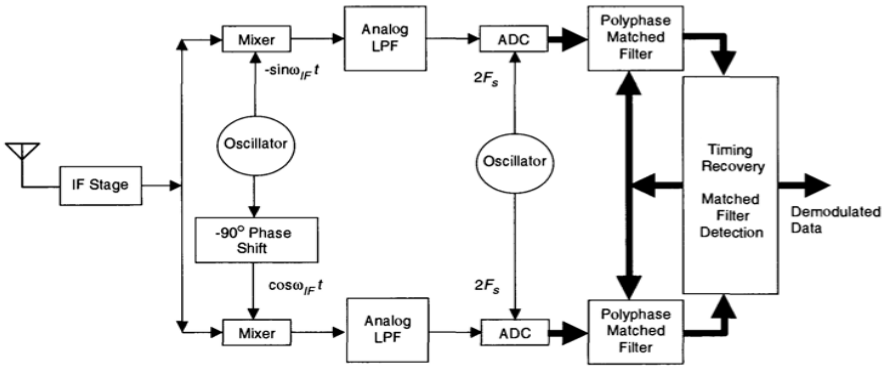

Figure 5. Multertae filter synchronization

The matched filter output used to decide the symbol decision at the end of every symbol time. This information could be used to decide which symbol is mainly likely to sent symbol. To make this decision, the detector should know when the symbols start and end. This technique called the timing synchronization in SDR system. The end of the symbol interval corresponds to the point in time where the eye diagram is the most open. To determine the optimum sampling point, one should find the point where the slope of the matched filter output is zero as illustrated in Figure 6. If the current timing estimate is too early, then the slope of the matched filter output is positive indicating that the timing phase should be advanced. If the current timing estimate is too late, then the slope of the matched filter output is negative indicating that the timing phase should be retarded. This method implements maximum likelihood timing synchronization. The second method uses the zero crossings in the matched filter output to estimate the times in between the optimum sampling points as shown in Figure 7. Zero crossings are found by searching for sign changes between matched filter outputs. Positive going zero crossings is added to an average while negative going zero crossings is subtracted [7-8].

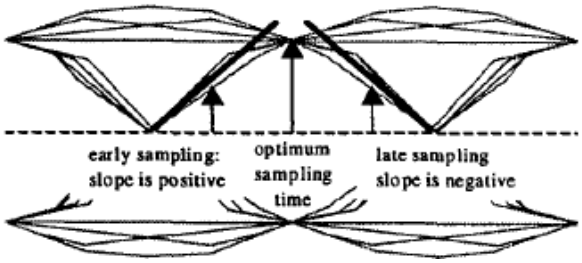

Figure 6: Maximum Likelihood estimation using the slope of the eye at the current estimate

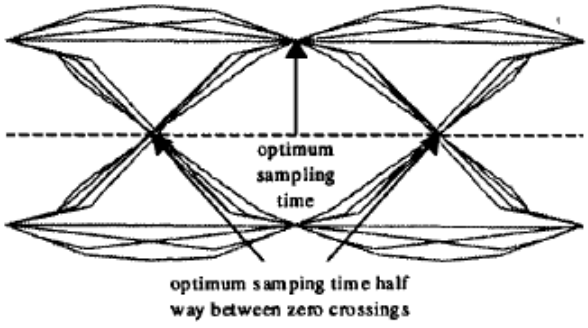

Figure 7: Zero-crossing detector

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4. 16 - QAM Transceiver Timing Recovery Design

This section focuses on the system level design using, DSP Design Tools. Based on the available resources from [9-10-11-12] a simple 16-QAM SDR transmitter and receiver model is designed for Virtex-4 FPGA architecture in Xilinx System Generator and MATLAB/SIMULINK environment. The GUI of the design is a model-based structure which uses the Xilinx specific block set as shown in Figure 8

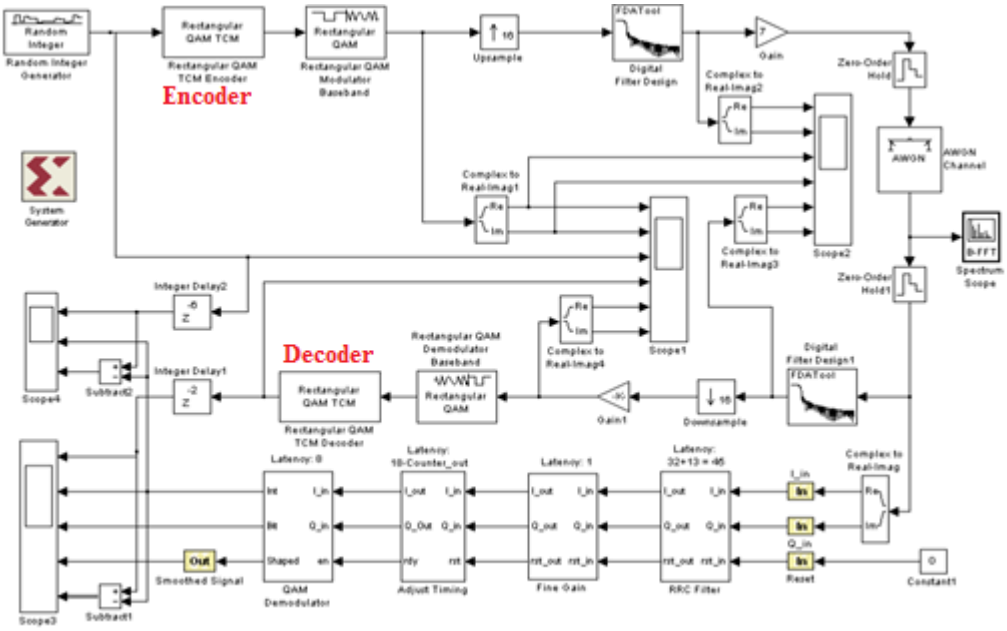

Figure 8: SDR Transceiver Design using System Generator

The receiver link accepts the IQ data streams from the AWGN channel and converts the data into fixed point format. First, noises existing in the received IQ signals are reduced by two identical RRC filters. Subsequently, the filtered signals are amplified to a specific level. The filtered and fine-gained IQ signals are down-sampled to convert them into IQ symbol pairs before demodulation. In the 16-QAM demodulation, the decision for the IQ symbol pairs is made using algorithms in *M Code* blocks. The symbol pairs are mapped back to 4-bit integer, subsequently translated back to bit stream through parallel-to-serial conversion.

An additional process of pulse shaping for the demodulated bit using normalized-gain raised cosine filter is incorporated for better visualization of DAC output via oscilloscope. The filter design parameters are: order = 16, over-sampling rate = 8, roll-off factor = 0.35, scale pass-band with Kaiser Window, and = 0.5. The demodulation is by far the mainly complicated part in the receiver because it must detect amplitude and phase of the signal correctly before the decision-making process. Thus, symbol synchronization is required before the demodulation. Figure 9 shows the 16-QAM receiver modeling in SDR technology.

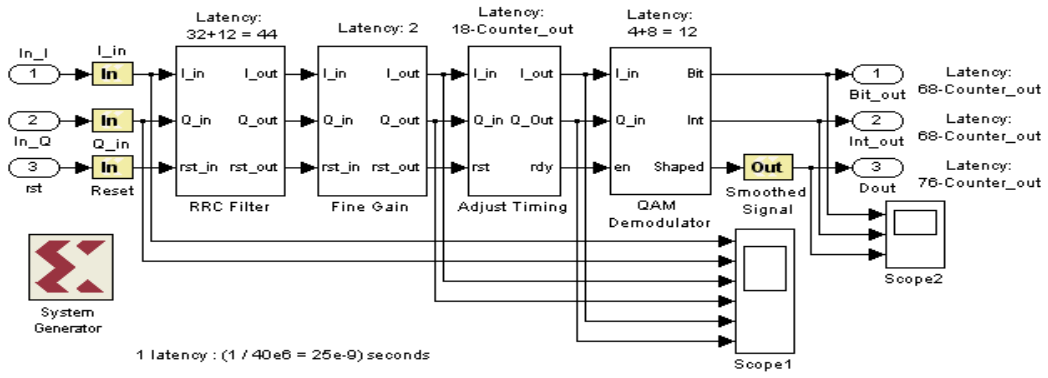

Figure 9: Receiver Link Modelling in SDR technology

Figures 10 and Figure 11 shows the input and output signals of the receiver model. The received IQ signals (40 Msps sample rate; 14 bits, 9th binary point) are filtered and fine-gained to become refined IQ signals (40 Msps sample rate; 16 bits, 14th binary point). The signals are subsequently synchronized and down-sampled by 16 to transform them into baseband IQ symbols (2.5 Mega-baud).

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After demodulation, the recovered 4-bit integers (2.5 Mega-baud) are converted to recovered bit stream (10 Mbps bit rate), and then transformed as smoothed signal (80 Msps sample rate; 16 bits, 13th binary point).

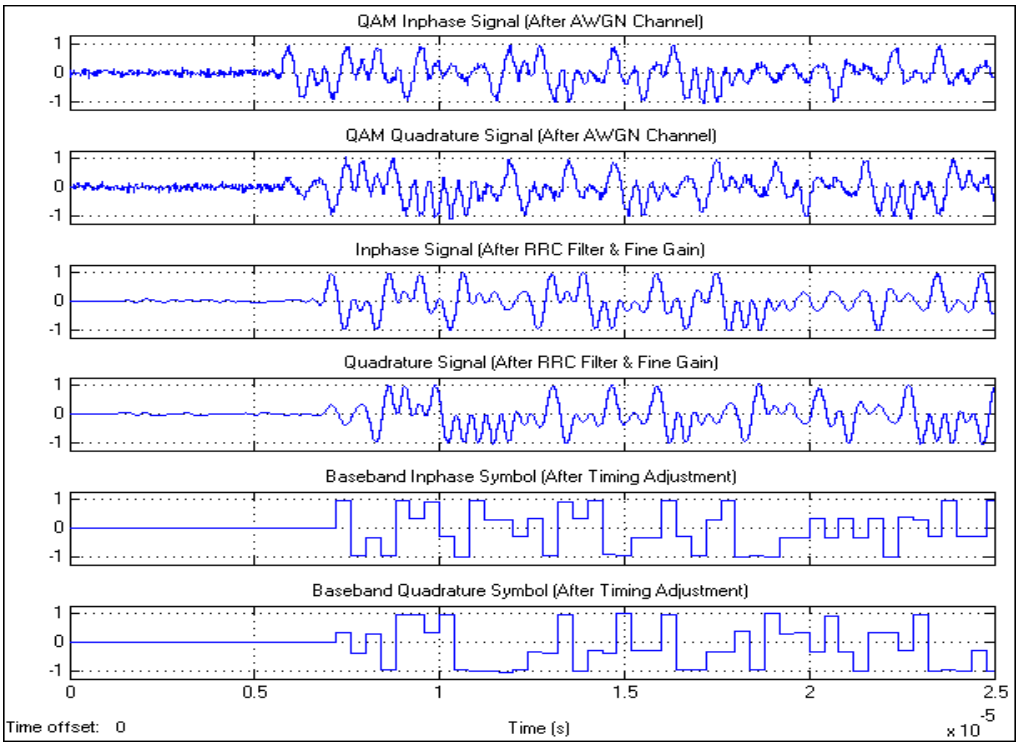

Figure 10: Receiver Signals: Received (IQ) signal: 40 Msps (14 bit, 9 fractional length); Filtered and fine-gained (IQ) signal: 40 Msps (16 bit, 14 fractional length); Baseband (IQ) symbol: 40/16 = 2.5 Mega-baud.

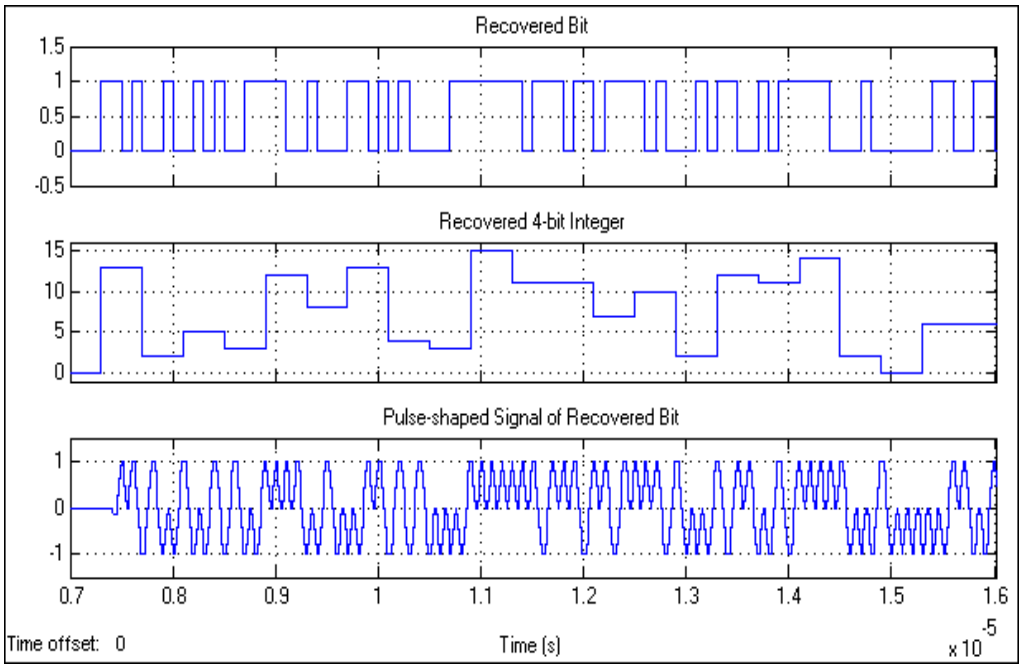

Figure 11: Receiver Output Signals: Recovered 4-bit integer: 2.5 Mega-baud; Recovered bit: 2.5×4 = 10 Mbps; Pulse-shaped signal of Recovered bit: 10×8 = 80 Msps (16 bit, 13 fractional length)

4.1 Input and Output Signals Timing Synchronization

The timing synchronization technique used in the proposed model is defined by the decision making in the matched filter output to estimate the times in the optimum sampling points. In this technique, the threshold level has been limited by three values (0.667, 0.333, and 0.125) that represent the tolerance range in the QAM (I/Q) channels.

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The technique of the decision making for the 16-QAM scheme is shown in Figure 12. In this technique, if the symbol magnitude is less than the decision making consider it as a noise and then neglected, and if the symbol magnitude greater than and less than , the decision making consider it as 1/3 QAM signal. If the symbol magnitude is found greater than , the decision making consider these values as 1 QAM signal. Figure 13 shows the input and output signals of the proposed SDR model. The difference between the original and the recovered message bits is zero, and the difference between the original and the recovered symbol integers is also zero. This indicates that the timing synchronization between the transmitter and the receiver is optimized and the symbol remapping removes the noise caused by AWGN using the tolerance range of threshold in decision-making technique. In this technique, the threshold level is limited by three values (0.667, 0.333, and 0.125) that represent the tolerance range in I and Q channels.

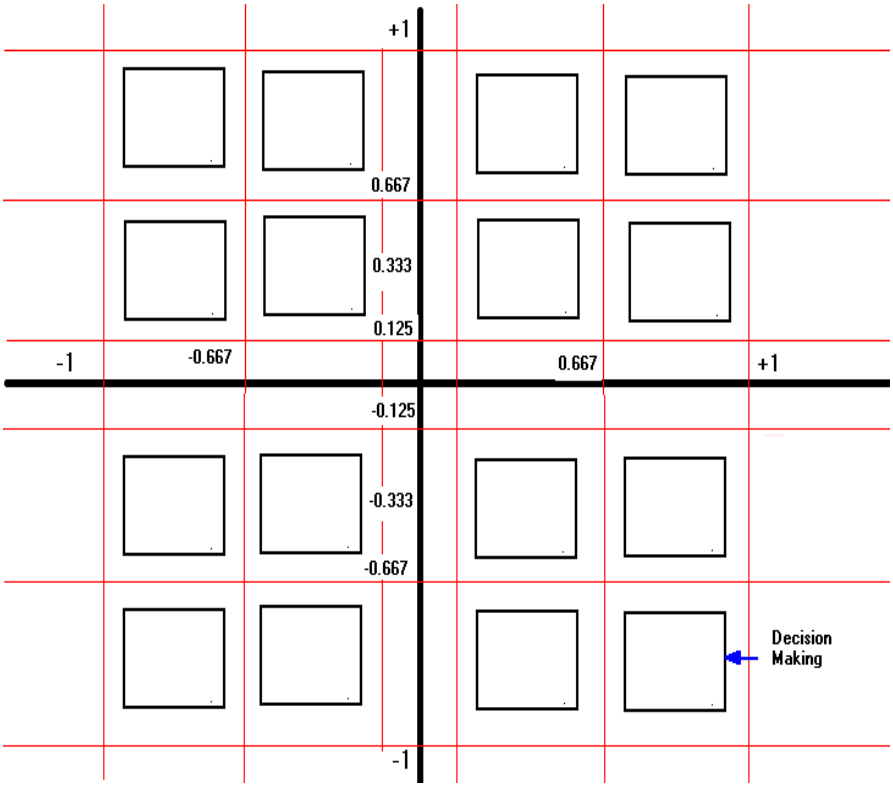

Figure 12: Tolerance highest peak search decision making technique

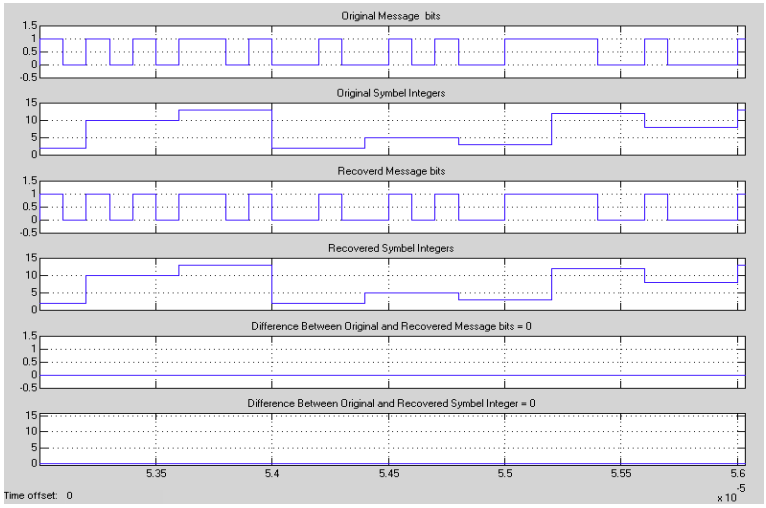

Figure 13: Input and output signal of proposed software defined radio

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The maximum likelihood timing synchronizer techniques using system generator is illustrated in Figure 14 and the output of each stage show in Figure 15.

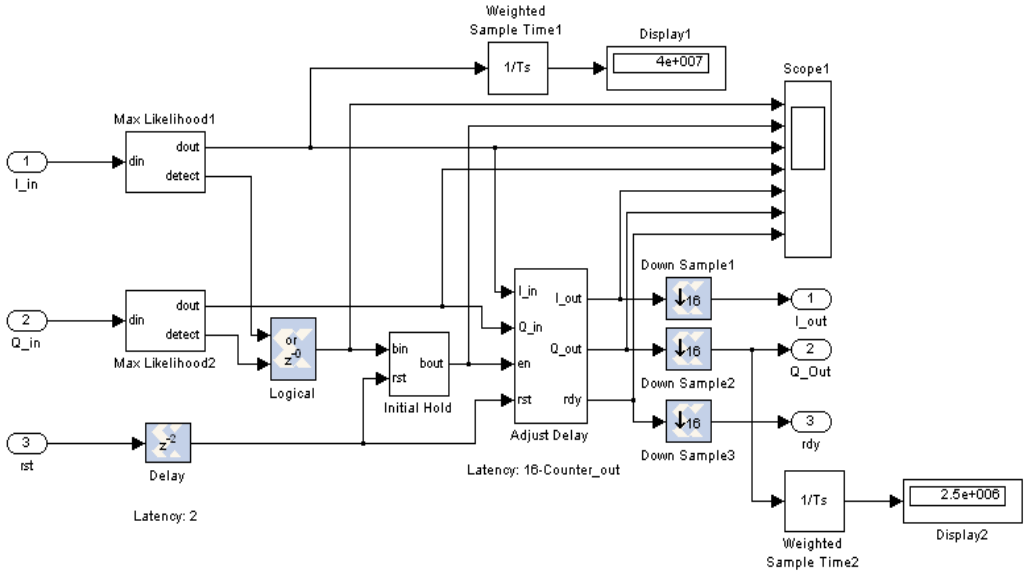

Figure 14: The maximum likelihood symbol timing estimator using System Generator

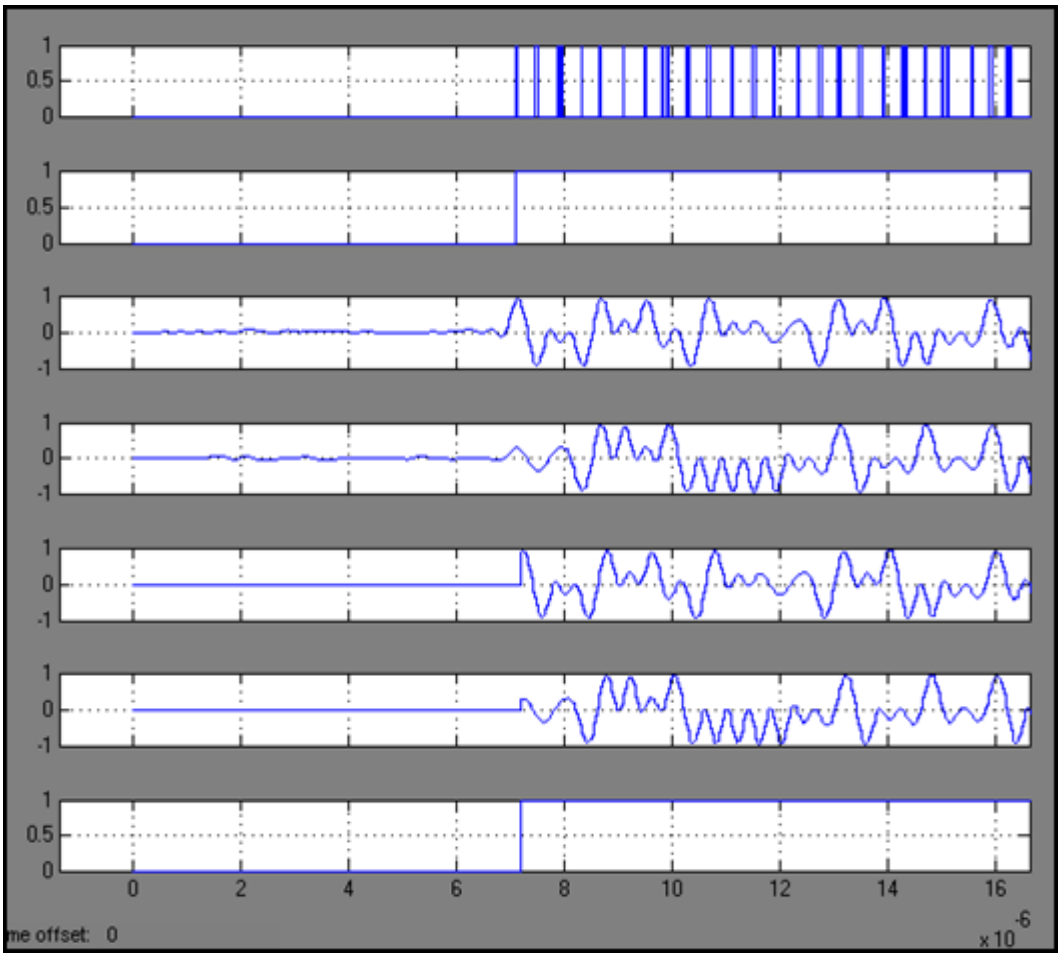

Figure 15: Output waveform of timing estimator

The nonappearance of error and warning from DRC and bit-stream generation process, the configuration bit-stream file is downloaded to Virtex-4 FPGA board. The input and output waveforms are experienced in the natural composite of the transmitter and receiver, as shown in Figure 16. It should be noted that the empirical (real-time) result is identical to the simulated result.

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The ADC input and DAC output signals in P240 Analog Module for the SDR transmitter and receiver are connected to oscilloscope in order to display real-time result. Transmitted I/Q and received I/Q signals should be similar, although noise effect and distortion may occur (real-world application issue). After the simulation of all SDR system (Transmitter and Receiver) was running correctly, the resulting response of each paths give equivalent shapes as shown in Figure 17.

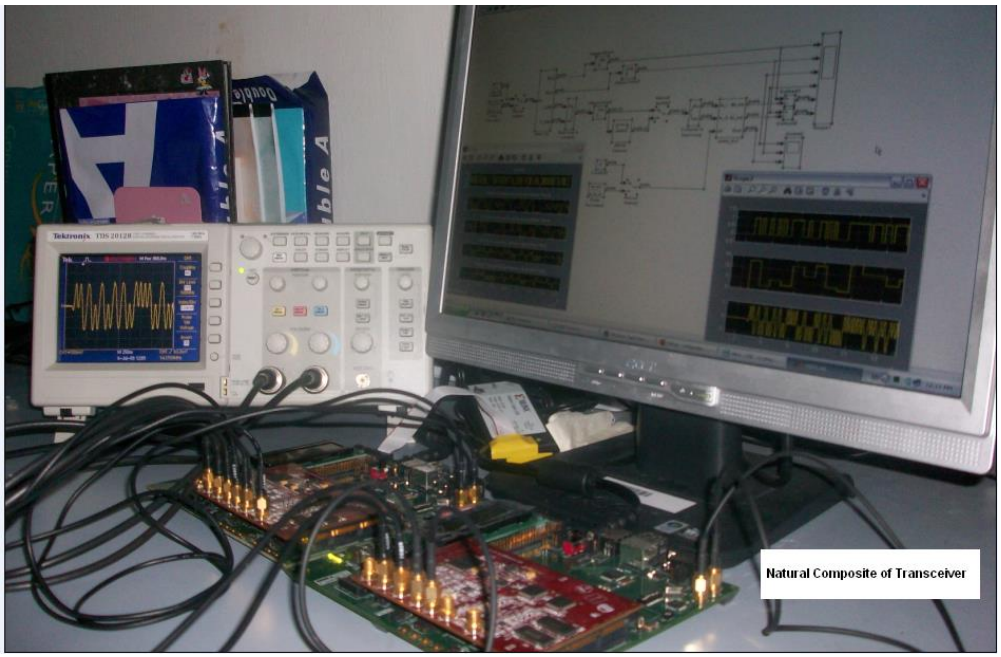
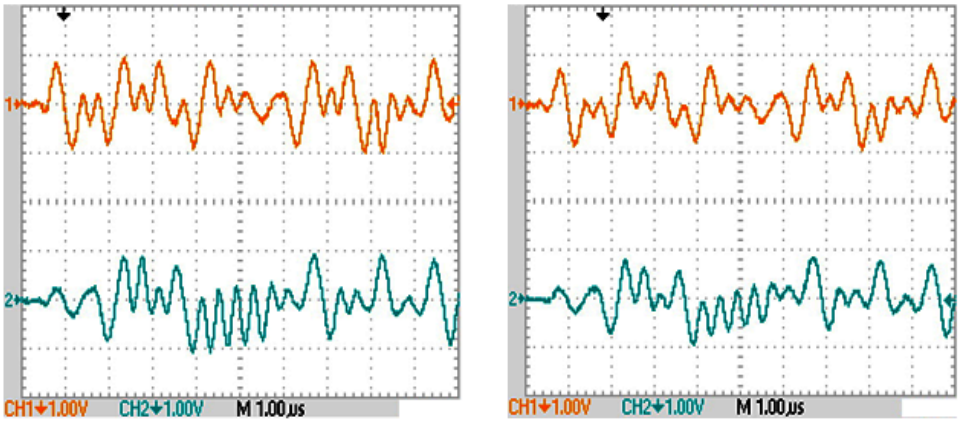


Figure 16: Natural Composite of Transceiver



(a) Transmitted (IQ) (b) Received (IQ)

Figure 17: Transmitted/Received (IQ) 16-QAM Signals

5. Conclusion

This paper has provided an overview of how timing synchronization can be implemented in an FPGA. While the 16-QAM loop and differential matched filter servo loops described in the paper form the key components of a QAM modulation system, a number of additions and refinements are required to produce a complete system. The waveform characteristics of the receiver were compared with the transmitter waveforms such as pulse interval (ns) and lower/higher amplitude peak. The pulse interval of receivers signal is 100 ns and the pulse interval of the transmitters signal is likewise 100 ns. This means that no error difference is found between them. The timing error is satisfied because of accurate timing adjustment, whereas errors of 5% are found between the amplitude of each signal because wiring, chip, and printed circuit board (PCB). However, the errors are acceptable. The simulated results for transmitted signal and receiver output in the time domain show equivalence in shape as show in Figure 16.

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References

[1] Chris Dick, fred harris and Michael Rice, "Synchronization in Software Radios - Carrier and Timing Recovery Using FPGAs", IEEE, 2000, PP.195-204

[2] H. Meyr, M. Moeneclaey and S. **A.** Fechtal, Digital Communication Receivers, John Wiley & Sons Inc., New York, 1998.

[3]B. Sklar, Digital Communications Fundamentals and Applications, Prentice Hall, Englewood Cliffs, New Jersey, 1988.

[4] D. R. Brown III and H. Poor, "Time-slotted round-trip carrier synchronization for distributed beamforming," IEEE Transactions on Signal Processing, 2008

[5] D. R. Brown III, G. B. Prince, and J. A. McNeill, "A method for carrier frequency and phase synchronization of two autonomous cooperative transmitters," IEEE 6th Workshop on Signal Processing Advances in Wireless Communication, 2005

[6] Chan, Tsui, Yeung, and Yuk," Design and Complexity Optimization of a New Digital IF for Software Radio Receivers With Prescribed Output Accuracy" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 54, NO. 2, pp 351-366, 2007

[7] Durke (2009), "Field Programmable Gate Array Based SDR Design" phd. Thesis, Naval postgraduate school, Department of Electrical and Computer Engineering,California:http://edocs.nps.edu/npspubs/scholarly/theses/2009

[8] Ezra, Joseph and kahn, "Carrier Synchronization for 3-bita and 4-bits per symbol optical transmission", IEEE, Journal of light wave technology, Vol.23, pp.4110-4124, 2005

[9] Jeffry H. Reed, "Software Radio a modern approach to radio engineering", Prentice Hall PTR, A division of person education Inc, ISBN 0-13-081158-0, pp.33-123, 2002

[10] Pedro and Nuno, "Multi-Mode Receiver for Software Defined Radio", Institute of Telecommunication – University of Aveiro – Portugal, online available: http://www.anacom.pt/render.jsp?contentId=761239, 2008

[11] Tony, "RF and Digital Signal Processing for Software-Defined Radio", Elsevier, ISBN 978-0-7506-8210-7, UK, pp. 319, 2009

[12] Proakis, and Salehi,. "Digital Communications", 5th ed., New York, NY: McGraw-Hill, Ch. 3, pp. 95-148, 2008