International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-3 Issue-4, April 2014

Leakage Power Optimization for VLSI Circuits @90nm CMOS Process

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Abstract – In Integrated Circuits (IC), the transistor density is increased by scaling down the size of MOSFETs. Scaling down of devices sizes for improving the performance has lead to a substantial increase in the subthreshold leakage current. In this paper, a new method is proposed to reduce leakage power in standby mode of operation. This proposed method combines Input Vector Control (IVC) and Gate Replacement (GR) techniques. The proposed method is validated by applying to three different benchmark circuits at 90nm CMOS process technology using HSPICE. The final results obtained are compared with other well known leakage reduction techniques and the proposed method proves to be more effective than other existing techniques.

Key words – leakage reduction, HSPICE, CMOS, full adder, PDP

I. INTRODUCTION

In CMOS circuits, there are three types of power dissipations namely, dynamic power, short circuit power and leakage power. Among these, dynamic power was the major component [1-2]. Nowadays, scaling down of voltage has resulted in reduction of dynamic power dissipation. According to International Technology Roadmap for Semiconductors (ITRS), the subthreshold current is becoming dominant in CMOS circuits with the scaling down of process technology. Literature contains many techniques to reduce leakage power either in standby mode alone or active and standby modes together. The leakage power is prominent in standby mode so the proposed method is targeted to reduce it. The rest of the paper is organized as follows. Section 2 explains some of the existing leakage reduction techniques. Section 3 explains the proposed method to reduce the leakage power. Section 4 contains the simulation results for the proposed method.

Manuscript published on 30 April 2014.
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II. EXISTING LEAKAGE REDUCTION TECHNIQUES

In Input Vector Control (IVC), the Minimum Leakage Input Vector (MLV) for a given circuit is found using a search based algorithm.
This MLV is applied to the circuit during standby mode to reduce the leakage power [3-4]. In stack method, every transistor of width W is replaced by two transistors, of width W/2, in series. This increases the effective resistance of the circuit which reduces the leakage power [5]. In LECTOR, two Leakage Control Transistors (LCTs) are placed between the pull up and pull down networks in a specific configuration. Each LCT is driven by the source of the other LCT.
This ensures that one of the LCTs is always near cut off region hence reducing the leakage power [6]. The proposed method is one such technique that combines IVC and Gate Replacement [7-9] which is discussed in section 3.

III. PROPOSED METHOD

The leakage current depends on various factors. Leakage current is a function of input vector pattern applied to the circuit. In the proposed method, the MLV which corresponds to the total minimum leakage power is identified and injected to the circuit during the standby mode of operation. Table 1 and 2 gives the power profile for 2 input NAND and 3 input NAND gates that are obtained at 90nm process technology at VDD = 1V.

TABLE 1

Leakage and average power of 2 input NAND

Input	Leakage (nW)	Average power (W)
00	4.20	4.2e-9
01	39.26	4.35e-8
10	21.97	2.19e-8
11	109.79	1.18e-7

TABLE 2
Leakage and average power of 3 input NAND

Input	Leakage (nW)	Average power (W)
000	2.74	2.74e-9
001	4.23	8.52e-9
010	2.27	4.57e-9
011	39.26	4.78e-8
100	3.38	3.38e-9
101	21.96	2.62e-8
110	20.57	2.05e-8
111	247.23	2.6e-7

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From table 1 and 2, the input vectors 00 and 000 are identified as the Minimum Leakage Vector (MLV) for 2 and 3 input NAND gates respectively.

The sequence of steps followed in the proposed method is given as follows:

1) Convert the given CMOS circuit into NAND - NAND based circuit.
2) Find the MLV for the NAND – NAND based circuit obtained in step 1.
3) Obtain MLV for 2 input NAND, 3 input NAND and 4 input NAND gates depending on the requirement for NAND – NAND circuit obtained in step 1.
4) Apply the MLV generated from step 2 to the circuit under consideration during standby mode.
5) Identify the gates which are in its worst leakage state and replace them with a higher order gate with the additional input as sleep signal.

Fig. 1 shows the full adder circuit with MLV 000 applied to the primary inputs. The gate G4 is in its worst leakage state with leakage power of 109.8nW. This gate is replaced by G4* with sleep signal as the third input (as shown in fig. 2). During standby mode of operation the sleep =0 and during active mode of operation sleep=1. This ensures that the circuit functionality is unaltered during active mode of operation. Replacement of gate G4 by G4* and insertion of sleep signal with sleep=0 alters the output of gate G4 and subsequently alters the output of other gates. These subsequent changes force gate G7 gate to its worst leakage state. Similar procedure of gate replacement is followed for the gates G7, G8 and G9 (Gates in worst leakage state) to reduce the overall leakage during standby mode of operation. During active mode sleep=1, so that the original functionality is not altered. Fig. 2 shows the full adder circuit after replacing the gates which are in worst leakage states.

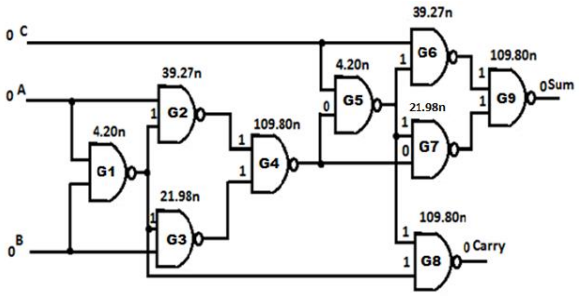

Fig. 1 Full adder showing leakage power (nW) of different gates when MLV is applied

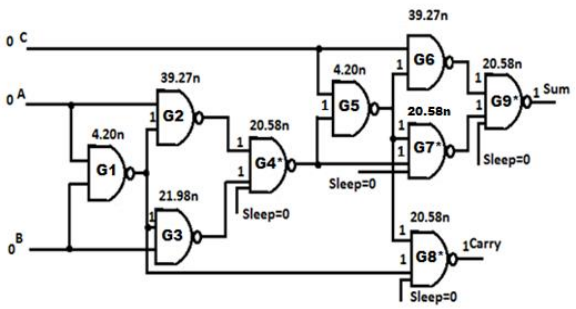

Fig. 2 Modified full adder with 4 gates replaced and input and sleep signal values during standby mode

IV. SIMULATION RESULTS AND DISCUSSION

The proposed technique is evaluated by applying it to three different benchmark circuits namely Full adder, C17 and 4X1 MUX. Wide range of experiments was conducted to measure the power and delay for the circuits under consideration. The simulation was done using HSPICE with a CMOS process technology of 90nm. The length is uniformly taken as 90nm and the width of PMOS (Wp) and NMOS (Wn) are taken as 3 µm and 1.5µm respectively for all the transistors. All devices were of standard threshold values and simulated at room temperature of 27°C.

The Minimum Leakage Vector (MLV) for the three benchmark circuits that are discussed in section 2 namely, full adder, C17 and 4X1 MUX are obtained from the table 3, 4 and 5. Fig. 3 shows the input – output values of a full adder circuit with proposed technique during active mode. The proposed method is compared with the other well known leakage reduction methods such as Input Vector Control (IVC), Stack method and LECTOR method and the results are tabulated in table 6.

TABLE 3
Power and delay profile of a 1- bit full adder

90nm process technology at VDD = 1V			
Input	**Leakage power (nW)**	**Average power (W)**	**Average delay (ns)**
000(MLV)	451.63	4.51e-7	0.97
001	504.07	5.12e-7	
010	500.22	5.09e-7	
011	556.47	5.73e-7	
100	504.53	5.09e-7	
101	560.78	5.73e-7	
110	495.49	5.13e-7	
111	547.92	5.74e-7	

TABLE 4
Power and delay profile of a C17 (random inputs only shown)

90nm process technology at VDD = 1 V			
Input	**Leakage power (nW)**	**Average power (W)**	**Average delay (ns)**
00000	289.23	2.89e-7	0.97
00010(MLV)	210.1	2.14e-7	
00100	324.29	3.28e-7	
01000	342.09	3.46e-7	
01010	262.95	2.72e-7	
01101	422.44	4.46e-7	
10000	307.01	3.07e-7	
11001	333.47	3.46e-7	
11111	460.28	4.86e-7	

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TABLE 5
Power and delay profile of a 4X1 MUX (random inputs only shown)

90nm process technology at VDD = 1V			
Input	**Leakage power (nW)**	**Average power (W)**	**Average delay (ps)**
000000	528.89	5.29e-7	50.4
100000(MLV)	332.41	3.37e-7	
101000	348.42	3.53e-7	
001001	402.06	4.23e-7	
110001	642.59	6.6e-7	
010010	409.76	4.3e-7	
111110	446.48	4.64e-7	
000111	496.06	5.33e-7	
111111	532.8	5.67e-7	

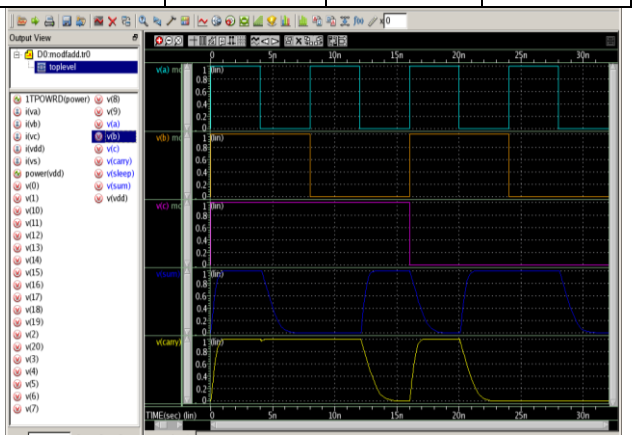

Fig. 3 The input and output waveforms of full adder circuit with the proposed technique during active mode with sleep signal =1

TABLE 6
Comparison results of proposed technique with other techniques for a full adder circuit for 90nm process technology

	Base case	Input vector	Stack	LECTOR	Proposed method
Leakage power (µW)	0.52	0.45	0.05	0.45	0.17
Average power (µW)	0.52	0.45	0.06	0.46	0.17
Delay (ns)	0.97	0.97	3.77	42.35	1.05
Leakage savings (in %)	-	12.2	91	11.8	66.2
Delay overhead (in %)	-	0	74.3	97.7	7.6
Static Power Delay Product (PDP)	0.50	0.44	0.19	19.05	0.18

From table 6, the following can be inferred.

- ✓ Row 2 reveals that the stack method is very effective in reducing the leakage power compared to IVC and LECTOR.
- ✓ From row 3, it is evident that the average power is less in stack method in comparison to base case.
- ✓ Row 4 shows that base case and IVC are having minimum delay and LECTOR is having the largest delay.
- ✓ In row 5 it is seen that the stack method is having the large leakage saving percentage followed by the proposed method with 66.2%.
- ✓ Row 6 it is inferred that the LECTOR is having the highest delay overhead followed by stack.
- ✓ Row 7 shows that the proposed method is having the optimum static PDP which is the desired feature for low power high speed circuits.

Thus, the proposed method is giving a reasonable leakage power saving and reduced delay overhead compared to other methods.

VI. CONCLUSION

In conclusion, this paper presents the collective features of IVC and GR methods in effectively reducing the leakage power during standby mode of operation. The proposed method resumes to the original circuit functionality during active mode of operation with sleep=1. According to HSPICE simulation at 90nm CMOS process technology at room temperature and under given conditions, the proposed method provides an optimum leakage saving and minimal delay overhead which makes it suitable for high speed applications. The proposed method can be extended to circuits of high logic depth in which the effect of this method is more pronounced.

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