International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-3 Issue-3, February 2014

Physical Design Implementation of Processor Torpedo at Different OCV Scenarios -40, 25, 125 Degree Celsius of an ASIC Design Chip

Tauseef Amin Azmi

Abstract— ***This Paper basically studies the physical design implementation of torpedo processor which incorporates 32 macros in overall and 43000 cell instances .We had 5 clocks ,3 propagated and 2 generated clock in a die size of 5.9 mm square which operated at a frequency of 400 megahertz having a supply voltage of 1.8 volts .The technology which we worked was 180 nm technology and working on the IC Compiler tool from synopsys and then moving on to static timing analysis part on the Prime time tool from synopsys and then further moving on to drc/lvs checking on the tool Calibre from mentor graphics.***

The foundry which supplied us the 180 nm technology documents was Jazz semiconductors INC.The earlier work on this project that were carried out were at different scenarios and hence the results were with different optimization ,here in our study we had made a comprehensive and mature step to achieve the maximum optimization of the placement of the standard cells and therefore in our effort we had chosen the three scenarios for our thesis which were three operating conditions :function minimum, function maximum , CTS maximum.

The temperature that we worked on the physical design implementation of this block level subsystem were -40 degree celcius , 25 degree celcius ,125 degree celcius. The three scenarios supply voltages were 1.65 volts ,1.8 volts and 1.9 volts respectively and the power dissipation was 300 milliwatts with a pre cts derate of 15 % and post cts derate of also 15% respectively.

The thesis was not so easy to carry out as we had several problems occurring at every step like the IR DROP was exceeding the limit which was provided as 5% of the total VDD+VSS supposed to be within 90 mv also errors from routing congestion and DRC errors were prompt.

Keywords— ASIC Design, OCV,VLSI,Physical design,Scenarios.

I. INTRODUCTION

This document is a template. An electronic copy can be downloaded from the conference website. For questions on paper guidelines, please contact the conference publications committee as indicated on the conference website. Information about final paper submission is available from the conference website. The thesis here is a study on the ASIC flow and we worked on the physical design aspect of the flow and hence a comprehensive work on the physical designing of the subsystem torpedo. This thesis basically studies the physical design implementation of torpedo processor which incorporates 32 macros in overall and 43000 cell instances .We had 5 clocks ,3 propagated and 2 generated clock in a die size of 5.9 mm square which operated at a frequency of 400 megahertz having a supply voltage of 1.8 volts.

Manuscript published on 28 February 2014.
***** Correspondence Author (s)
Tauseef Amin Azmi. VLSI Research Academy, RV-VLSI Design Centre Jayanagar 4th block Bangalore,Karnataka,India.

The technology which we worked was 180 nm technology and working on the IC Compiler tool from synopsys and then moving on to static timing analysis part on the Prime time tool from synopsys and then further moving on to drc/lvs checking on the tool Calibre from mentor graphics.
The foundry which supplied us the 180 nm technology documents was Jazz semiconductors INC.The earlier work on this project that were carried out were at different scenarios and hence the results were with different optimization ,here in our study we had made a comprehensive and mature step to achieve the maximum optimization of the placement of the standard cells and therefore in our effort we had chosen the three scenarios for our thesis which were three operating conditions :function minimum, function maximum , CTS maximum.
The temperature that we worked on the physical design implementation of this block level subsystem were -40 degree celcius , 25 degree celcius ,125 degree celcius. The three scenarios supply voltages were 1.65 volts ,1.8 volts and 1.9 volts respectively and the power dissipation was 300 milliwatts with a pre cts derate of 15 % and post cts derate of also 15% respectively. The thesis was not so easy to carry out as we had several problems occurring at every step like the IR DROP was exceeding the limit which was provided as 5% of the total VDD+VSS supposed to be within 90 mv also errors from routing congestion and DRC errors were prompt.

II. EDA TOOL DESCRIPTION

An The IC Compiler is a part of the tools from synopsys galaxy platform extensively used in the VLSI industry for physical design implementation of the chip at the tape out stage of the ASIC flow. It is implementation platform which delivers a comprehensive design solution, it includes synthesis, physical implementation, low power design and design for manufacturability. IC Compiler can be said to be a single convergent, chip level physical implementation tool that has flat and hierarchical design planning, placement and optimization, clock tree synthesis, routing, manufacture and also low power capabilities which enable designers to put today's high end performance, complex design on schedule.
IC Compiler can be said to be a comprehensive place and route system ,the quality of reports(QOR) is best in according with the timing ,area ,power ,signal integrity , routability . It helps in faster design closure as well. Multicore support through out our working environment delivers improved yield. In the coming years growing design complexity , ever increasing DRC rules and complex manufacturing compliance needs have complicated the design of the chip on the sup optimal scale.

In design technology has been made possible by the integration of IC validator , DRC/LVS sign off solution and IC Compiler allows designers to migrate these problems in implementing steps for faster sign off and design closure
IC Compiler helps a lot in maintaining the signal integrity of the the wires here in by providing spacing with minimizing the cross talks erupting in the work systems for longer signal propagation.

THE QUALITY OF REPORTS: ANALYZING REPORTS GENERATED.

The new technologies which are innovative are peer innovative technologies in IC Compiler delivers QOR improved quality of work ,measures in terms of the complete cost vector ,timing area , power ,signal integrity , routabilty and manufacturability.
The flow involves Multi corner Multi mode optimization which includes enhanced signal integrity capabilities. Multisource clock tree synthesis nad physical data path technology enable designers to meet aggressive OQR targets. QOR is generally generated after each timing report generation. “Physical Datapath” technology allows designers to create structures by specifying constraints for the relative column and row positions of instances. These structures are called relative placement (RP) structures. Figure 2 .4 highlights some of the benefits of relative placement (RP).

TABLE I
TIMING REPORT GENERATED AFTER 5 ITERARTIONS.

No . of itera tions	Quality of reports for design timings: Scenario function maximum and minimum		
	Critical path length for the design constraints under the timing closure	Critical path slack, total negative slack, no of violating paths	No of hold violations
1	2.81	-1.91,-43.71,150	0
2	1.73	-2.92,-60.84,25	0
3	2.71	-0.26, 10.00.26	0
4	2.90	-2.36,-2053.7,4372.00	0
5	1.50	-1.34,-76.38,147.0	0

Scenario 'func_min', func max
Timing Path Group 'REGOUT'

Levels of Logic: 0.00
Critical Path Length: 0.00
Critical Path Slack: 0.00
Critical Path Clk Period: n/a
Total Negative Slack: 0.00
No. of Violating Paths: 0.00
Worst Hold Violation: 0.00
Total Hold Violation: 0.00
No. of Hold Violations: 0.00

Scenario 'func_min'
Timing Path Group 'scan_clk'

Levels of Logic: 0.00
Critical Path Length: 0.00
Critical Path Slack: 0.00
Critical Path Clk Period: n/a
Total Negative Slack: 0.00
No. of Violating Paths: 0.00
Worst Hold Violation: -0.47
Total Hold Violation: -119.53
No. of Hold Violations: 868.00

Scenario 'func_min'
Timing Path Group 'sys_clk'

Levels of Logic: 0.00
Critical Path Length: 0.00
Critical Path Slack: 0.00
Critical Path Clk Period: n/a
Total Negative Slack: 0.00
No. of Violating Paths: 0.00
Worst Hold Violation: -0.45
Total Hold Violation: -68.52
No. of Hold Violations: 737.00

Scenario 'func_min'
Timing Path Group 'sys_rclk'

Levels of Logic: 0.00
Critical Path Length: 0.00
Critical Path Slack: 0.00
Critical Path Clk Period: n/a
Total Negative Slack: 0.00
No. of Violating Paths: 0.00
Worst Hold Violation: -0.02
Total Hold Violation: -0.15
No. of Hold Violations: 15.00

Scenario 'func_min'
Timing Path Group 'uart_clk'

Levels of Logic: 0.00
Critical Path Length: 0.00
Critical Path Slack: 0.00
Critical Path Clk Period: n/a
Total Negative Slack: 0.00
No. of Violating Paths: 0.00
Worst Hold Violation: -12.12
Total Hold Violation: -48.41
No. of Hold Violations: 4.00

Cell Count

Hierarchical Cell Count: 1088
Hierarchical Port Count: 33172
Leaf Cell Count: 70731
Buf/Inv Cell Count: 33108
CT Buf/Inv Cell Count: 1548
Combinational Cell Count: 55008
Sequential Cell Count: 15723
Macro Count: 32

Area

Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)

Combinational Area: 1053031.803151
Noncombinational Area:
4643411.86
Buf/Inv Area: 621970.278129
Net Area: 0.000000
Net XLength : 2326021.50
Net YLength : 2441038.50

Cell Area: 5696443.667407
Design Area: 5696443.667407
Net Length : 4767060.00

Design Rules

Total Number of Nets: 72828
Nets With Violations: 851
Max Trans Violations: 851
Max Cap Violations: 0

Hostname: yamuna

Compile CPU Statistics

Resource Sharing: 0.00
Logic Optimization: 0.00
Mapping Optimization: 5126.07

Overall Compile Time: 5136.67
Overall Compile Wall Clock Time: 4853.12

Scenario: func_max WNS: 2.91 TNS: 2230.01 Paths: 4729
Scenario: func_min WNS: 0.00 TNS: 0.00 Number of Violations: 0
Design WNS: 2.91 TNS: 2230.01
Number of Violating Paths: 4729

III. CONCLUSIONS

The G cells that are generated after the global routing and the track assignment produced us the following reports and inferences to draw after several iterations and then the final tracking of the cells in the core area and hence finalizing the report of our work here in the inferences.
Thus we conclude here that in the coming future these ASICS can be implemented in different scenarios keeping in accordance with the temperature, volumes of the design we were working on . Hence the max temperature can be varied in between 125 degree Celsius to 130 degree for the future works to be carried out .

ACKNOWLEDGMENT

At the outset, we thank the Almighty for making our endeavor a success. We also express our gratitude to our guide **Rekha Agrawal (Assistant Professor),** Department of Electronics & Communication Engineering, Suresh Gyan Vihar University, Jaipur for providing us with adequate facilities, ways and means by which we were able to complete this seminar. This work was also possible because of the able leadership of **Naveen Hemrajani (Vice – Principal), Rashid Hussain (Head of Department), and Sandhya Sharma (Associate Professor),** Department of Electronics & Communication Engineering, Suresh Gyan Vihar University, Jaipur.
It is also my pleasure and privilege to acknowledge and express my deep sense of gratitude to my teacher **Rekha Agrawal**, Department of Electronics & Communication Engineering, Faculty of Engineering, Suresh Gyan Vihar University, Jaipur, who inspired and initiated me to prepare this seminar despite her busy academic schedule. She has always been kind enough to spare her valuable time and thought in giving necessary guidance. Her reach and varied experience as an academician immensely helped me in understanding this topic clearly.
I express my immense pleasure and thank all the teachers and staff of the Department of Electronics & Communication Engineering, SGVU for their cooperation and support. Last but not the least, I thank all others, and especially our classmates and our family members who in one way or another helped me in the successful completion of this work.

REFERENCES

1) Naveed sherwani ,a dissertation submitted at the summit of open silicon December1999 .
2) Venkatesh Prasad and Srinath b k a design for the issues in the torpedo processor ,RV VLSI design centre Bangalore year 2007 bangalore India .
3) S.Chien, S.Ma and L.Chen, “Efficient Moving Object Segmentation Algorithm Using Background Registration Technique”, IEEE transcript on circuits and systems, July 2002.
4) J.Moon, D.Kim and R.Park, “Video Matting Based on Background Estimation”, Enformatic Transactions on Engineering, December 2004.
5) R.C. Gonzalea and R.E. Woods, Digital Image Processing (2nd Edition), Prentice Hall, 2002.
6) Andreas Koschan and Mongi Abidi, “Comparison of Median Filter Techniques for Noise Removal in Color Images”, Imaging Robotics and Intelligent Systems Laboratory, The University of Tennessee, Knoxville.
7) Abdessamad Ben Hamza, “Removing Noise and Preserving Details with Relaxed Median Filters”, Dept. de Fiscia Aplicada, Universidad de Granada, Spain, 2009.
8) Pawan Patidar, Manoj Gupta and Sumit Srivastava, “Image De – Noising by Various Filters for Different Noise”, International Journal of Computer Application, November 2010.
9) D.Maheswari and Dr. V.Radha, “Noise Removal in Compound Image Using Median Filter”, International Journal on Computer Science and Engineering, 2010.

Published By:
Blue Eyes Intelligence Engineering
and Sciences Publication (BEIESP)