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Design of Low Voltage Low Power CMOS Analog Multiplexer For Bio-Medical Applications

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Abstract-One of the frequently used IC in bio-medical instruments for multiplexing the various signals is Analog multiplexer. This paper demonstrates the design of low voltage, low power CMOS analog multiplexer, using pass transistor logic for bio-medical application. The design goal is to achieve minimum power dissipation and minimum ON resistance with wide range of low voltage and low frequency of operation. The above goals are met by selection of proper technology parameters and by enhancing the design using minimum number of NMOS Pass transistor. Modified pass transistor logic is proposed, which replaces the traditional pass transistor logic for designing a multiplexer and require less no. of transistors. The ON resistance of 10Ω is achieved and the power dissipation of around 10nW is achieved in this design. Design and analysis is performed using 45 nm CMOS technology in CADENCE IDE.

Keywords: Bio-medical application, Low power, Low voltage, Low frequency, ON resistance, f_{switch}.

I. INTRODUCTION

Bio-medical signal processing system is widely used in health monitoring, brain machine interface, and neural prosthesis, etc. [5] [4].In pass-transistor logic style the source side is connected to some input signals instead of the power lines. The advantage is that one pass-transistor either it may be NMOS or PMOS is sufficient to perform the logic operation. With the effect of this no of transistors are reduced and input loads also reduced [8]. Pass-transistor logic with swing restoration circuitry is sensitive to voltage scaling [9].The scaling down of size and threshold voltage in MOS technology leads low power consumption and low ON resistance [1]. Driving a MOS transistor with analog signal is a great challenge for a designer and the transistor always in saturation [11]. Analog multiplexer design for bio-medical instruments concentrates on low power consumption low ON resistance and faithful reproduction of input at output [2].

Rest of the paper is organized as follows. Section II explains the generalized design of 8:1 Analog multiplexer using 24 pass transistors with less performance. Section III illustrates how the performances are enhanced by selection of technology parameters and implementation of design with minimum 14 transistors. Section IV gives the simulation results and section V concludes the paper.

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II. CONVENTIONAL DESIGN

Multiplexer is a device which selects one out of many inputs on the basis of selection lines. Fig. 1 shows a conventional design of an 8:1 multiplexer using NMOS pass transistor [3]. The logic equation describing the operation of the multiplexer is given by

$$V_{out} = A\,\overline{S2}\,\overline{S1}\,\overline{S0} + B\,\overline{S2}\,\overline{S1}\,S0 + C\,\overline{S2}\,S1\,\overline{S0} + D\,\overline{S2}\,S1\,S0 + E\,S2\,\overline{S1}\,\overline{S0} + F\,S2\,\overline{S1}\,S0 + G\,S2\,S1\,\overline{S0} + H\,S2\,S1\,S0$$

This multiplexer design uses 24 Pass transistors in the logic and 6 transistors for three selection lines. Table I shows the performance of the conventional design of a multiplexer's technology parameter considerations. Table II shows the performance parameters. Power dissipation of the multiplexer is calculated using equation [3] [4]

$$P.D = I_{DD} * V_{DD} \quad \ldots\ldots\ldots (1)$$

I_{DD} is the current drawn from V_{DD} by the multiplexer. The design should handle the power of below 100w with the supply voltage of 650mv [7].

ON resistance calculation is done using equation (1)

$$Ron = 1 / (K * I_D) \quad \ldots\ldots\ldots\ldots (2)$$

Where Id is the drain current of transistor and is given by

$$I_D = 0.5 * \beta * (V_{GS} - V_{TH})^2 \quad \ldots\ldots\ldots\ldots (3)$$

β is called as process parameter and is given by equation

$$\beta = \mu * Cox * W/L \quad \ldots\ldots\ldots\ldots (4)$$

Where W=width of channel
L=length of channel
Cox=oxide thickness
μ=mobility of carrier

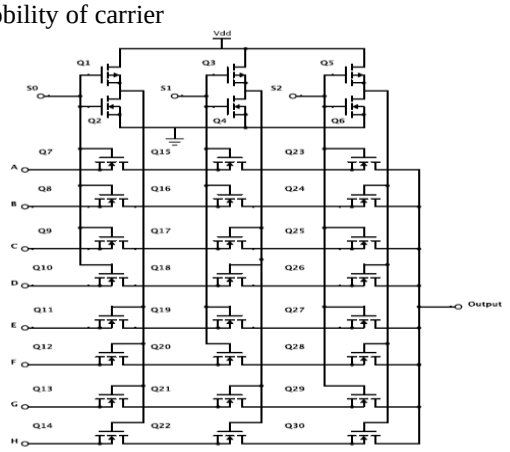

Fig.1 Schematic Diagram of 8:1 Multiplexer

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Table I: Technology Parameter

PARAMETER	VALUE
LENGTH(L)	45 nm
WIDTH (W)	100nm
THRESHOLD	520nm

Table II: Performance parameter

PARAMETER	VALUE
R_{ON}	21KΩ
POWER DISSIPATION	50nW

From equation 1, 2, 3 and 4 on resistance of the transistor depends on the technology parameters. As input of the ON transistor vary hence current I_D also vary, so ON resistance. In Order to make ON resistance as low as possible and constant so that input signal will be protected to be attenuated, the width W must be maintained as high as possible such that, Ron dependency on I_D will be least. Also the threshold parameter must be maintained at its minimum value.

Next section explains the optimum design and technology parameters that enhance the performance of the multiplexer.

III. PROPOSED OPTIMIZED DESIGN

Here is he proposed design of a multiplexer comprises of less no. of transistors. In this the transistor count is optimized without any degradation in the original output. Table III shows the technology parameter for which gives optimum performance for the design in Fig. 1. Optimized performance is given in Table IV. Further the performance is enhanced by modifying the design as explained below.

From Fig. 1 it can be observed that active high value of selection line S0 will forward A, B, C and D input signal to the next level. In the same way, active low value of selection line S0 will forward E, F G and H input signals. Similarly, Logic high value of S1 should allow the input signals A, B, E and F input signals. Active low value of selection line S1 will forward C, D, G and H input signals.

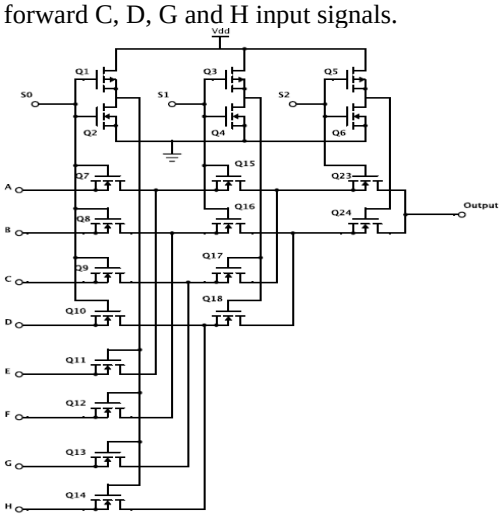

Fig. 2: Optimized Design Schematic of Multiplexer

Similarly, Logic high value of S2 should allow the input signals A, C, E and G input signals. Active low value of selection line S will forward B, D, F and H input signals. But, the above selection lines at a time will allow only one signal to the output.

From the above it is clear that, in any level of multiplexer, four input signals are blocked from a bunch of eight input signals and four are forwarded to the next level. Hence, the output of the first level any two inputs with opposite selection value are collected together as a pair and applied to the next level.

So, there are only four inputs to the second level. Again the same procedure is applied here also. Two pairs of two input signals with different selection value are collected at the output and forwarded to the last level. Only two input signals, between them any one of the input signal is preceded to the output.

Table III: Optimized Technology Parameter

PARAMETER	VALUE
LENGTH(L)	45 nm
WIDTH (W)	4.8 µm
THRESHOLD	120 nm

Table IV: Optimized Performance

PARAMETER	VALUE
R_{ON}	10.298Ω
POWER DISSIPATION	10nW

Table V: Optimized Performance Parameter Value

PARAMETER	VALUE
R_{ON}	10Ω
POWER DISSIPATION	8.66 nW

By this, the eight transistors in the second level of the multiplexer are replaced with the four and in the third level by two transistors. So, overall 10 transistors are reduced in the design and can be built with only 14 transistors. Hence power dissipation is almost half of the traditional logic with the same technology parameters given in Table III and 4. The overall optimized performance parameter is given in Table V.

IV. EXPERIMENTAL RESULT

The above Designed Analog multiplexer is tested for the wide range of low level low frequency input signals. Simulated result of both designs in Fig. 1 and Fig. 2 for the same values of technology parameters specified in Table II is shown in Fig. 3. Simulated result is obtained with the input signal characterized. Amplitude for input signal is from 10uV to 10 mV and frequency varying from 8KHz to 32KHz.The above Fig. shows analog multiplexer output at each and every voltages which are represented in the Table. The proposed multiplexer is operable at 1Hz to 1KHz switching frequency without a load capacitor and operable at 1MHz switching frequency with a capacitor of 10pF at 10KHz and C_L=4nF at 1MHz frequency and the Table VI showing that the input signal frequencies and their amplitude levels. This can be applicable for the amplitude levels of 10µV and above.

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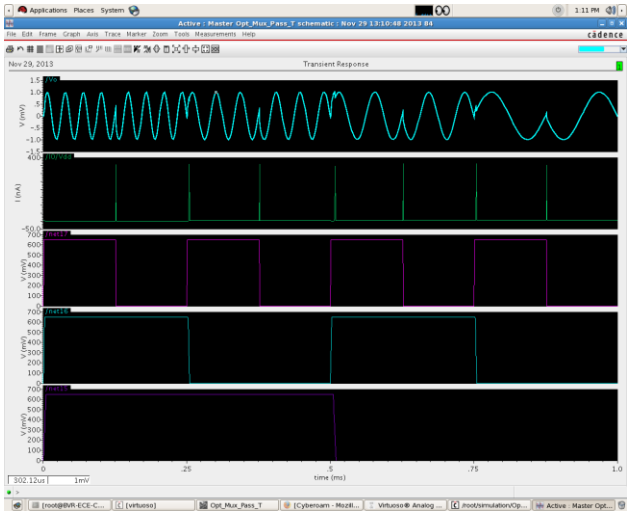

Fig.3: Simulation result at f_{switch}= 1 KHz

Table VI: Input Test Signals

AMPLITUDE (mV)	Frequency (KHz)
1	32
1	32
1	24
1	24
1	16
1	16
1	8
1	8

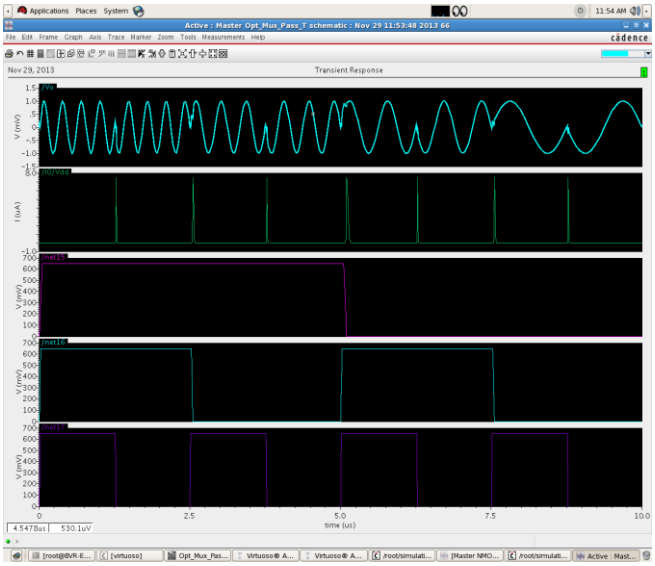

Fig. 4: Simulation result at f_{switch}= 100 KHz

V. CONCLUSIONS AND FUTURE SCOPE

The proposed multiplexer design for the purpose of bio-medical application, require less no. of transistors and is effectively used in the range of 0.1Hz to 10KHz switching frequency with a wide range of input signal voltage 10µV to 0.5V. Obtained ON resistance of 10Ω and optimized power dissipation of 7.8nW – 98nW.

Table VII shows the simulation results obtained for proposed design of Analog multiplexer.

Table VII: Analog Multiplexer Specifications

Specifications	Value
Supply voltage (V_{DD})	650 mV
Operating Voltage (Vin)	10uV-100mV
Switching Frequency (f_{switch})	0.1Hz-5KHz
Load Capacitance (C_L)	1pF-20pF
ON resistance (Ron)	≈ 10 Ω
Average Current Drain(I_{DD})	≈ 12nA
Power Dissipation(PD)	7.8nW – 98nW

VI. ACKNOWLEDGMENT

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