Power Quality Improvement in Switched Reluctance Motor Drive Using Zeta Converter

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Abstract*: This present paper deal with the power quality improvement using a Zeta ac-dc boost converter in the mid-point converter based Switched Reluctance Motor drive (SRM).Using a simple bridge rectifier the mid-point converter based SRM drive shows low power factor at ac mains and produces very high harmonics content. The proposed Zeta ac-dc boost converter in continuous conduction mode (CCM) with mid-point converter fed SRM drive which helps to improves the input power factor, reduces total harmonic distortion of ac mains current (THDi), provides constant dc link voltage and balanced capacitor voltages for static operation. The SRM drive with input Zeta converter is modeled and the performance is simulated in MATLAB environment for 230V and 50Hz. Here the Zeta converter performance is compared with a conventional bridge topology for the SRM drive.

Index Terms*— Power quality, Power factor correction (PFC), SRM, Mid-point converter, Zeta ac-dc boost converter, continuous conduction mode (CCM.)

I. INTRODUCTION

In the recent few years , Switched Reluctance Motor (SRM) have attracted renewed interest and become a competitive selection for many application of electric drive system due to its relative simple construction, reliability, fast response because of torque to inertia ratio and low cost. So with relatively simple converter and control requirement the SRM is gaining an increasing attention in drive industry. SRM uses power converter for its operation and they need a stable dc supply[1-2]. The conventional SRM drive usually includes a simple diode rectifier with a filter capacitor used as a front-end converter. Although this structure is simple but it draws a pulsating ac line current resulting in poor power quality that is low power factor and high harmonic content in the line current.

Therefore, the appropriate method that is power factor corrected (PFC) converters is used for AC-DC conversion which are also known as power factor pre-regulators (PFP). Here the used PFP is Zeta ac-dc boost converter which operates in continuous conduction mode (CCM) to achieve good power quality at the input AC mains. In CCM, a sinusoidal input current having power factor nearly at unity can be obtained with the help of two feedback loop i.e one for outer voltage and another for inner current feedback loop [3]. Figure1 shows a conventional bridge converter fed mid-point converter based SRM drive. The demerit of this converter is that it is difficult to maintain the voltage across capacitor balanced at dc bus.

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To improve the input power factor of power converter and reduces total harmonic distortion (THD) of ac mains and also maintains a constant dc voltage, a power factor correction circuit is needed at input side of the converter and placed in the front-end side of the converter which in turn interfaced at the load side with the load[4].

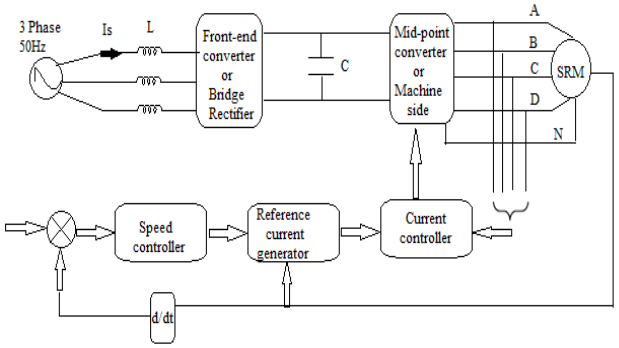


Figure 1.Conventional Bridge Rectifier as front end converter fed SRM drive

Here, the Zeta AC-DC boost converter is used for the power quality improvement and maintain constant dc voltage[5].

A Zeta converter with mid-point (machine side) converter fed SRM drive is suitably designed, modeled and simulated in Matlab/Simulink .

Advantages of simulation method are as follows:

- saves the run time
- It is free from expression
- Can be applied widely

The proposed SRM drive system helps of improve the power factor almost to unity with low THD of supply current and balanced the dc link capacitor voltage.

II. PROPOSED TOPOLOGY FOR SRM DRIVE

In SRM, the Zeta converter is used as front-end converter to improve the power quality at the input ac mains. Fig 2 Shows the schematic diagram of the proposed scheme

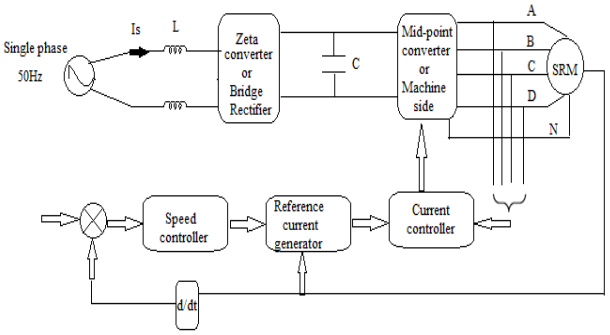


Figure 2 Proposed Zeta converter fed mid-point converter fed SRM drive

Figure 3 shows the power circuit of a zeta converter based SRM.The proposed system is consists of Diode bridge rectifier (DBR) and Zeta converter ac-dc boost converter fed mid-point converter based SRM drive connected in cascade configuration.

The zeta converter has an inductor on each input line which is connected to the bridge rectifier and capacitor connected on the dc link. The outer voltage feedback controller senses the dc voltage (V_{dc}) and compared it with the reference voltage (V_{ref}) to generate the error voltage, which is passed through the Discrete Proportional Integral (PI) controller. A multiplier is used to generate the reference current signal (I_{ref}) .This reference current is then sends to MOSFET and the power switching (M) is operating at 142KHz frequency .

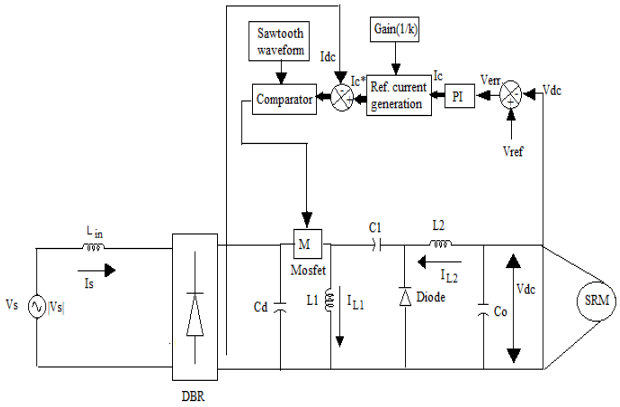


Figure 3 Proposed power circuit of a Zeta converter based SRM

III. DESIGN AND ANALYSIS OF ZETA CONVERTER

The design procedure of PFC based Zeta ac-dc converter includes the calculations of components are as follows.

A) Inductor design

The value of duty cycle, for a Zeta converter operating in continuous conduction mode (CCM) (De Britto et al 2008; Ali et al 2010) is defined as,

$$D = \frac{V_o}{V_{in} + V_o}$$

Where, D is the duty cycle, V_{dc} is the output voltage at dc link and Vs is the rms value of input ac voltage

To determine the value of inductance L_1 and L_2 the peak-to-peak ripple current is taken approximately 10-20% of the average output current. The value of these inductances may be expressed as,

$$L_1 = L_2 = \frac{V_{in} D}{\Delta I_L f_s}$$

The coupling capacitor (C_1) is designed on the basis of its ripple voltage. The maximum voltage handled by a coupling capacitor (C_1) is equal to input voltage. It can be estimated as,

$$C_1 = \frac{I_o D}{\Delta V_{c1} f_s}$$

The output capacitor (C_o) must have enough capacitance to maintain the dc link voltage and must have to provide continuous load current at high switching frequency. It can be calculated as,

$$C_o \geq \frac{I_o D}{\Delta V_{co}(0.5 f_s)}$$

Where D is duty cycle, V_o is dc link voltage, V_{in} is rms value of the input voltage, I_o is output rated current, f_s is switching frequency ,ΔV_{c1} is the ripple voltage of the coupling capacitor, ΔV_{co} is ripple voltage of output capacitor

IV. CONTROL OF ZETA CONVERTER FED SRM DRIVE

In normal condition, a single-phase AC supply is a sinusoidal voltage source having amplitude (V_{sa}) and frequency (f). The instantaneous input voltage is given as,

$$V_s = V_{sa} \sin\omega t$$

From input supply voltage, V (t) a voltage template is evaluated to generate reference current and controls the AC mains current to follow the reference current to achieve better power factor using a PFC ZETA converter. This control scheme consists of a Discrete Proportional Integral (PI) controller and reference current generation which provide switching frequency to the power switch (MOSFET).

A Discrete PI controller is used for the voltage regulation of the output voltage in the voltage loop. The DC link voltage (V_{dc}) is sensed and then compared with the reference voltage (V_{ref}).

The resulting voltage error (Verr) at mth sampling instant is given as,

$$V_{err}(m) = V_{ref}(m) - V_{dc}(m)$$

The output of Discrete PI controller at mth sampling instant can be given as,

$$I_c(m) = I_c(m-1) + K_p\{V_{err}(m) - V_{err}(m-1)\} + K_i V_{err}(m)$$

where I_c (m) is the outputs of dc link voltage controller at m^{th} and $(m-1)^{th}$ sampling instants , V_{err} (m) and V_{err} (m-1) are the errors in dc link voltage at m^{th} and $(m-1)^{th}$ sampling instants and K_p is the proportional gain and and K_i is the integral gain.

Current control loop is used for wave-shaping of input ac current to obtain power factor nearly at unity and reduces the current harmonics. Current signal should match the rectified line voltage to improve the input power factor.

The input voltage template V(t) obtained from sensed supply voltage is multiplied with its amplitude (the output of Discrete PI controller) and the resulting signal forms the reference for input current.

$$I_c^* = I_c(m) * V(t),$$

where $V(t) = |V_{sa}| / V_{sa}$

The inductor current error is the difference of reference current and sensed inductor current. This error signal is amplified by a gain K and compare to triangular repeating waveform or sawtooth waveform to generate gating signals for power MOSFET of the Zeta converter. If the signal is

greater than the triangular waveform, then a switching signal is generated for the MOSFET used as switch M else it is not gated and the freewheeling diode conducts.

V. MATLAB MODEL OF PROPOSED PFC ZETA CONVERTER BASED SRM

The proposed PFC ZETA converter based SRM drive is modeled in Matlab/Simulink environment as shown in fig 4.

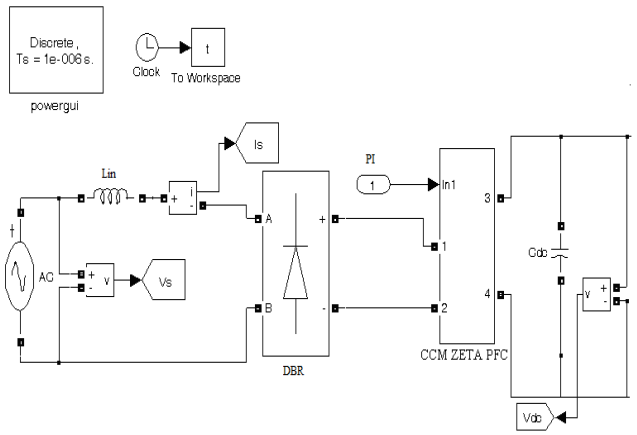


Figure 4. Matlab model of proposed PFC ZETA converter based SRM drive

The PFC ZETA converter based topology is modeled where an average current control scheme with current multiplier approach is applied using Discrete PI (Proportional Integral) controller for operating the ZETA converter in continuous conduction mode (CCM). The PWM switching frequency of power switches is maintained constant at142 kHz . The designed values of the ZETA converter components obtained from the various equations are selected appropriately to achieve better power quality at the input AC mains. More components values along with Discrete PI controller parameters are given in Appendix.

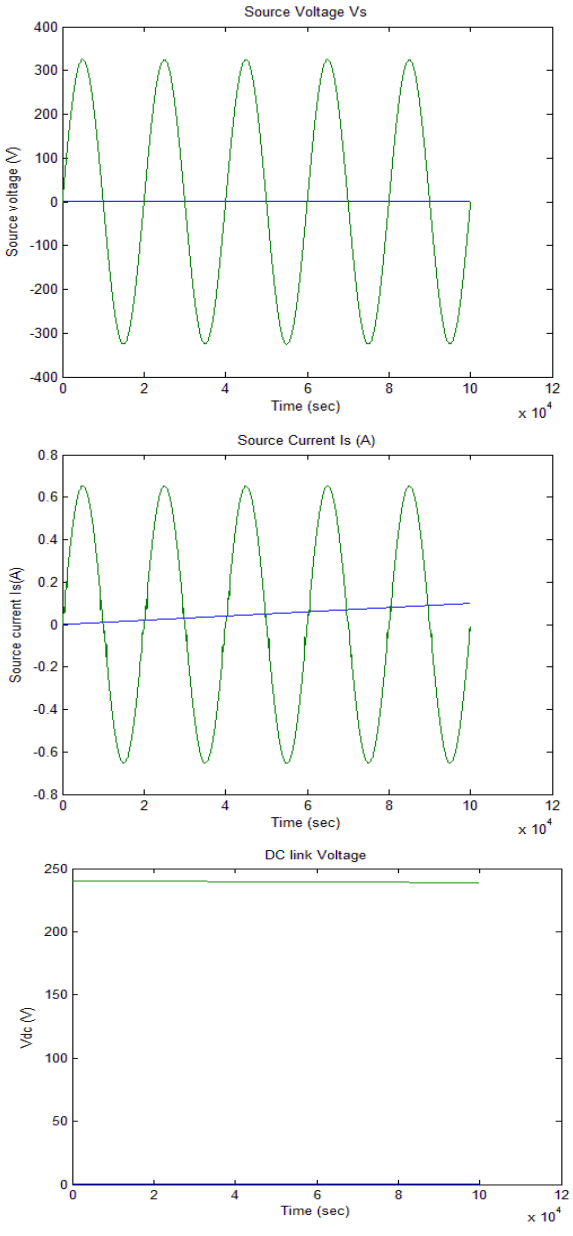
This example presents a current-controlled 60-kW 6/4 SRM drive using the SRM specific model based on measured magnetization curves. The SRM is fed by a three-phase asymmetrical power converter having three legs, each of which consists of two IGBTs and two free-wheeling diodes. During conduction periods, the active IGBTs apply positive source voltage to the stator windings to drive positive currents into the phase windings. During free-wheeling periods, negative voltage is applied to the windings and the stored energy is returned to the power DC source through the diodes. The fall time of the currents in motor windings can be thus reduced. By using a position sensor attached to the rotor, the turn-on and turn-off angles of the motor phases can be accurately imposed. These switching angles can be used to control the developed torque waveforms. The phase currents are independently controlled by three hysteresis controllers which generate the IGBTs drive signals by comparing the measured currents with the references. The IGBTs switching frequency is mainly determined by the hysteresis band.

The converter turn-on and turn-off angles are kept constant at 45 deg and 75 deg, respectively, over the speed range. The reference current is 200 A and the hysteresis band is chosen as +-10 A. The SRM is started by applying the step reference to the regulator input. The acceleration rate depends on the load characteristics. To shorten the starting time, a very light load was chosen. Since only the currents are controlled, the motor speed will increase according to the mechanical dynamics of the system. The SRM drive waveforms (phase voltages, magnetic flux, windings currents, motor torque, motor speed) are displayed on the scope. As can be noted, the SRM torque has a very high torque ripple component which is due to the transitions of the currents from one phase to the following one. This torque ripple is a particular characteristic of the SRM and it depends mainly on the converter s turn-on and turn-off angles.

VI. RESULTS AND DISCUSSION

The main purpose of the modeling and simulation is to declare the design of proposed PFC ZETA converter based SRM drive is valid which has high power factor nearly at unity and low THD of ac mains current. The voltage at dc link is maintained almost constant that is 240 V.

Under steady state operation, the input voltage (Vs), current (Is) waveforms, DC link voltage (V_{dc}) & voltage across DBR at ac mains of 230V are shown in fig- 5



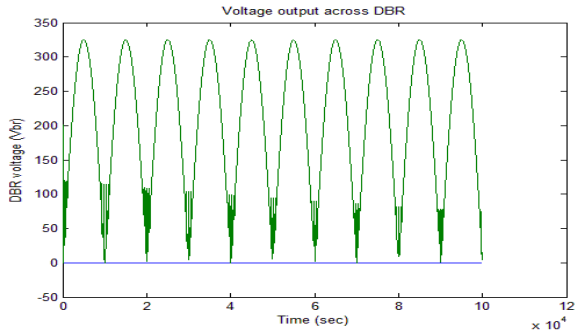
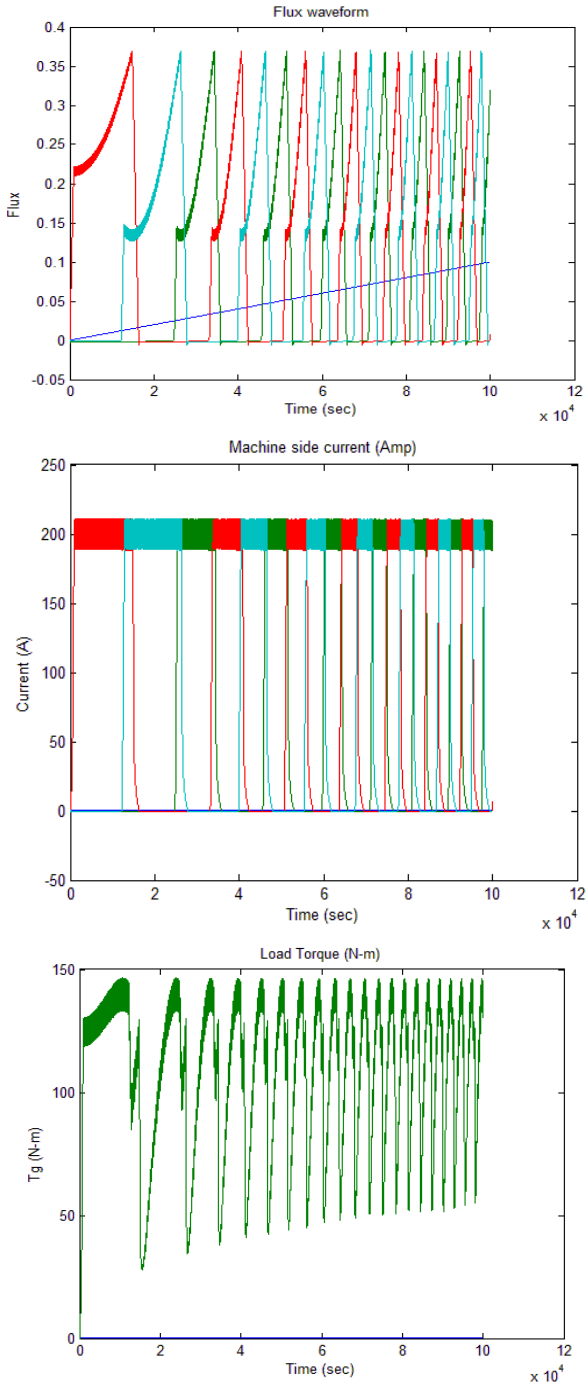


Fig-5 Performance of proposed converter in terms of source voltage (Vs), source current (Is), DC link voltage (V_{dc}), Voltage across at diode bridge rectifier (V_{dbr}) at 230V ac mains

The SRM is driven by a machine side converter, Fig shows Flux, Load current (IL), load torque (TL) & speed (w) of the output side.



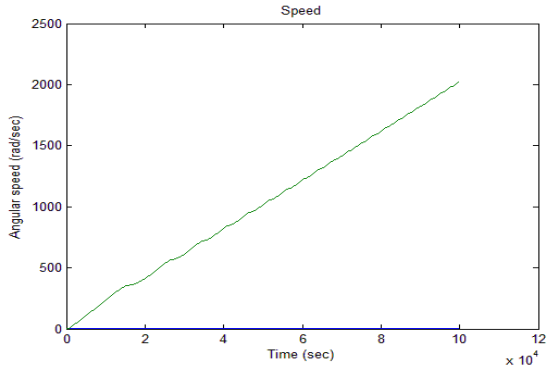


Fig-6 Steady state response of ZETA converter fed SRM drive at 230V source input voltage.

Table-I shows the variation of power factor (PF), %THD of ac main current and crest factor of PFC ZETA converter based front end converter with a wide variation in ac mains voltage. These results validate the power factor correction and constant power operation in wide input voltage variation.

TABLE-I

Simulated results of ZETA fed SRM Drive by varying supply voltage

Vs (V)	Is (A)	V_{dc}	PF	THD	CF
125	0.254	238.8	0.9993	0.248	1.4
140	0.320	238.8	0.9994	0.248	1.4
150	0.368	238.9	0.9996	0.249	1.4
180	0.392	239.1	0.9996	0.249	1.4
200	0.410	239.6	0.9998	0.249	1.4
220	0.432	239.8	0.9998	0.251	1.4
230	0.452	239.8	0.9998	0.256	1.4
250	0.495	239.9	0.9998	0.258	1.4
270	0.551	240	0.9999	0.262	1.4
300	0.594	240	0.9999	0.264	1.4
320	0.620	240	0.9999	0.272	1.4
350	0.707	240	0.9999	0.276	1.4
370	0.725	240	0.9999	0.278	1.4

VII. CONCLUSION

A PFC ZETA boost AC-DC converter for mid-point converter fed SRM drive has been designed and its performance is simulated for a 60 kW, 6/4 pole SRM. The proposed ZETA converter operating in continuous conduction mode (CCM) has been shown an improved performance with nearly unity power factor of input ac mains. The voltage at the dc link capacitor are kept balanced which is needed for the stable operation of mid-point converter fed SRM drive.

VIII. APPENDIX

PI controller gain:- (Kp) : 0.05 and (Ki) : 0.004 , Switching frequency of PFC switch (fs) : 80 kHz,
PFC components: - inductor (L1 =L2): 0.1mH , coupling capacitor (C1): 37.56µF, DC link capacitor (Co): 4.1µF,
Vs(rms) : 230V, 50 Hz, source inductance Lin : 20mH.

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