

Programmable Decimation Filter Design For Multi-Standards Software Defined Radio (SDR) Reciever

Falah Hasan

Abstract— This Paper Investigates The Design Of Programmable Decimation Filters To Be Used In The Channelizer Of Multi-Standard Software Defined Radios Receivers. The Technique Of New Algorithms For Reducing The Passband Ripple Of Linear Phase Fir Digital Filters Which Minimizes The Passband Deviation In The Decimation Block Is Introduced And Is Used To Implement A Multistage, Multi-Standard Decimating Filter. The Design Will Enhanced Different Communications Standards And Is Thus Ideal For Use In Systems Which Support Dynamic Reconfiguration. Results Obtained Shows An Important Reduction In The Passband Ripple In The Decimation Part From 0.03 Db To 0.012 Db And High Reconfigurability In The Filtration Requirements.

Index Terms— FIR, SDR, Digital down-converter, GSM, Equiripple FIR, passband ripple, adjacent band rejection, blocker requirements.

I. INTRODUCTION

Modern mobile multimedia devices need to deliver high performance. The user requires adequate functionality, adaptive behaviour and energy-efficiency. As in all designs a trade off needs to be found for the optimal solution. With the growing popularity of mobile multimedia devices, the demand for energy-efficient wireless communication increases. A key part of wireless communication is the Digital Down Converter (DDC). Like most algorithms, it can be performed by dedicated hardware or executed on a kind of processor. Which solution is preferred, depends on the desired adaptive behaviour, processing performance and energy-efficiency. In a multimedia device it is possible that the digital down conversion is only needed occasionally. For example, when the GSM module is activated, to connect to the internet via WLAN, it can be useful to reconfigure that part of the chip, which is used for the DDC, to execute other tasks, instead of going to its standby modus. In this case the hardware has a higher utilization factor. When a DDC is needed in a device like a mobile phone or a single mode digital radio, it has to perform a dedicated task. The algorithm has to be performed continuous and only the parameter settings might be changed. Adaptability and spare performance will not be used in this situation [1]. Current radio frequency (RF) transceivers demand higher integration for low cost and low power operations, and adaptability to multiple communication standards. Specifically, software defined radio (SDR) is a wireless interface technology in which software-programmable hardware is used to provide flexible radio solutions in a single transceiver system. Multi-standard operation is achieved by using a receiver

architecture that performs channel selection on chip at baseband. Several design and implementations of decimation filters for software defined radio are presented in recent researches.

To show the prime importance of the Software Defined Radio, some of relevant works in the field need to be reviewed. Decimation filter design for GSM, WCDMA (Wideband Code Division Multiple Access), 802.11a, 802.11b, 802.11g and WiMAX (Worldwide Interoperability for Microwave Access) standards are given in [2].

A multistage sample rate converter for SDR receiver was proposed by [3], The order of Equiripple FIR filter is decided according to the Hermann formula, they got the length of desired Equiripple linear phase filter $L = 52$ and reduced the number of multipliers to 26 Multipliers. A low passband error DDC filter to be worked according to GSM mask frequency with adjacent band rejection of (-105db) and (-0.05db) passband ripple was reported by [4]. Decimation filter for Multi- Standard Wireless Transceivers using MATLAB with (-0.1db) in passband ripple and (65db) stopband attenuation to work with GSM, WCDMA, WLAN was designed by [5]. New design of multi standards DDC filter with minimum passband ripple (-0.03dB) to work with GSM, IS-95, and WCDMA was produced by [6]. The purpose of this paper is to advance a new technique for the design of linear-phase FIR filters with equiripple stopbands and very low ripple in the passbands. The proposed technique is based on the McClellan-Parks algorithm for FIR filter design. This paper is organized as follows. Section II examines the SDR receiver front end before focusing on techniques for implementing high-speed digital filters in hardware. Section 3 introduces the filter design problem, mathematical background and the details of the coefficient optimization. Section 4 introduces the multi-standard DDC filter design for the GSM and WCDMA standards, while section 5 presents the results of the design exercise. Section 6 concludes this paper.

II. SDR RECEIVER SCENARIO

This section describes the SDR receiver scenario and provides an analysis of issues [5] relating to the simulation of FIR decimation filters in MATLAB. The basic receiver for SDR uses a digital down converter (DDC) to replace the analogue intermediate frequency (IF) demodulator as shown in the system block diagram of figure 1(a). This eliminates the local oscillator (LO)/IF carrier mixing and achieves perfect gain/phase matching between channels. The IF output from the RF mixer is converted to a digital signal using a high speed analogue to digital converter (ADC). This signal is then converted to baseband by the DDC for processing by the digital signal processor (DSP). The block diagram for the DDC is shown in figure 1(b).

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The output from the ADC and the programmable numerically controlled oscillator (NCO) are multiplied to centre the desired signal at the baseband location. Interfering signals in adjacent bands are removed using a narrow band (high selectivity) filter built from a sequence of multi-rate filters consisting of a cascaded integrator-comb (CIC) filter which can be decimated by a factor from 5 to 64, a compensating FIR filter (CFIR) which decimates by 2, followed by a programmable FIR filter (PFIR). The output of the PFIR can be programmed to decimate by 2 if desired. Because of the high input data rates (typically 50-100 Mbps), the DDC filter implementation needs to be as fast and as efficient as possible. Generally, multiplierless filter implementations are preferred because of their high speed and hardware efficiency.

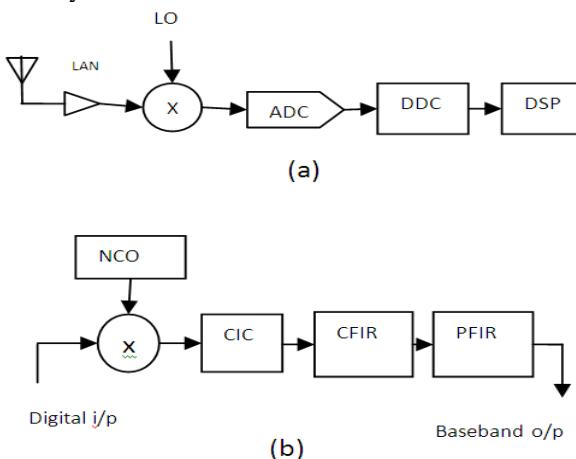


Figure 1. (a) The basic SDR system block diagram, and (b) The digital down converter unit.

2.1- Optimal FIR filter design.

While the truncated-and-windowed impulse response design algorithm is very simple and reliable, it is not optimal in any sense. These design are generally inferior to those produced by algorithms that employ some optimization criteria in that it will have greater order, greater transition width or greater passband/stopband ripples. Any of these is typically undesirable in practice, therefore more sophisticated algorithms come in handy [7].

2.3-The Remez Exchange Algorithm.

When one design a filter using the **Remez** algorithm it is of interest to know an approximation of the filter order N to use in the filter design. The filter order is given by $N = M - 1$, and the filter length M may be estimated by using Kaisers approximation formula given by

$$M = \frac{-20\log_{10}(\sqrt{\delta_p \delta_s} - 1)}{14.6 \Delta f} 1, \quad \Delta f = (\omega_s - \omega_p)/2\pi \quad (1)$$

where Δf is the width of the transition band $\Delta f = (\omega_s - \omega_p)/2\pi$, δ_p is the passband tolerance related to the passband ripple A_p in dB, and δ_s is the stopband tolerance related to the stopband attenuation A_s in dB. To use the function **Remez** the first step is to guess the order of the filter using equation (1). The obtained filter coefficients are then evaluated. Check the minimum stopband attenuation and compare it with the given A_s and then increase or decrease the filter order. Repeat this procedure until the desired A_s is obtained. The most common implementation of the Remez Exchange Algorithm is the version by Parks, McClellan and Rabiner [8], [9].

$$\delta_p = \frac{10^{A_p/20}-1}{10^{A_p/20}+1} \quad , \quad A_p = -20\log_{10} \frac{1-\delta_p}{1+\delta_p} > 0 (\cong 0) \quad (2)$$

$$\delta_s = 10^{-A_s/20} \quad , \quad A_s = -20\log_{10} \frac{\delta_s}{1+\delta_s} > 1 \quad (3)$$

III OPTIMUM FILTER FOR GSM MASK FREQUENCY.

Depending on above theorems [8,9] we introduce the following flow chart to minimize the passband error of the linear phase FIR filter to be used with multi standards DDC decimation filter with any desirable error in passband ripple in order to reduce the power consumption by the filter. The flow chart is shown in Figure 2. The multistage decimator block diagram is shown in Figure 3.

The 5-stage cascaded integrated comb (CIC) filter takes the high-rate input signal and decimates it by a programmable factor. The CIC filter is followed by a 21-tap compensation FIR (CFIR) filter that equalizes the “droop” due to the CIC filter and provides further lowpass filtering and decimation by 2. The CFIR is followed by a 63-tap programmable FIR (PFIR) filter that is used for a final decimate-by-2. One thing to note is that in a multistage decimator one would always put the simplest filter first (that is, working at the highest rate), and would progressively increase the complexity of the filters in subsequent stages. This is exactly what happens here, the CIC filter is attractive at high rates because it provides multiplierless operation. The filter provides (coarse) lowpass filtering using adders and delays. The filter is not without its drawbacks though, its magnitude response is very far from ideal and exhibits a “droop” in the passband which progressively attenuates signals. The CFIR filter is also relatively simple, having only 21 taps. Its primary job is to compensate for the droop from the CIC filter. The PFIR filter is the most complex of the three, requiring 65 multiplications per sample, which is why it operates at the lowest rate. It is worth pointing out that this design that required a fixed filter order. Also both the CFIR and PFIR are linear-phase filters by construction. Linear phase is usually a desirable characteristic in data transmission. To minimize the passband error of the linear phase FIR filter, the flow chart shown in Figure 2 is proposed.

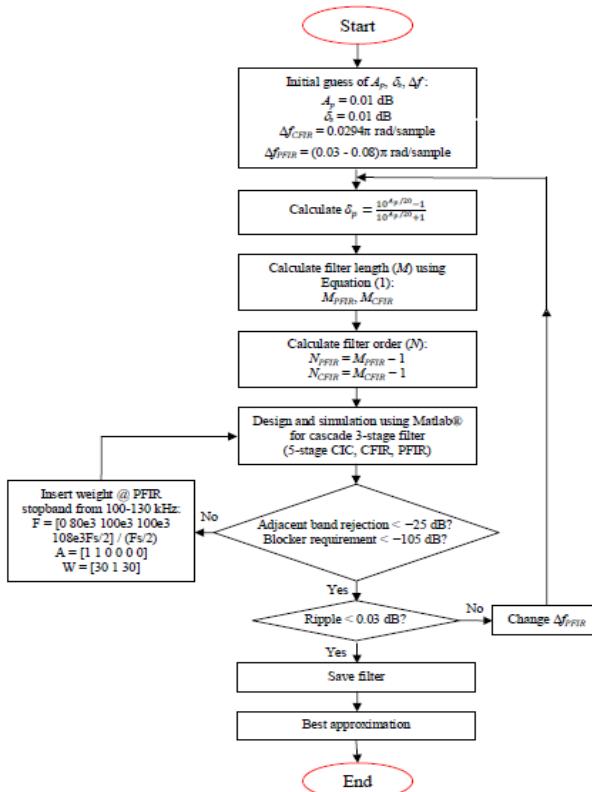


Figure 2: proposal FIR filter design flow chart

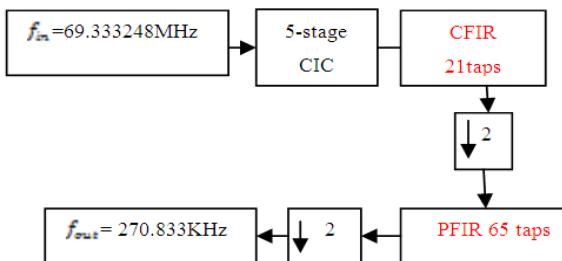


Figure (3) : Proposed DDC block diagram for GSM base station

As shown in Figure 3, the input sample rate to the proposed decimation filter is 69.333248 MHz and the output sample rate is 270.833 KHz respectively which represent the intermediate frequency of GSM system and its baseband sample rate.

IV. EXPERIMENTAL MATLAB SIMULATION RESULTS

4.1- Designing the CIC filter.

The CIC filter has 5 stages and a decimation factor of 64. To view the magnitude response of this filter, we can simply create a CIC decimation object and use fvtool. The magnitude response is shown in Figure (4). The filter exhibits a $|\sin(x)/x|^5$ shape. It also has a large DC gain (more than 180 dB), that has to be compensated for.

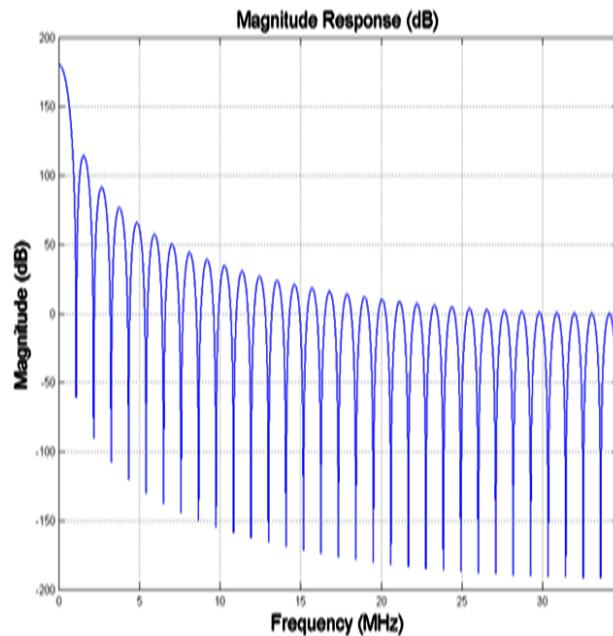


Figure (4): Magnitude response of 5-stage CIC decimator

4.2-Designing the CFIR filter

Since the overall passband is 80 kHz, it is worthwhile to look at the CIC response in this band to get an idea of what the CFIR filter must compensate for. The passband details of the CIC filter are shown in Figure (5).

The filter shows a droop with an attenuation of about 0.4 dB at 80 kHz. This is far more than the allowable peak to peak ripple. We want to design an optimal equiripple filter to make the most of the 21 taps available. Since only 11 coefficients are actually freely specifiable, we are constrained to a linear-phase design.

We use the firceqrip function for the following important reasons:It allows for compensation of responses of the form $|\sin(x)/x|^N$, The filter order is specifiable, It allows for a slope in the stopband, which we will use to attenuate spectral replicas of the PFIR filter that follows, We can constrain the peak passband and stopband ripples, Instead of the cutoff frequency, we can specify the passband-edge frequency.

In this particular case, since the passband is the interval [0,80kHz], we want to compensate for the CIC droop in the passband only. The filter order is determined for us by the hardware. For the passband-edge frequency, we select 90 kHz, since this is the final passband of interest. We choose a very small passband ripple, 0.01 dB, in order for the overall ripple to be within specification of GSM requirements, keeping in mind that there is still the PFIR filter to follow which will add its own passband ripple.

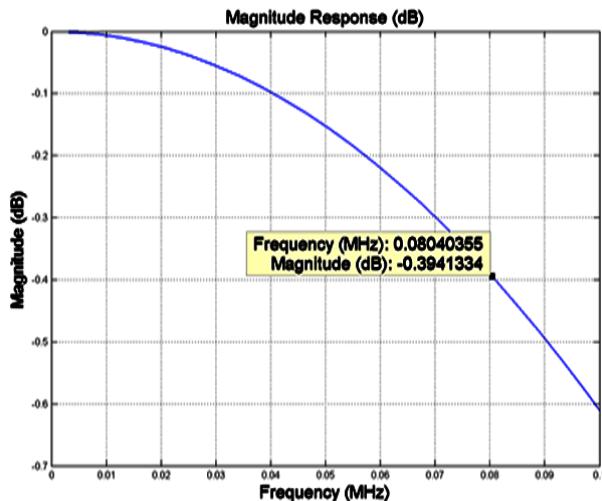


Figure (5): Passband details of scaled 5-stage CIC decimator.

The stopband attenuation is selected as 80 dB with a 60 dB slope to provide adequate attenuation of the PFIR spectral replicas. Because this is a 5-stage CIC, the droop is of the form $|\sin(x)/x|^5$, so we select 5 as the sinc power to compensate for. Finally, the sinc frequency factor is chosen as 0.5.

The magnitude response of the CFIR filter is shown in Figure (6) quantized to 16 bits. Without zooming in, it is hard to see the passband inverse-sinc response. We can see however, as expected, the large transition width along with the sloped stopband.

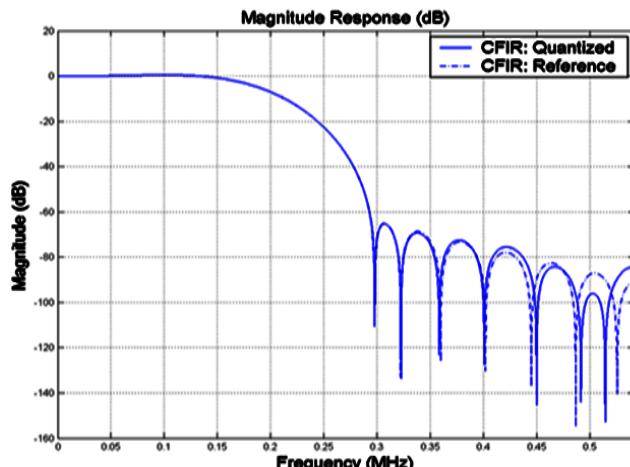


Figure (6): Magnitude response of CFIR filter

To get an idea of the combined filter CIC*CFIR, we overlay the magnitude response of each of these filters, along with the combined magnitude response of the two. This is shown in Figure (7). We can see the spectral replicas of the CFIR filter centred around the frequency it is operating at, 1.0833332 MHz.

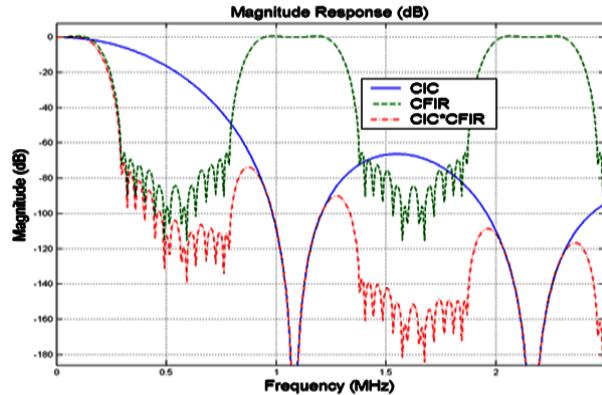


Figure (7): Magnitude response of CIC filter and CFIR filter overlaid, along with the combined response of the two.

It is hard to see the sinc compensation in this plot. For this we zoom in further. The zoomed-in plot is shown in Figure (8). The plot covers approximately the band [0, 120kHz]. It is evident from the plot that the combined response is virtually flat in the passband (up to 80 kHz).

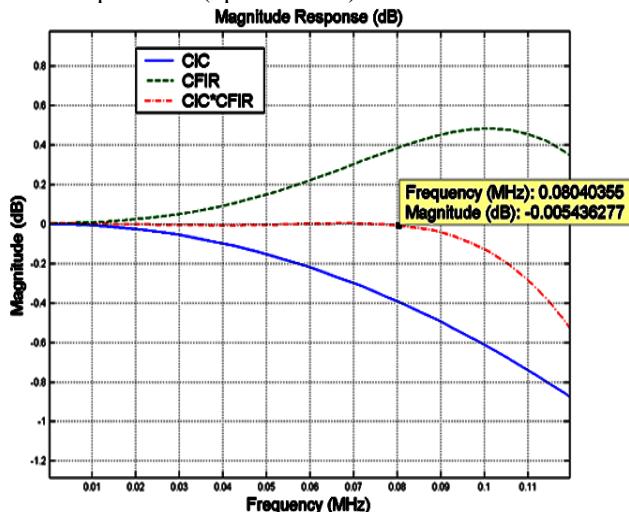


Fig.(8): Passband details for the magnitude response of CIC filter and CFIR filter overlaid, along with the combined response of the two.

4.3-Designing the PFIR filter .

An overlay of the GSM spectral mask requirements [9] with the combined response of the CIC filter and the CFIR filter is shown in Figure (9). It is evident from the plot that the combination of these two filters is not sufficient to meet the GSM requirements for either adjacent band rejection or blocker requirements. The combined filter still has a transition band that is too large, due to the large transition band from the CFIR filter. Clearly the combination of these two filters does not meet the GSM requirements. The PFIR filter is intended to be used to do the extra work required to meet the GSM specifications.

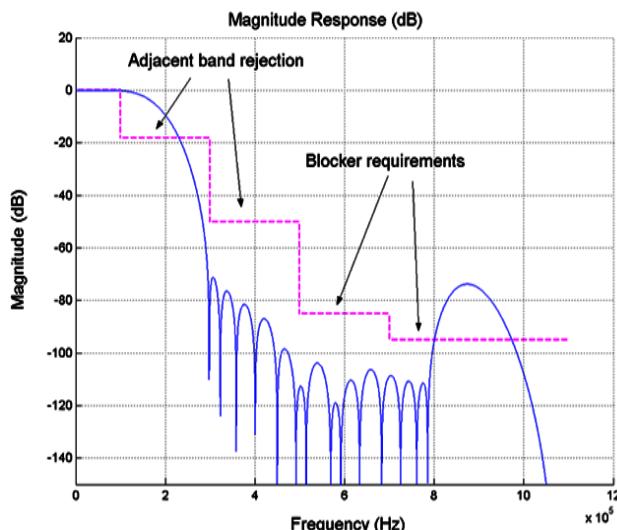


Fig.(9): Magnitude response of combined CIC and CFIR filters overlaid with the GSM spectral mask requirements.

From Equations (3-2-1) we choose the stopband allowed deviation ($\delta_s = 0.01$) and we assume that we need to have a low passband ripple $A_s \leq -0.015 \cong -0.012 \text{ dB}$ then the passband allowed deviation δ_p is determined by equation (2) as:

$$\delta_p = \frac{10^{\frac{0.012}{20}} - 1}{10^{\frac{0.012}{20}} + 1} \cong 0.0007$$

Then the filter length is:

$$M = \frac{-20 \log(0.01 \times 0.0007)^{1/2} - 13}{14.6 (0.28 - 0.24)} + 1 = 65$$

And filter order is:

$$N = M-1 = 65-1 = 64$$

It is a linear-phase FIR filter consisting of 65 taps. The design gets a little tricky though. We know that the passband edge is 80 kHz, and the first adjacent band is at 100 kHz. If we design a simple lowpass filter with Remez or Gremez, The passband ripple requirement is not quite met. We can alter the weights to get better passband ripple, but we must be careful not to violate the adjacent band specifications. A setting of $W = [10, 1]$; would do the trick, but with significantly less adjacent band attenuation. A compromise can be achieved by setting up the design as a lowpass with two separate stopband regions, each one with a different weight to be used in the optimization.

The quantized PFIR filter is shown in Figure (10). The maximum coefficient is 0.3378 so once again we use the [16, 16] format. The reference (nonquantized) filter is also shown, but it is practically indistinguishable from the quantized response. The different attenuation in the two stopbands due to the different weighting is evident. The passband ripple is kept small in order to not exceed the allowed peak to peak ripple. A plot showing the magnitude responses of all three filters, CIC, CFIR, and PFIR, is shown in Figure (11). Notice that the sloped stopband of the CFIR filter provides maximum attenuation when the spectral replicas of the PFIR filter occur.

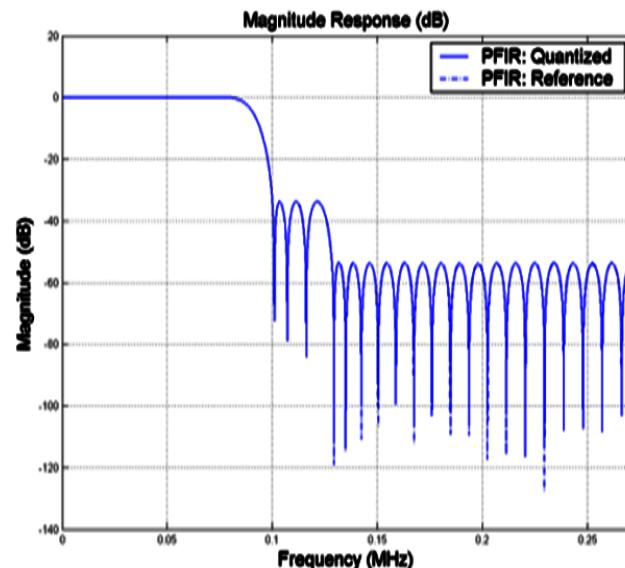


Fig.(10): Magnitude response of PFIR filter.

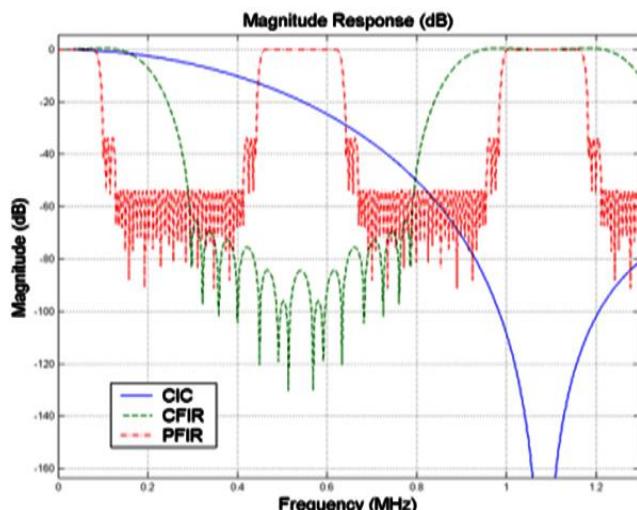


Fig. (11): Magnitude response of CIC, CFIR and PFIR filters.

4.4-The overall response

The overall response of the combination CIC*CFIR*PFIR is shown in Figure (12). The GSM spectral mask requirements are now easily met as is clearly shown in the figure. The requirement that the peak to peak ripple be less than 0.1 dB is easily met. Figure (13) shows the maximum error in passband ripple results by this design is approximately (-0.012dB) after making zooming to final GSM mask of three filters that designed. The passband ripple for new filter was reduced from -0.028dB to -0.012dB and compensate the adjacent band rejection and blocker requirements of the filter. This development increase the effective length of words and reduce the power consumption by the filter, therefore make the develop on 3G base station more economical and effective. From above results we can calculate the stopband attenuation as follow:

atypical absolute specification of this filter is defined in equation (3) in which is:

$$A_s = -20 \log_{10} 0.01 = -40 \text{ dB}$$



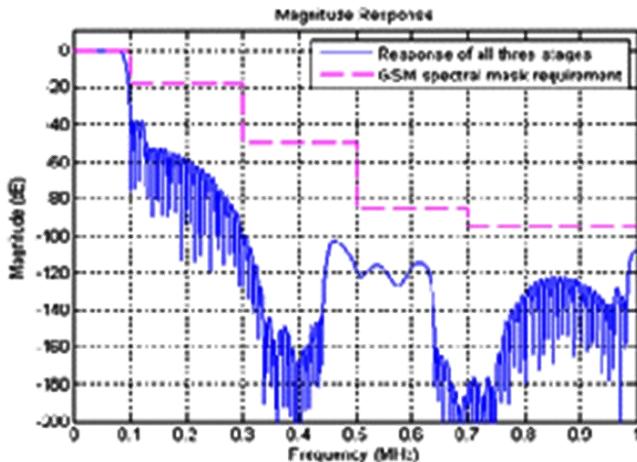


Figure (12): proposed Combined response of CIC, CFIR, and PFIR filters, along with GSM spectral mask requirement.

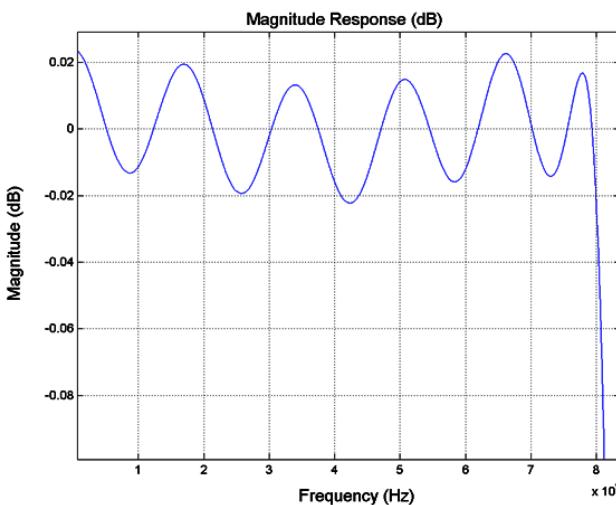


Fig. (13): Average passband ripple of proposed DDC filter = -0.012db after zoom in.

V.COMPARISON WITH OTHER DESIGN

5.1-Passband ripple

The GRAY CHIP (GC) passband response for GSM mode [7] is shown in Fig.(13). It is clear that the proposal model more effective in passband region, lease passband ripple by about (-0.077db) from GC-GSM mode as explained in table (2).

Table (2): DDC filter specifications comparison.

Parameters	GSM MODE Conventional GC 4016	GSM Mode Conventional GC 4017	In Ref. [11]	Proposed DDC
Passband ripple	-0.09dB	-0.03dB	-0.015dB	-0.012dB
Stopband attenuation	40dB	40dB	40dB	40dB

5.2-Adjacent band rejection and blocker requirements

The adjacent band rejection and blocker requirements of proposed model is shown in fig.(12). It appears more

effective than the conventional GSM mode so the filter was compensated and developed as explaine in tables (3).

Table (3) comparison between conventional and proposal DDC Filter

Parameters	Conventional (GC)DDC Filter	Proposed DDC Filter
adjacent band rejection	-25db	-35db
Blocker requirements	-105db	-117db

VI. CONCLUSIONS

From tables (2) and (3), many parameters was developed and compensated in the proposed design to follow the rapid growth in wireless communication system to be more effective and meet the user requirements. The minimum error in passband ripple mean, low power consumption by filter, increase the memory size, and not only reduces the speed requirement of DDC converters below that necessary with traditional low-pass sampling; it also reduces the amount of digital memory necessary to capture a given time interval of a continuous signal. The clock of DDC filter is also improved to allow this filter to work with multi-standard like GSM, WCDMA, and support all system that works in the frequency band up to 100MHZ. The blocker requirement is moved far from nearest band to avoid any interference between GSM signal and other signals. So the DDC filter was developed and improved to get more efficient in wireless communication systems.

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