Simulation and Implementation of Orthogonal Frequency Division Multiplexing (OFDM) Model Based SDR

Hazim Salah Abdulsatar

Abstract— An OFDM transceiver based on software defined radio (SDR) techniques is modeled by MATLAB in this paper. The modulated input data using orthogonal subsidiary companies , with carrier frequency 70MHz. After contaminating the signal with noise , and re- sampling - the received signal and convert it to a digital system to extract the original information . Results obtained tend to increase in the signal to noise ratio , and improve the planned constellation of the received signal and bit error rate (BER) of the system decreases to zero when the S / N ratio greater than 12dB. FPGA to implement a complete SIMULINK model first and then generate HDL code and DSP design tool from XILINX, and the results will be obtained from MATLAB and FPGA be approximately equal .

Index Terms— OFDM, Software Defined Radio, MATLAB-SIMULINK.

I. INTRODUCTION

OFDM is multi-carrier transmission technique that divides the available spectrum into subcarriers, with each subcarrier containing a low rate data stream. The subcarriers be appropriate spacing and shape of the band -pass filter to meet orthogonal . Compared with the traditional system of parallel data , frequency division multiplexing (FDM), where the guard band is necessary between subcarriers which results in inefficient use of the spectrum , uses OFDM spectrum overlapping orthogonal subcarriers , leading to the effective use of the spectrum [1] . Thus, OFDM can be considered as an issue of spectrally efficient FDM. OFDM system uses the inverse Fourier transform separate (IDFT) of the process of formation , and the temporal pulse shape of a single icon is a rectangle . This results in the form of a Fourier transform of the signal on each subcontract with a large side lobes due to the frequency response of the filters that distinguish sub- channels . However , as long as the receiver are synchronized with each other , and sub- channels perpendicular to each other and overlap caused insignificant . Multi- carrier modulation , such as OFDM, and spread widely in the reception of data at high speed , DSL [2]. IEEE802.11a [3], standards IEEE802.11g [4], IEEE802.16a [5], and because of its ability to deal with the efficiency of the distortion introduced by frequency selective fading channels [6] . It is clear from the structure of the global processor computing restructuring in SDRs in Figure 1. SDR Radio software is where all the layers of material are programs that define the region and effectively used in FPGA [9-10-11-12-13].

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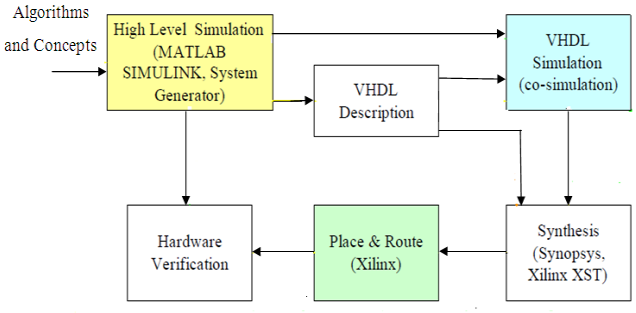


Figure (1): Universal structure of reconfigurable computing processor in SDR technology

II. OFDM MODEL BASED-SDR

A basic OFDM model based on SDR is proposed and modeled using MATLAB. The goal of the simulation is done to measure the performance of the system under the influence of OFDM signal to noise ratio degrees. The proposed model which is shown in Figure 2 is to send and receive modulated IF signal OFDM.

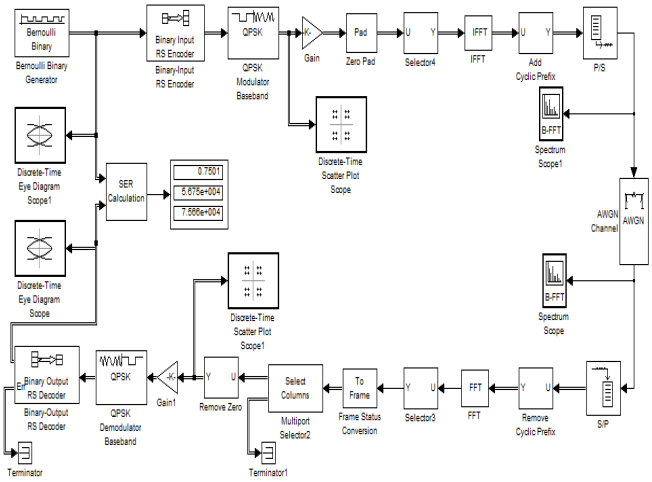


Fig.(2): Proposed Basic OFDM Model Based on SDR

2.1- Data Generation

Due to the use of dual RS encoder input in this form, and must be based on the input data frame column vector and this can be achieved by using the Bernoulli binary generator to generate a framework based on the data stream with the following parameters:

- probability of zero = [0.5]
- initial seed = 1234567
- sample time = 4e-6/44/7
- sample per frame = 44
- frame based output.

The reason for choosing the frame-based because of the high efficiency, rate, capacity,laten- cy, and a good spread in real time. A modulator converts a set of bits in the number corresponding to the complex constellation signal. Modification system depends on the sub-carrier. A sub-carrier with high SNR will be assigned more bits than a sub-channel with low SNR. Modulation implemented here is QPSK.

2.2- Choise OFDM Parameters

The choice of various OFDM parameters is tradeoff between various, often conflicting requirements .Usually there are three main requirements to start with:

- Bandwidth
- Bit rate
- Delay spread

The delay spread directly decades the guard time. As a rule, the guard time should be about two to four times the root-mean-squared delay spread. This value depends on the type of coding and QAM modulation. Higher order QAM (like-64QAM) is more sensitive to the (ISI) than QPSK, while heavier coding obviously reduces the sensitivity to such interference. Since the guard time has been set, the symbol duration can be fixed. To minimize the signal-to-noise ratio (SNR) loss caused by the guard time, its desirable to have the symbol duration much larger than the guard time. It cannot be arbitrarily large however, because large symbol duration means more subcarrier with smaller subcarrier spacing, a large implementation complexity, and more sensitivity phase offset and frequency offset as well as an increased peak-to-average power ratio. After the symbol duration and guard time are fixed, the number of subcarriers can be determined by inverse of the useful symbol duration (symbol duration – guard time) .Alternatively, the number of subcarriers may be also determined by the required bit rate divided by bit rate per sub-carrier. The bit rate per subcarrier is defined by the modulation type (i.e 4QAM) coding rate and symbol rate. An additional requirement that can affect the chosen parameters is the demand for an integer number of samples both within the FFT/IFFT interval and in the symbol interval [7],[8]. For the details mentioned above we can calculate each parameter for the model. We have the main requirements.

B.W=1MHz , Bit rate = 20Mbps , Delay spread = 200ns

Then

-Guard time = 4(Delay spread) = 4 x 200 =800ns.

-Symbol duration = (guard time) = 6 x 800 =4.8 us

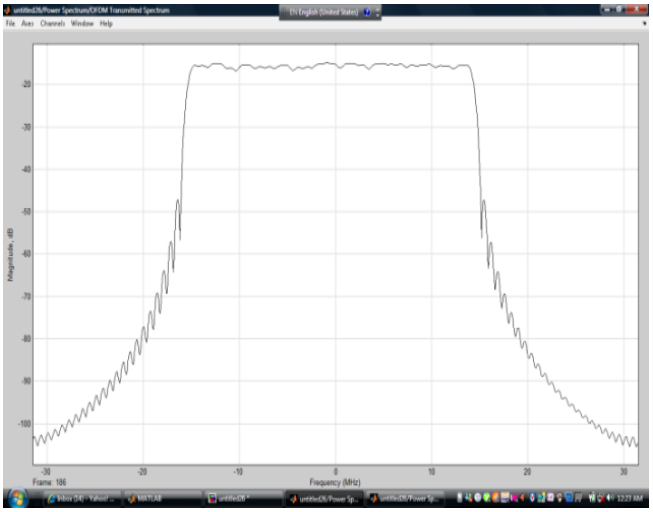
-Useful symbol duration = symbol duration – guard time = 4.8 – 0.8 = 4 us

-Subcarrier spacing = 1 / useful symbol duration = 1/4 = 250 KHz

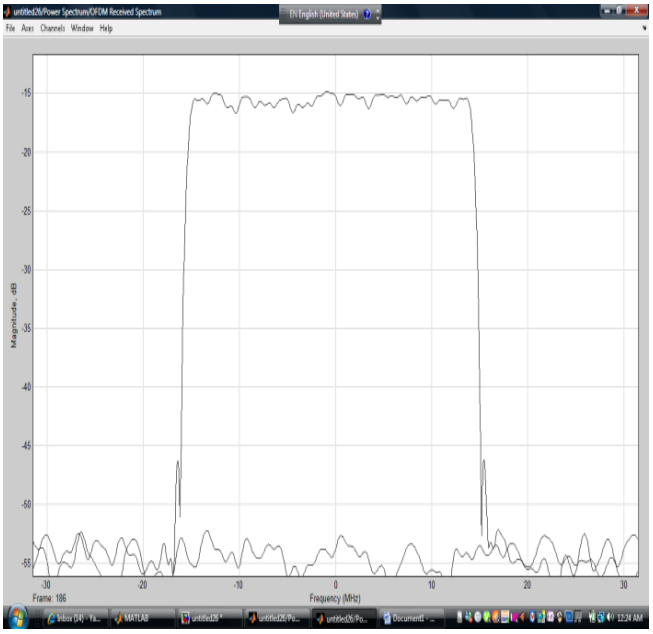
-Information bit =Bit rate x symbol duration = 20x 4.8 = 96 bits

-Subcarriers = B.W / subcarrier spacing = 16 / 250 = 64

So, QPSK with rate ¾ or pi/4 which give 2bit/symbol/ subcarrier. The numerical values for OFDM parameters used in the model are given in Table(1) and the transmit / received power spectrum is show in Figure 3 and Figure 4.



Fig(3): transmit power spectrum



Fig(4):Received Power Spectrum

Table (1) : OFDM parameters of the simulated model

Parameters	Values
Bit rate	20Mbps
Delay spread	200ns
Bandwidth	16MHz
Guard time	800ns
Symbol duration	4.8 μs
UsefulKsymbol duration	4 μs
Subcarrier spacing	250KHz
Subcarriers	64
Modulation type	QPSK
Channel model	AWGN

2.3- Bit Error Rate (BER) of The Model

Bit error rate simulation for small values of SNR slightly above the theoretical probability curve. As is increased SNR, and intersects the error rate simulation code and then fall to less than the theoretical error vector. We gave several examples of different modulated as in Figure 5 .

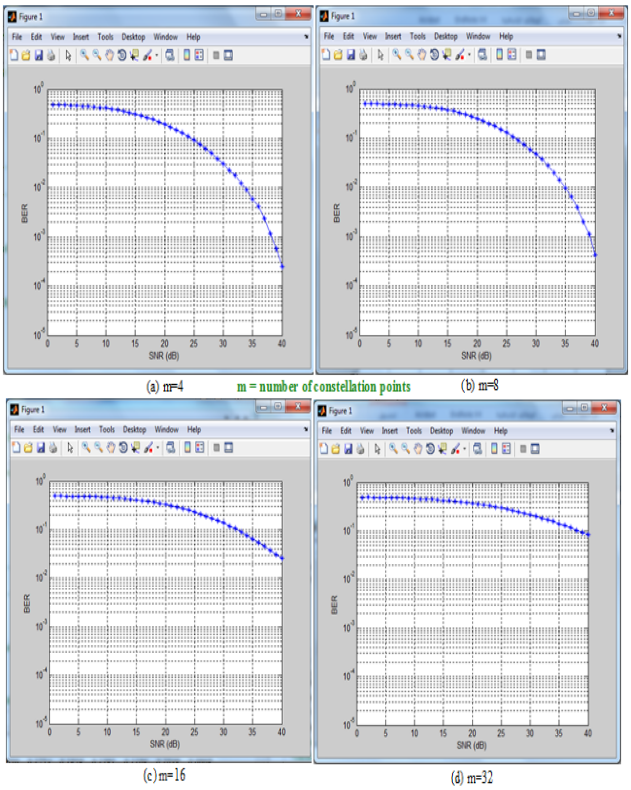
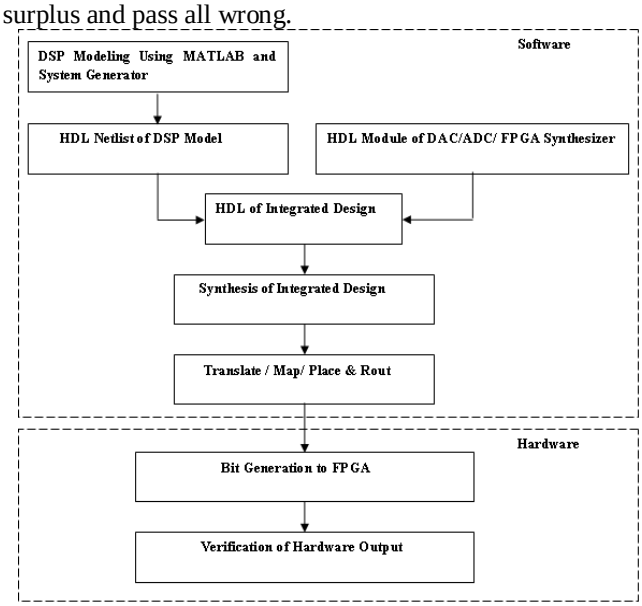


Fig.(5): BER for proposal model with different type of modulation.

III- OFDM IMPLEMENTATION

The OFDM model is implemented using system generator and DSP design tools from Xilinx to ensure the simulation results as well. Uses a flow chat to FPGA implementation is shown in Figure 6 is associated with programs from XILINX. After the model was designed in floating point values using MATLAB, and the design of a model based on the birth of the system in terms of the values of a fixed point in order to generate the hardware description language (HDL) VHDL or pattern Verilog synthesis and synthesis of this language to FPGA Vertix-4 using XILINX ISE program of the bit stream generation after translate and map the location and processing of defeat. Timing constraint has been developed FPGA board and chip rate and arranged to overcome the surplus and pass all wrong.



Figure(6): FPGA design flow of Proposed OFDM model.

Synthesis output files required by the software XILINX ISE in EDIF (file interface electronic design) and UCF (User constraints file) formats, which represents the synthesized netlist optimally integrated design, and timing constraints and FPGA pin assignment, respectively. To implement the design synthesized in VIRTEX-4 Development Board FPGA, XILINX ISE perform the following steps as shown in Figure 7.

Netlist conversion of integrated design in the form of EDIF 's NGD (in the original database) file that contains a description of the logical components of the hierarchy and priorities using the XILINX NGD Build. Logical DRC (Design Rule Check) on file NGD, and then assign the design logic chipset and I / O cells in VIRTEX-4 FPGA to create the original circuit description (NCD) file. Restrictions area can be sized correctly using the PACE (restrictions pin from the editor) , and then restart the map. Place and route the design in the appointment of a file in NCD VIRTEX-4 FPGA based on timing constraints by using timing analysis tools . The pipe is full file NCD. File translation NCD fully oriented to form a bit stream (. BIT) file using the program Bit Gen. Finally , download the file bit stream in VIRTEX-4 via cable JTAG FPGA using the program impact.

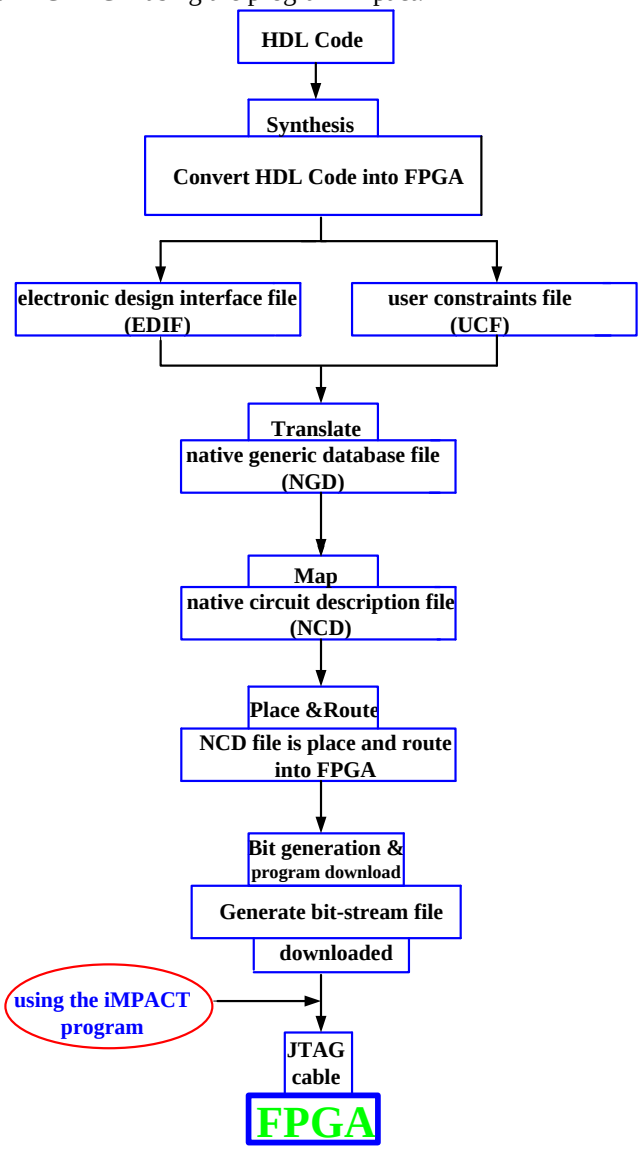


Figure (7): FPGA Implementation steps.

Program ISE put all LUTs needed close to each other to spread the minimum of data, that some of the terminals within the slice is not used in some slice uses FFS only, without terminals , the number of LUTs can not be counted manually , and thus can LUTs be less or more of the segments depend on software optimization. Summary of use of the device that has been created by the ISE represents the elements available in the FPGA logic elements and logic used by the project at hand is designed . Is calculated by the percentage of logic elements used for the logic elements available as follows:

$$\frac{\text{used logic elements}}{\text{available logic elements}} X\ 100$$

For example:
Utilized number of Slice Flip Flop =(392/30720) x 100 = 1%
Utilized number 4-input LUTs =(280/30720) x 100 = 0.9%
Utilized number of occupied Slices =(370/15360) x 100 = 2%
Utilized number of bonded IOBs =(300/353) x 100 = 84%

The results were obtained from the system shown in figure 8.

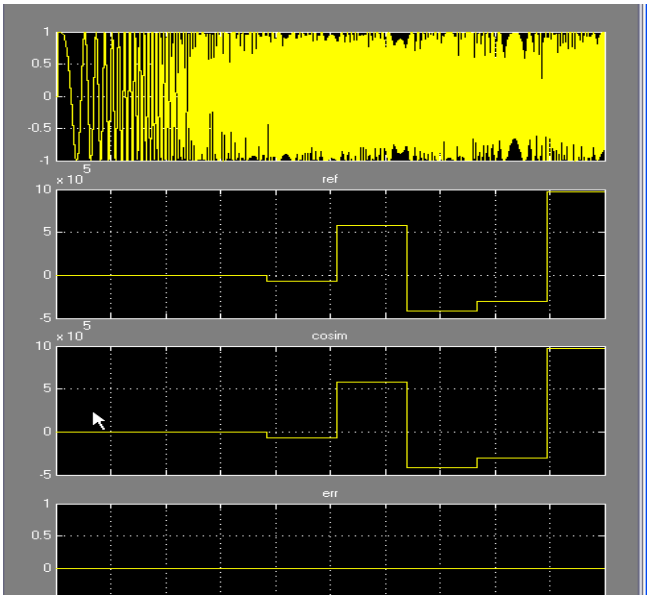


Fig.(8). Results from the system

IV. CONCLUSION

Proposed Model, submit a new application of the system of OFDM, and bit error rate (BER) of the system stands affected has not changed snapshot factors less than approximately 6DB, 10dB output for 16PSk, QPSK, respectively, and peak power to RMS ratio independent on the type of modulation used in the system. The results obtained showed that for 3 different types of modulations (QPSK and 16PSK), does not respond to the system based on the SDR OFDM any delay less than the guard interval. Performance is improved in terms of the delay spread OFDM system based on special drawing rights because of the extension period League (256 samples) and not periods of zero padding.
For FPGA implementation first complete simulink model and then generate the HDL code using system generator and DSP design tool from Xilinx. The results obtained from MATLAB and FPGA were equal and this proves that the simulation in Matlab gave good results in the FPGA and the proposed system works successfully.

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