Gate Driver with Output Having Positive Triple Input Voltage and Negative Double Input Voltage

K. I. Hwu, Y. T. Yau

Abstract—This paper presents a gate driver, whose output possesses the positive triple input voltage and the negative double input voltage under only one positive-voltage source required. Such a gate driver can reduce the transient period of the gate driver and hence can reduce the corresponding switching loss. In addition, since double the negative input voltage is imposed on the input of the power switch during the turn-off period, not only the error in triggering the switch due to the Miller effect can be reduced, but also the leakage current can be reduced. The detailed operating principles are illustrated and some simulated and experimental results are provided to verify the effectiveness of the proposed scheme.

Index Terms—Gate driver, leakage current, switching loss.

I. INTRODUCTION

As generally acknowledged, the switching loss of the MOSFET power switch takes an important role in the total loss. This is because the MOSFET power switch exhibits the resistive property during the transient period of turn-on/off. The more the switching frequency is, the more the loss. Consequently, if the transient period is reduced, then the switching loss can be decreased significantly. As generally recognized, the gate of the MOSFET power switch can be regarded as a capacitor. Since the traditional positive-output-voltage gate driver for the n-channel MOSFET power switch is powered only by the positive-voltage source, the gate of n-channel MOSFET power switch is not driven enough fast during the turn-off period and hence the switching loss is increased.

In order to reduce the switching loss mentioned above, one way is to apply the resonant concept to the gate driver [1]-[7]. However, the resonant circuit used will increase the cost and complexity. And, another way is to apply both positive and negative output voltages to driving the n-channel MOSFET power switch [8], so as to shorten the discharge time of the gate of the n-channel MOSFET switch during the transient period of turn-off. However, in this case, not only one positive-voltage source but also one additional negative-voltage source is required to drive the n-channel MOSFET power switch, and this is inconvenient in industrial applications. In addition, such a gate driver can also be applied to driving the p-channel MOSFET power switch.

Consequently, in this paper, a novel gate driver is presented, whose output has the positive triple input voltage and the negative double input voltage under only one positive-voltage source fed.

Furthermore, this driver has the same ground reference for input and output ports. And hence, such a gate driver is easy to implement and would drive the MOSFET power switch fast. Moreover, this gate driver can be applied to driving the n-channel MOSFET power switch as well as the p-channel MOSFET power switch. And, during the turn-off period the negative voltage applied to the input of the n-channel MOSFET power switch or the positive voltage applied to the input of the p-channel MOSFET power switch can reduce the leakage current, thereby causing the energy loss to be decreased, and besides the error in triggering the switch due to the Miller effect can be reduced. In summary, the proposed gate driver is very convenient in industrial applications. The following are operating principles to be illustrated and some simulated and experimental results to be offered, so as to verify the effectiveness of the proposed circuit topology.

II. CIRCUIT TOPOLOGY FOR THE PROPOSED GATE DRIVER

The circuit for the proposed gate driver is presented in Fig. 1. This circuit with one positive-voltage source required, used to source the gate of the MOSFET power switch or to sink the gate of the MOSFET power switch, is mainly constructed by one half-bridge circuit containing one p-channel MOSFET Q1 and one n-channel MOSFET Q2. Moreover, there are four charge pump cells in the circuit. The first charge pump cell is constructed by one capacitor C1 and one diode D1, the second charge pump cell is built up by one capacitor C2 and one diode D2, the third charge pump is composed of one capacitor C3 and one diode D3, and the fourth charge pump is established by one capacitor C4 and one diode D4. Since in this paper, the MOSFET power switch is of n-channel, the gate of the n-channel MOSFET power switch is modeled by one capacitor Cgs. Hence, these four charge pump cells are used to boost up the positive/negative voltage across Cgs. Furthermore, there are two voltage-clamping circuits which are used to control the level of the output voltage, positive or negative. One is constructed by one capacitor C1 and one diode D1; the other is built up by one capacitor C4 and one diode D4. The selection of the current direction, responsible for the path of charging or discharging of the gate of the MOSFET power switch, is controlled by one p-channel MOSFET Q1 and one n-channel MOSFET Q4. By the way, the signal PWM is a control signal fed to the proposed gate driver.

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119
III. OPERATION PRINCIPLES OF THE PROPOSED GATE DRIVER

Prior to taking up this section, it is assumed that the forward voltages for all the diodes are zero, the voltages across C1 and C2, \( v_{C1} \) and \( v_{C2} \), are both almost equal to \( V_{CC} \), the voltages across C3, C4 and C5, \( v_{C3} \) and \( v_{C4} \) and \( v_{C5} \), are all almost equal to \( 2V_{CC} \), and the voltage across C6, \( v_{C6} \), is almost equal to \(-V_{CC} \). There are two operating modes for the proposed gate driver to drive the gate of the n-channel MOSFET power switch, modeled by \( C_{gs} \).

A. Mode 1

As shown in Fig. 2, Q1 is turned on but Q2 is turned off. Therefore, D2 is forward biased and C2 is abruptly charged to \( V_{CC} \). At the same time, the input voltage \( V_{CC} \), together with the voltage across C6, charges \( C_6 \) to \( 2V_{CC} \). In addition, since D1 is reverse biased, the voltage across C1, together with \( V_{CC} \), charges \( C_1 \) to \( 2V_{CC} \). On the other hand, the voltage between the gate and source of Q3, \( V_{gs3} \), is \(-V_{CC} \), thereby causing Q3 to be turned on, whereas the voltage between the gate and source of Q2, \( V_{gs2} \), is zero, thereby causing Q2 to be turned off. Hence, \( V_{gs} \) is equal to \( 3V_{CC} \).

B. Mode 2

As shown in Fig. 3, Q1 is turned off but Q2 is turned on. Therefore, D1 and D4 are forward biased whereas D2 and D4 are reverse biased. By doing so, \( C_1 \) is charged to \( V_{CC} \). At the same time, the voltage between the gate and source of Q3, \( V_{gs3} \), is zero, thereby causing Q3 to be turned off, whereas the voltage between the gate and source of Q4, \( V_{gs4} \), is equal to \( V_{CC} \), thereby causing Q4 to be turned on. On the other hand, \( C_1 \) is charged to \( V_{CC} \) whereas \( C_3 \) is charged to \( 2V_{CC} \). Hence, \( V_{gs} \) is equal to \(-2V_{CC} \).

IV. SIMULATED AND EXPERIMENTAL RESULTS

Before this section is taken up, there are some specifications to be given as follows: (i) \( V_{CC} \) is set at 5V; (ii) the values of \( C_1, C_2, C_3 \) and \( C_6 \) are all set at 10μF; (iii) the values of \( C_3 \) and \( C_4 \) are both set at 1μF; (iv) the value of \( C_{gs} \) is chosen to be 22nF; (v) the output buffer switches named IXDD414P are used as \( Q_1 \) and \( Q_4 \); (vi) the product name of \( Q_2 \) and \( Q_3 \) is FDS8333C containing one n-channel MOSFET and one p-channel MOSFET; and (vii) the product name of \( D_1, D_2, D_3, D_4, D_5 \) and \( D_6 \) is 1N5819.

The following simulated results shown in Figs. 4 and 5 are based on Fig. 1 at the switching frequencies of 10kHz and 500kHz, respectively. Afterwards, under the same conditions, the experimental results are shown in Figs. 6 and 9. It is obvious that the output voltage of the proposed gate driver has the triple input voltage and the negative double input voltage to drive the n-channel MOSFET power switch under the proposed gate driver with only one positive-voltage source required.

![Fig. 1. Proposed gate driver.](image)

![Fig. 3. Power flow of the proposed gate driver with \( C_{gs} \) discharged.](image)

![Fig. 2. Power flow of the proposed gate driver with \( C_{gs} \) charged.](image)

![Fig. 4. Simulated results at the switching frequency of 10kHz: (1) PWM; (2) \( V_{x1} \); (3) \( v_{x1} \); (4) \( V_{gs3} \); (5) \( v_{gs3} \); (6) \( V_{c3} \); (7) \( v_{c3} \); (8) \( V_{c5} \); (9) \( v_{c5} \); (10) \( V_{c6} \); (11) \( v_{c6} \).](image)
V. CONCLUSION

In this paper, a novel gate driver with a single positive-voltage source offers the output with the positive triple input voltage and the negative double input voltage to drive the MOSFET power switch. For such a gate driver, if the negative voltage is used to drive the n-channel MOSFET power switch during the turn-off period, then the transient period of turn-off is reduced and hence the switching loss can be decreased. Aside from this, during the turn-off period, the negative voltage applied to the n-channel MOSFET power switch or the positive voltage applied to the p-channel MOSFET power switch can reduce the leakage current, thereby causing the energy loss to be decreased, and besides the error in triggering the switch due to the Miller effect can be reduced.

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