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Low power Transceiver Structure for Wireless and Mobile Systems Based SDR Technology Using MATLAB and System Generator

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Abstract*— This paper presents the design and implementation of Software Defined Radio (SDR) transceiver based 16-QAM as one of the key techniques in structure of wireless and mobile communication system. The widely used of QAM in adaptive modulation due to efficient power and bandwidth force the researchers to found better and easy design by use the available software like MATLAB in order to advance the idea of software defined radio. The setting of parameter for random generator, QAM modulation and demodulation, AWGN wireless channel are provided. The Error rates of QAM system against the signal-to-noise ratio are used to evaluate the QAM system. The implementation results shows the system capability to transmitand receive intermediate frequency of 40 MHZ keeping the power under limited FPGA Slices and look up table (LUT).

Index Terms*— SDR, QAM, MATLAB SIMULINK, Wireless and Mobile System, FPGA.

I. INTRODUCTION

The rapid growth and development of modern communication system, state for reliable high data rate transmission, which stimulate much interest in modulation techniques. To send different bits per symbol and achieve different throughputs, different modulation technique should be used. One of widely used modulation is QAM due to its efficient in power and bandwidth [1-2]. Tow amplitude modulated signals are combined into a single channel in QAM system so duplicate the effective bandwidth. Though, it also be noted that when a modulation technique such as 64-QAM, better signal to noise ratios are needed to overcome any interference and maintain a certain bit error rate [2]. The use of adaptive modulation can increase the transmission rate considerable by matching modulation schemes to time varying channel conditions, which justifies its popularity for future high-rate wireless applications [3-4]. Crucial to adaptive modulation is the requirement of channel state information at the transmitter. A general estimate of the channel state information for different modulation techniques is provided. As you increase your range, you step down to lower modulations (in other words, QPSK), but as you are closer you can utilize higher order modulations like QAM for increased throughput. In addition, adaptive modulation allows the system to overcome fading and other interference [5]. Both QAM and QPSK are modulation techniques used in IEEE 802.11 (Wi-Fi), IEEE 802.16 (WiMAX), and 3G (WCDMA/HSDPA) wireless technologies [5].

The modulated signals are then demodulated at the receiver where the original digital message can be recovered. The use of adaptive modulation allows wireless technologies to optimize throughput, yielding higher throughputs while also covering long distances [6]. To better understand the QAM system, a MATLAB/Simulink-based simulation system is designed in this paper. In the simulation model, the parameter settings for random generator, QAM modulation and demodulation, AWGN wireless channel are provided. Error rates of QAM systems versus the SNR are used to evaluate the QAM system for adaptive modulation. The model can be used not only for the criteria of adaptive modulation but also for a platform to simulate other modulation techniques. The MATLAB program along with system generator could be used to simulate the proposed model and ISE software is used as synthesis tool to implement the transceiver scheme in FPGA. The Xilinx system generator provide a bit accurate of FPGA and automatically generate the bit stream of the Netlist design [7-8-9-10-11-12]. The VHDL design can be used for implementation of the design process as illustrated in Figure 1 [13-14-15].

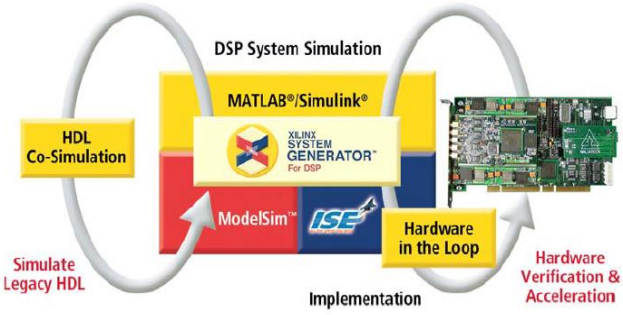

Figure 1: FPGA test-bed implementation process [8].

II. SDR SIMULINK MODEL

The IF and baseband sections of the transmitter and receiver have been designed and simulated using the MATLAB SIMULINK block set to facilitate the analysis of the proposed model performance under channel noise. In the first step, the transmitter part consists of modulation, up-sampling, and pulse-shaping filter, and the receiver part comprises pulse shaping, down-sampling, and demodulation, which have been designed and simulated according to the model shown in Figure 2.

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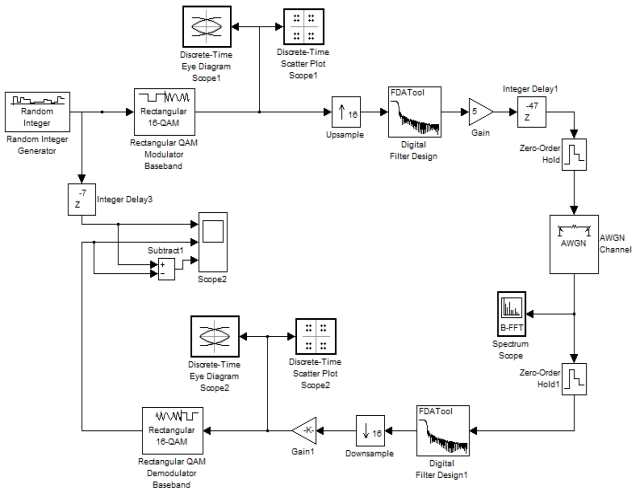

Figure 2. : SDR Transceiver SIMULINK Model

2.1. *Transmitter Design*

In the transmitter, the generated signal from the random integer generator is modulated by the 16-QAM modulator, which has a symbol rate of 2.5 M symbol/s. The ideal eye diagram of the generated 16-QAM baseband signal is shown in Figure 3, whereas the constellation diagram is shown in Figure 4. The modulated signal is subsequently up-converted by a factor of 16 and pulse-shaped by the Root Raised Cosine (RRC) filter.

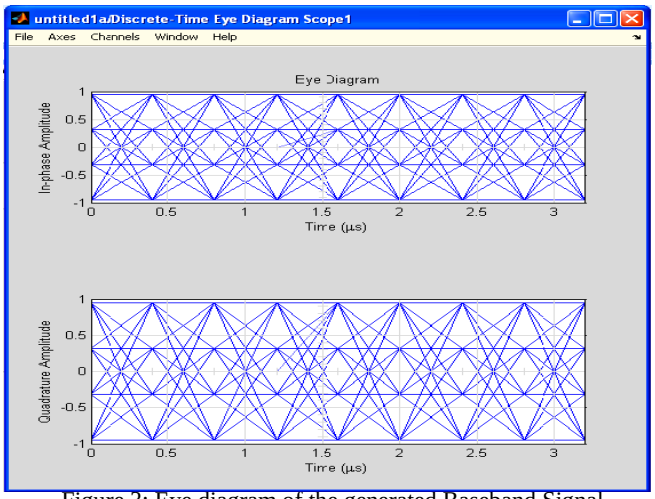

Figure 3: Eye diagram of the generated Baseband Signal

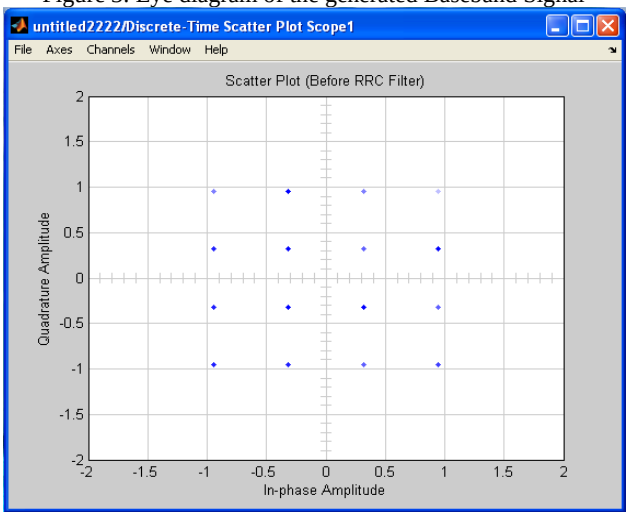

Figure 4: Constellation diagram of the generated Baseband Signal.

2.1.1. Interpolation (Up-Sampling)

Generally, it is useful to modify the effective variety speed of an existing sampled signal. A sample rate of a signal is increased by interpolation. Conceptually, interpolation comprises the generation of a continuous curve passing through old samples, followed by sampling the curve at the new sample rate to obtain the interpolation sequence. To increase a given sample rate or up-sample, a factor of M, M-1 intermediate values between each samples in the old signal, has to be calculated. The interpolation increases the sampling frequency (Fs) to:

$$f_s = f_{new} = Mf_{old} \quad (1)$$

For the proposed system, the 16-QAM baseband signal is up-sampled by a factor of 16 to produce a new sample rate of 40 M symbol/s. The interpolation process produces inherent amplitude loss factor of M. This loss factor is compensated by adding gain stage in the system to achieve unity gain between the old and the new sequences.

2.1.2. Pulse Shaping (Root Raised Cosine Filter)

The core of any wireless communication system is the use of transmitter and receiver pulse shaping filters. The requirements of Root Raised Cosine filter (RRC) is shown in Table 1.

Table 1: Design Requirement of Root raised cosine Filter.

Centre frequency f_{centre}	2.5 MHz
Sampling rate	40 MHz
Stop-band attenuation	-40 dB
Roll-off factor β	0.35
Phase Response	Linear
Stability status	Stable

In order to achieve these requirements, a FIR filter using Kaiser Window is chosen to design the filter. There are three significant frequency points associated with the raised cosine response. The first is known as the Nyquist frequency, which is equal to the centre frequency. The second significant frequency point is the stop band frequency (f_{stop}), defined as the frequency at which the response first reaches zero magnitude. The third, and the final significant frequency point is the pass band frequency (f_{pass}) defined as the frequency at which the response first begins to depart from its peak magnitude.

$$f_{stot} = (1+\beta)f_{center} = (1+0.35)X\ 2.5MHz = 3.375MHz \quad (2)$$

$$f_{pass} = (1-\beta)f_{center} = (1-0.35)X\ 2.5MHz = 1.625MHz \quad (3)$$

The magnitude and impulse responses of RRC filter are shown in Figure 5 and Figure 6 respectively. The characteristics of the filter indicate that the filter is non-distorting.

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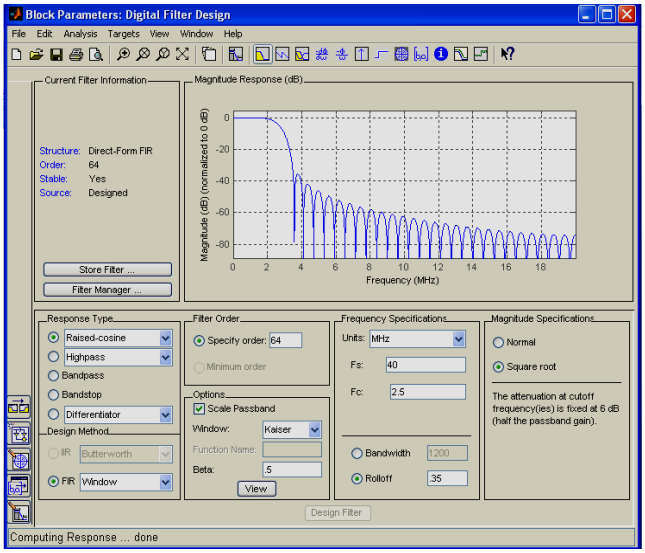

Figure 5: Magnitude response RRC filter.

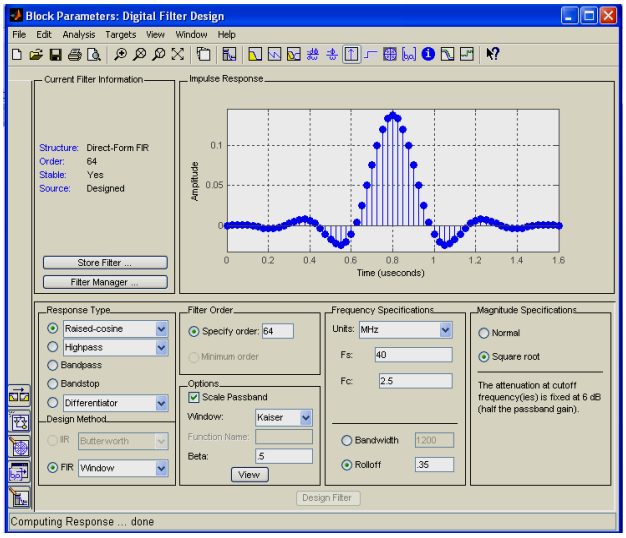

Figure 6: Root Raised Cosine Filter impulse response.

The original spectrum of the baseband signal is processed under the 20dB AWGN channels as shown in Figure 7. The power of the baseband magnitude signal is 2.5dB.

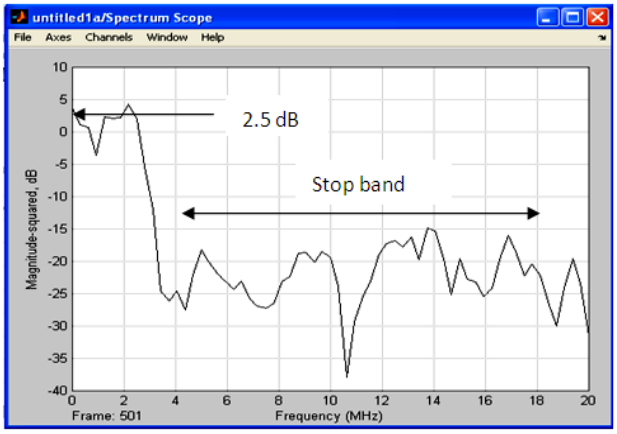

Figure7:Original baseband Signal

1.2. Receiver Design

After the signal is tainted by noise, its down converted to IF in the receiver path. The receiver link accepts data streams from AWGN channel which are processed under the 20-dB SNR. The IF received signal is pulse shaped when using RRC filter with sample rate of 40MHz, and the received signal is decimated by a factor of 16. The decimation process produces an inherent amplitude loss from the received signal, and this loss is compensated by adding gain stage in the system to achieve unity gain between new and old sequence. The filtered and fine-gained signals are down-sampled to become symbol-pairs before demodulation. The eye and constellation diagram of received signal is shown in Figure 8 and Figure 9.

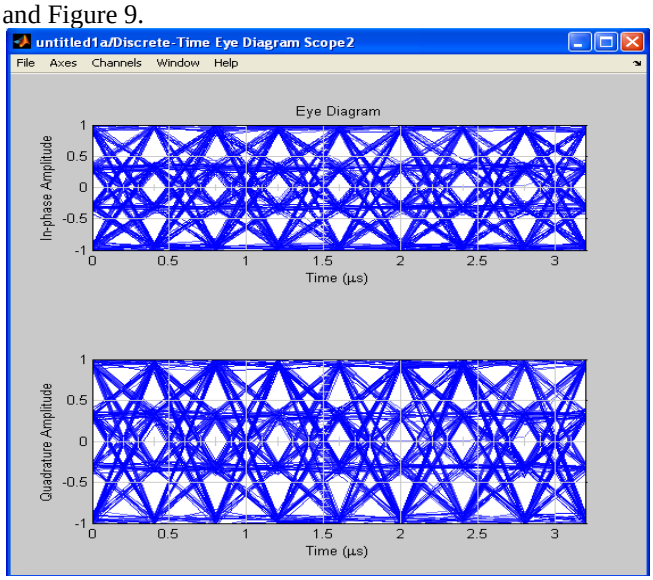

Figure 8: Eye diagram of 16-QAM received signal.

If one makes a look at the received signal, the signal is affected by noise effect with SNR of 20 dB. When the SNR increased to 30 dB, the noise margin start to close out and the error is decreased in eye diagram. Since, the SNR decrease to 10 dB, the eye diagram has more distortion in the system. Figure 9 shows the eye and constellation diagrams of the receiver signal when SNR = 30 dB. The eye diagram reveals less distortion given that the eye opening is more defined. The correct eye results and less bit error and hence, less transmission error. Comparison between Figure 9, Figure 10 and Figure 11 demonstrates clearly that the cause of the difference is the increase of SNR in the channel.

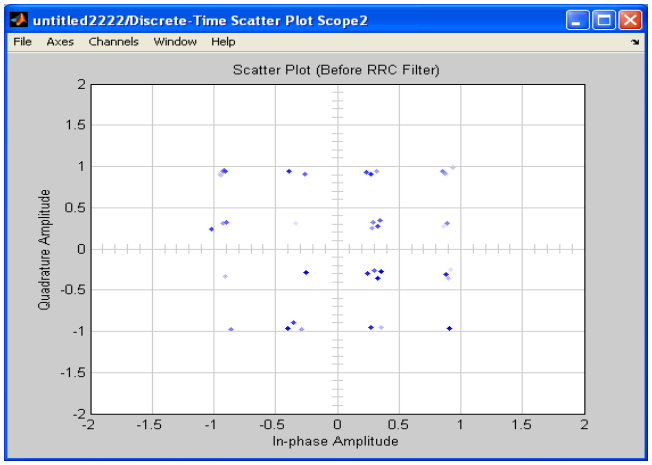

Figure 9: Constellation diagram of 16QAM Received signal with 20dB

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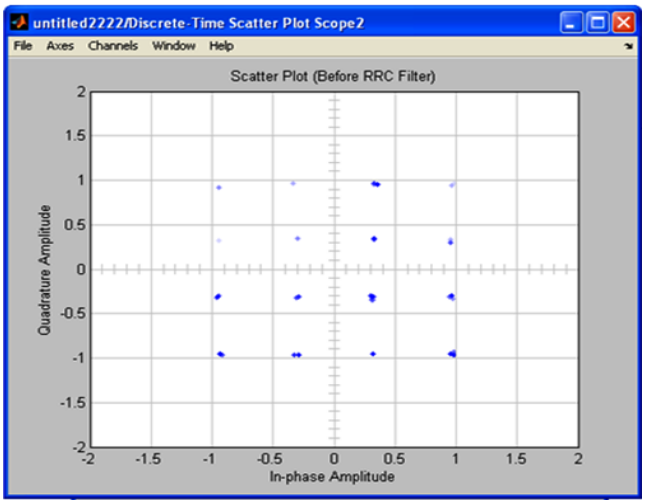


Figure 10: Constellation diagram of the Received signal at 30dB

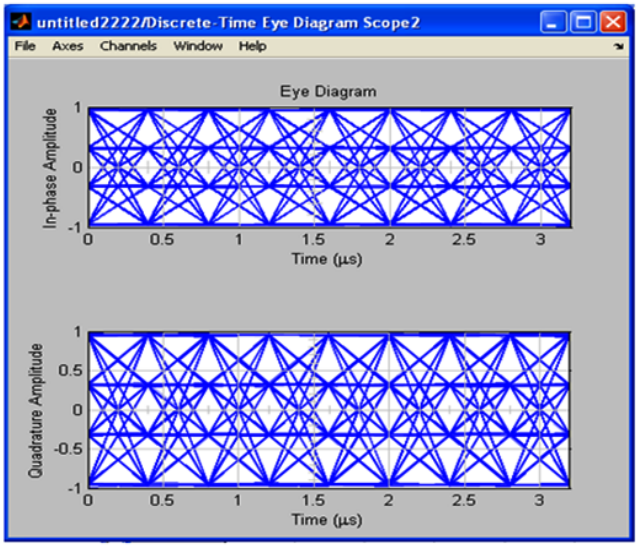


Figure 11: Eye diagram of the Received signal at 30dB

Figure 12 shows the input and output waveforms of the transmitter and receiver model. The received IQ signals are filtered and fine-gained to convert them into refined IQ signals. Subsequently, the signals are synchronized and down-sampled by a factor of 16 to become baseband IQ symbols (2.5mega-baud). After demodulation, the recovered 4-bit integers (2.5mega-baud) are compared with the transmitter input to confirm all system functions. The difference between the original message 4-bit integer and receiver output 4-bit integer is zero.

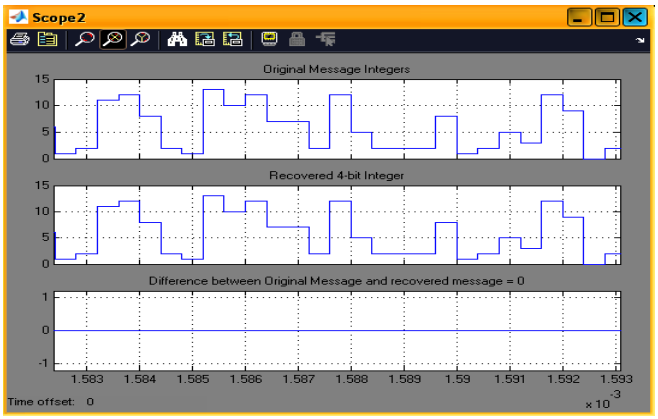


Figure12: Transmitter Input signal and Receiver Output Signal

II. FPGA IMPLEMENTATION

The generalized implementation flow chart of SDR transceiver model design is shown in Figure 13. The software part of all stages is illustrated clearly according to FPGA applications [16-17]. The FPGA is used here for the soft reconfigurable and DSP will control the FPGA and other data flow task.

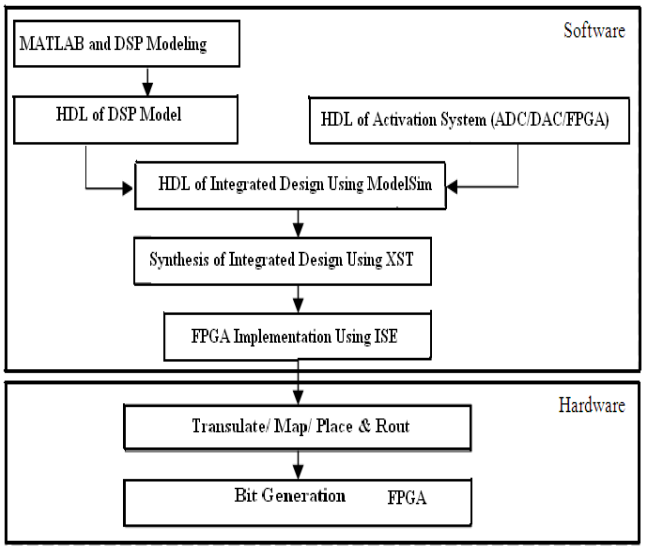


Figure 13: Proposed flow chart of Design and Implementation

Due to the accessibility of enormous parallelism and partial reconfigure ability of FPGA we have proposed the flow chart shown in Figure 13 which in turn reduces the total resource utilization and hence the power consumption and speed. The developments of configurable of SDR are described in detailed. Generally, the flow of design and implementation can be divided into 2 parts namely software and hardware. Each stage in the general flow of design and implementation will be detailed below. The first stage in the general flow of design and implementation is modeling the configurable transciever of SDR using digital signal processing (DSP) algorithms in high level graphical user interface (GUI) [18-19-20]. In this work, the high level GUI is Simulink environment contained in MATLAB software with add-in of Xilinx System Generator software. All DSP models contained in the transcievers are built by connecting the blocks provided by libraries of Simulink Blockset and Xilinx Blockset in this GUI. The synthesis output files generated by the ISE software in electronic design interface file (EDIF) and user constraints file (UCF) forms represent the optimized netlist of integrated design, timing constraints, and FPGA pin assignment that have been implemented into the FPGA development board by following the steps listed below:

- Translate: Convert the netlist file of integrated design in EDIF format to native generic database (NGD) file, which contains logic description of hierarchical components and Xilinx primitives for the integrated design using NGD build program.
- Map: Perform logical DRC on the NGD file and map the design logic to slices and input-output (I/O) cells in FPGA to create native circuit description (NCD) file.

- Place and Route: The design in mapped NCD file is place and route into FPGA based on timing constraints using timing analysis tools with no errors found. All signals are completely routed for transmitter and receiver, respectively.
- Bit generation and program download: Bit generation is used to generate configuration bit-stream file in BIT format form, and subsequently downloaded into FPGA via JTAG cable using the iMPACT program.
- The timing requirement is satisfied as shown in the post-PAR (final) static timing report as shown in Tables 2 and Table 3.

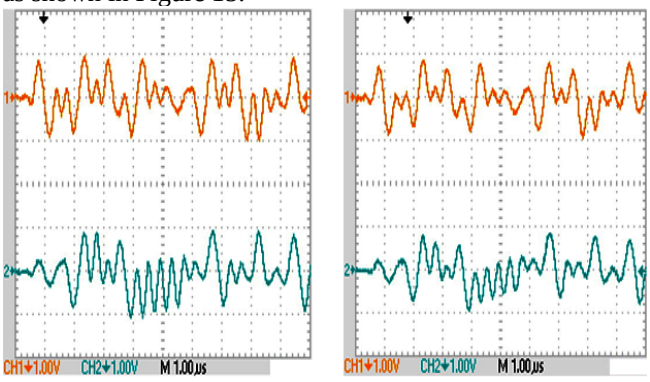
Starting Clock	Requested Frequency	Estimated Frequency	Requested Period	Estimated Period	Slack
CLK_100	100.0 MHz	189.4 MHz	10.000	5.280	4.720
LIO_CLKIN_1	80.0 MHz	218.7 MHz	12.500	4.573	7.927
System	100.0 MHz	511.8 MHz	10.000	1.954	8.046

Table 2: Post-PAR Static Timing Report for 16-QAM Transmitter

Table 3: Post-PAR Static Timing Report for 16-QAM Receiver

Starting Clock	Requested Frequency	Estimated Frequency	Requested Period	Estimated Period	Slack
CLK_100	100.0 MHz	189.4 MHz	10.000	5.280	4.720
LIO_CLKIN_1	80.0 MHz	134.1 MHz	12.500	7.456	5.044
System	100.0 MHz	216.6 MHz	10.000	4.617	5.383

The ADC input and DAC output signals in P240 Analog Module for the SDR transmitter and receiver are connected to oscilloscope in order to display real-time result, as shown in Figure 14. Transmitted I/Q and received I/Q signals should be similar, although noise effect and distortion may occur (real-world application issue). It should be noted that the empirical (real-time) result is identical to the simulated result, as shown in Figure 15.



(a) Transmitted (IQ) (b) Received (IQ)

Figure 14: Real time Transmitted/ Received (IQ)16-QAM

The transmitter and receiver project status and device utilization summary are reported by the ISE program, as shown in table 4 and table 5. These tables provide the total number of slices and LUTs used in this design, which represent the total area used in FPGA. Depending on the number of devices used in FPGA , the total power consumption in the transmitter,s implementation can be seen , according to the number of slices and LUTs.

Table 4: Transmitter utilization summary

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	442	30,720	1%	
Number of 4 input LUTs	295	30,720	1%	
Logic Distribution				
Number of occupied Slices	353	15,360	2%	
Number of Slices containing only related logic	334	353	94%	
Number of Slices containing unrelated logic	19	353	5%	
Total Number of 4 input LUTs	436	30,720	1%	
Number used as logic	295			
Number used as a route-thru	11			
Number used as Shift registers	130			
Number of bonded IOBs	61	448	13%	
Number of BUFG/BUFGCTRLs	4	32	12%	
Number used as BUFGs	4			
Number used as BUFGCTRLs	0			
Number of FIFO16/RAMB16s	8	192	4%	
Number used as FIFO16s	0			
Number used as RAMB16s	8			
Number of DSP48s	12	192	6%	
Total equivalent gate count for design	539,143			
Additional JTAG gate count for IOBs	2,928			

Table 5: Receiver utilization summary

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	11,345	30,720	36%	
Number of 4 input LUTs	7,908	30,720	25%	
Logic Distribution				
Number of occupied Slices	6,187	15,360	40%	
Number of Slices containing only related logic	6,187	6,187	100%	
Number of Slices containing unrelated logic	0	6,187	0%	
Total Number of 4 input LUTs	8,291	30,720	26%	
Number used as logic	7,908			
Number used as a route-thru	187			
Number used for Dual Port RAMs	32			
Number used as Shift registers	164			
Number of bonded IOBs	89	448	19%	
Number of BUFG/BUFGCTRLs	4	32	12%	
Number used as BUFGs	4			
Number used as BUFGCTRLs	0			
Number of DSP48s	4	192	2%	
Number of RPM macros	1			
Total equivalent gate count for design	181,238			
Additional JTAG gate count for IOBs	4,272			

III. CONCLUSIONS

MATLAB/Simulink and system generator is a very powerful tool that can be used for simulation and implementation of communication, control, DSP, etc. This paper builds a simulation and implementation the SDR model to illustrate the QAM techniques and how the Communication Blockset of the Simulink allow you to implement it. The simulation model verified the theory of QAM and can be used not only for the criteria for adaptive modulation but also for a platform to design other modulation systems. The speed and performance of FPGA can be improved and compensating and the area can be decreased by using short and accurate path and efficient software.

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