Multi-Input Multi-Pseudo Floating Gates Used In Circuits

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Abstract— Multi Pseudo floating gates with multi-inputs are used in circuits. The main operation of pseudofloating gates is bidirectional property by control gates.

Keywords-

I. INTRODUCTION

Floating Gate is a normal MOS transistor, except that the gate terminal is electrically isolated and has no DC path to a fix potential. The gate is completely surrounded by SiO_2, a high quality insulator that prevents charge stored on the floating-gate from leaking. In most cases using a standard CMOS process, a small leakage often exists. This leakage is crucial for modern processes. For 0.35µmm process with an oxide thickness less than 70A°, reprogramming may be necessary. Semi-floating gate is being recharged and then left floating same behaviour as non-volatile floating gates.

As their programming and initializing makes slight use of some complex techniques, there can be structures involving direct coupling to the floating gate. Pseudo-floating gate is constantly being recharged either by a forced leakage or by a constant feedback. Frequent recharging may require additional elements, thus adding some unwanted side effects such as leakage.

To exploit the floating gate computational property, the implementation multiple values of logic or functions are essential. In ref [2,4] the multiple valued logic is based on signal processing that is carried out using multiples of logic levels and thresholds.

Multiple valued logic circuits are to reduce signal lines on the chip effectively due to increase of information per line. The most of the designs have been current mode circuits due to the difficulties inherent in adding up signals in the voltage-mode and the need for additional fabrication steps/masks. The voltage mode CMOS circuits within multiple-valued logic have encountered to construct and realize a device that can distinguish the logical levels. The multiple valued designs consume less area and are faster.

II. A VOLTAGE-MODE MULTIPLE VALUED FLOATING-GATE INVERTER

The capacitive divider function of the floating gate is used to weight the input signals and the floating gate potential would determine the output. For this case of multiple-valued signal processing the inverter is made analogue. The feedback capacitor C_f can be obtained a certain gain for multi-input analogue floating gate inverter.

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The gain should be |1| by adjusting the $\frac{C_f}{C_i}$ ratio. The output satisfying $V_{out} = V_{dd} - V_{in}$ is preferred.

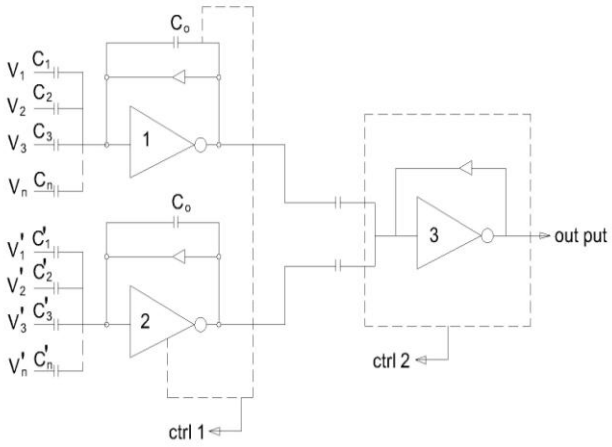
III. PSEUDO FLOATING GATE (PFG)

The pseudo floating gates are recharged by either a forced leakage or by a constant feedback in ref [1,3,5,6]. The main difference is the use of a feedback "buffer" instead of a recharge switch and thus eliminating the recharge clocks and periods. The pseudo floating gates can compute multiple – valued signals. The main operation of pseudofloating gate is bidirectional property by control signals.

IV. MULTI PSEUDO FLOATING GATES

Multi-valued logic is based on signal processing that is carried out using multiples of logic levels and thresholds. In current mode multiple valued logic circuits consume a significant amount of power due to static currents for each logic level. In fact, some voltage mode multiple valued logic modules easily can be fabricated and it requires less area and are faster.

V. SYMBOL OF MULTI-INPUT MULTI-PSEUDO FLOATING GATE



Multi-input multi-pseudo floating gate

VI. SIMULATION MODEL FOR MULTI-PSEUDO OF FLOATING GATE WITH MULTI-INPUT MOS TRANSISTOR

$$V_{icm1} = \frac{(C_1V_1 + C_2V_2 + \ldots + C_nV_n + Q_1)}{(C_0 + C_1 + C_2 + \ldots + C_n)}$$

Where V_i is the voltage of i^{th} control gate, n input control gates are capacitively coupled to the pseudo floating gate. Q_1 is the initial charge on pseudo floating gate.

$V_{PFG,CM}$ = Voltage for pseudo floating gate on common mode

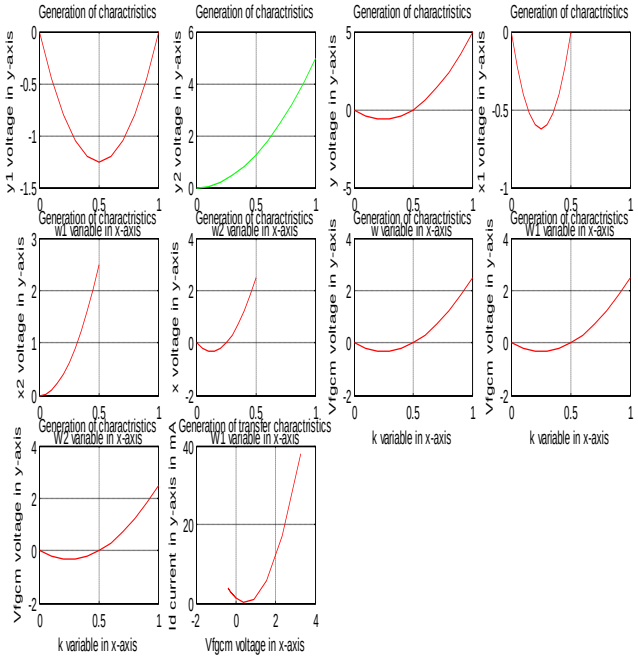
$= K_1 V_{PFG_1} + K_2 V_{PFG_2}$

where $K_1 V_{PFG_1} = \omega_1 v_{icm1} + \omega_2 v_{b_1}$

and $K_2 V_{PFG_2} = \omega'_1 v_{icm2} + \omega'_2 v_{b_2}$

v_{b_1} and v_{b_2} has the maximum value of v_{dd} .

$I_{ds} = \frac{1}{2}\mu C_0 \frac{\omega}{L}(V_{PFG,CM} - V_T)^2 = k_0 (V_{PFG,CM} - V_T)^2$ current is dependent on V_{GS} but less depend on V_{ds} .



Voltage characteristics of multi-pseudo floating gate with multiple control gates

VII. CONCLUSION

1. If we do not consider weak feedback buffer the physical structure of the pseudo floating gate transistor is the same with floating gate transistor.
2. Multi pseudo floating gates can be used in circuit to reduce the multi-signal path.
3. Now-a-days, application to Neural Network which will be a great challenge to the fabrication of pseudo floating gate. This work is going on and will be published very soon.

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