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# Design and Implementation of Envelope Amplifier and Power Amplifier for Envelope Tracking in Polar Transmitters

**T.K.Abdul Qadir, V.Venkateswarlu**

***Abstract*— Envelope tracking is an amplitude modulation technique for a polar transmitter. The circuit for implementing envelope tracking technique consists of an envelope amplifier (EA) and a power amplifier (PA) whose design and implementation on Cadence Virtuoso platform is presented. The envelope amplifier amplifies the envelope signal by a gain of 2 and the power amplifier requiring a power added efficiency (PAE) of 55-60% and a peak to average ratio (PAR) of 4-6dB tracks the envelope of the transmit signal to ensure it operates linearly, i.e. the supply voltage rides above the amplitude modulated signal. The envelope and phase signals are generated from envelope and phase power supply sources available in Cadence Virtuoso. The overall system efficiency is determined by the product of the envelope amplifier efficiency and PAE of the RF power amplifier.***

***Index Terms*— Polar transmitter, envelope tracking, phase modulation, amplitude modulation, envelope amplifier and power amplifier.***

## I. INTRODUCTION

The transmitter architecture called polar transmitter is different from conventional quadrature transmitter. Polar modulation techniques offer the capability of multimode wireless system and the potential for the high efficiency Power Amplifier (PA). As we know, any input signal of baseband message is decomposed into magnitude and phase signal, and then goes through envelope modulator and phase modulator respectively. The modulated envelope and phase message signals are combined and amplified by switched-mode PA.

### *A. Polar concept-*

The phase component modulation is applied using the phase locked loop (PLL) while the amplitude component modulation is applied at the PA. Since the amplitude of the phase-modulated signal produced by the PLL remains constant, it can be amplified using very efficient, saturated or compressed amplifiers. This dramatically reduces DC power consumption by the transmitter [6].

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Ideally, the amplitude modulation is applied at the PA as this approach is potentially the most efficient [6]. That is because the sole purpose of the PA is to amplify the transmit signal to a strong enough level to establish a reliable wireless link.

As such, it dissipates more dc power than any other circuit in the wireless transceiver. The best PA efficiency is achieved with a saturated PA that operates as a switch and toggles between the positive regulated voltage and ground. Its design pushes the device voltage toward ground during the output current peaks, minimizing power dissipation in the transistor. As a result, a saturated PA can achieve efficiency levels above 60 percent or higher. This type of PA produces strong harmonics and requires an output filter to select the RF carrier. In practice, the amplitude modulation (AM) is applied to the saturated PA by adjusting the positive regulated voltage. This is usually accomplished with a DC-DC converter or switching regulator with extremely good efficiency. In practice, the regulator's efficiency depends on the switching frequency, which also affects the supply noise and the AM signal's bandwidth. Using this approach produces nearly ideal amplitude control all the way down to low supply voltages. At these low supply voltages, the transistor acts less like a switch, and distortion results [6].

An alternative PA topology using envelope tracking operates less like a switch and more like an amplifier to reduce distortion. In this PA the DC-DC converter tracks the envelope of the transmit signal to ensure that the amplifier operates linearly. That is, the supply voltage rides above the AM signal. This type of system can adapt if the bandwidth of the dc-dc converter falls short of the AM signal requirements. This approach achieves approximately 50 percent efficiency. Both PA modulation approaches improve efficiency at moderate to high output power levels [6].

We can express phase and amplitude with a theoretical justification for the polar method of modulating the amplitude and phase of a carrier of radian frequency $\omega_0$. any modulated waveform x(t) at carrier frequency ω0 rad/sec is expressed with full generality by the expression-

$$X(t) = \mathrm{Re}\left(\gamma(t)\, e^{j\omega_0 t}\right) \quad (1)$$

Where is a complex waveform that may be expressed in polar format as -

$$\gamma(t) = r(t)\, e^{j\theta(t)} \quad (2)$$

Here, r (t)>=0, the envelope and θ(t) belongs to (-π,+ π), the phase are both real numbers. Hence we get,


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$$X(t) = Re\left(r(t)e^{j(\omega ot + \theta(t))}\right) = r(t)x\ cos(\omega ot + \theta(t)) \quad (3)$$

The above equation shows that amplitude and phase modulated signals are combined at the power amplifier [1][2].

## II. PROJECT

The polar transmitter (Tx) systems have timing mismatches between AM and PM paths at the PA, large bandwidth required for polar transmission and the I/Q to polar conversion (CORDIC processing) is non-linear which expands the bandwidth of the AM and PM signals [1].These major issues can be significantly relieved by using a modification of conventional polar Tx architecture called Envelope Tracking (ET) -based polar Tx architecture as shown in fig. 1 [1].

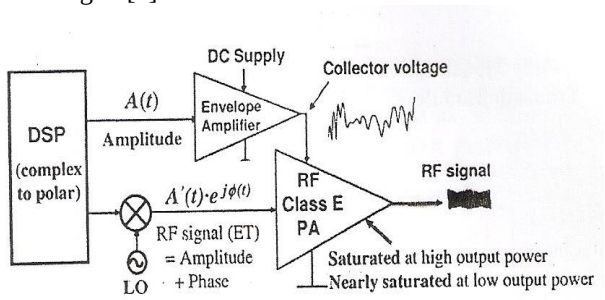


Fig. 1– A simplified block diagram of a RF polar Tx using ET technique.

### *A. Principle of an envelope tracking -*

Fig.2 illustrates the principles of an envelope tracking power supply amplifier, which detects the envelope of the RF amplifier input signal and controls the RF power amplifier power supply voltage accordingly. Using a variable $V_{DD}$ reduces average power dissipation and increases permissible peak output, and thus enables higher amplifier power efficiency than is possible with a fixed power supply voltage. This circuit consists of an operational amplifier, used as a wideband voltage source, plus a DC-DC converter used as a high-efficiency current source [11].

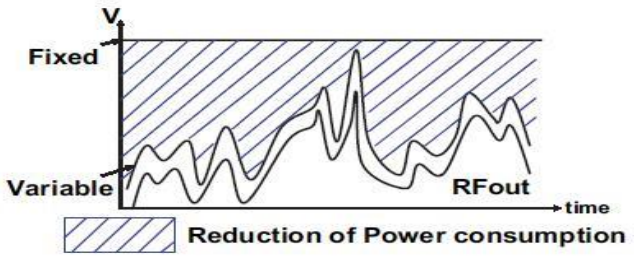


Fig. 2 – Principle of ET

### *B. Generation of envelope and phase signal -*

In a polar transmitter, the phase and amplitude signal components are generated by the CORDIC processor (Appendix).A baseband signal is represented by [3] –

$$V(t) = x(t) + j * y(t) \quad (1)$$

In the CORDIC processor, this baseband signal is split into envelope signal A (t) and phase signal θ (t) [3].

$$A(t) = (x(t)^2 + y(t)^2)^{\frac{1}{2}} \quad (2)$$

$$\theta(t) = \tan^{-1}\left[\frac{y(t)}{x(t)}\right] \quad (3)$$

As the envelope signal has a square root function, all envelope values are positive values and both sides of the phase signal are tracked with respect to these envelope signal values. That is why the envelope signal is single ended input [3].

Since the design of the CORDIC processor or envelope detector is not dealt with, the envelope and phase signals are generated from envelope and phase sources available in Cadence Virtuoso and then envelope modulation followed by envelope tracking with PA is designed and implemented. The range of envelope signal variation is from 0.6 V to 1V which is obtained on the basis that the power supply to the complete system is 3V and for the PA of a GSM/EDGE system to have input power supply of 8dBm and PAR of 55-60% , the envelope range at the input of the op-amp has to be between 0.6-1V so that when given a feedback gain of 2 and supplied to the $V_{DD}$ of PA, the envelope signal ranges from 1.2-2V giving input power of 8dBm and PAR of 55-60%. The phase signal given as RF input to the PA has phase 45-60deg and frequency 2GHz [1].

### *C. Operation of conventional envelope amplifier -*

High efficiency power amplifiers (PAs) are critical in portable battery-operated wireless communications because they can dominate the power consumption. The traditional ET system improves the efficiency by driving the radio frequency (RF) transistor in switch mode (Class D/E mode) with a constant amplitude phase signal and superimposing the envelope signal at the collector/drain of RF transistor. The highly efficient envelope amplifier is critical to the ET system since the total system efficiency is the product of the envelope amplifier efficiency and RF transistor drain efficiency, i.e:

Total efficiency $\eta = \eta_{\text{envelope amp}}. X\ \eta_{\text{RF transistor}}$ (4)

The wideband envelope amplifier is composed of a parallel linear voltage source and a highly efficient switched current source.

Fig.3 shows the conventional envelope tracking power supply circuit, with the RF amplifier we modeled as a resistance load. When we input a DC signal, the operational amplifier provides current to the load resistance such that the output voltage equals the input voltage and the voltage across the sense resistor terminals increases. When a comparator turns on the MOSFET switch, the current in the inductance increases gradually and the operational amplifier current decreases.

The voltage across the sensing resistor decreases until the comparator turns the MOSFET switch off. Then the current in the inductance decreases gradually, and accordingly the voltage follower output current increases to make up the output current. These actions are repeated (in other words, the circuit oscillates). The hysteresis band determines the gap between switch-on and switch-off points. The larger the hysteresis band, the longer the switching interval. Also, the larger the inductance the longer the switching interval. Therefore, we see that the switching frequency is inversely proportional to both the inductance value and the hysteresis band (fig. 3.4, 3.5, 3.6) [11].

(3.4.3)


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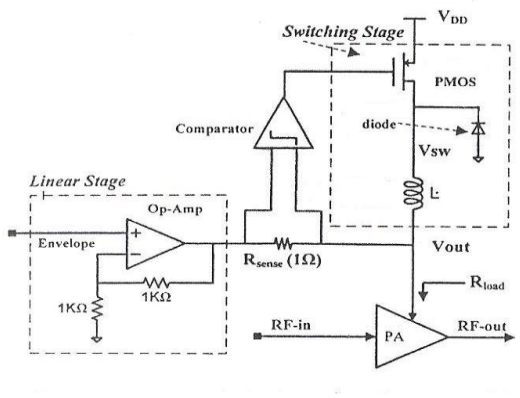


Fig 3. – Envelope tracking circuit

The envelope amplifier has 3 modes of operation [1][2][3] –

1) Linear operation for small signal envelope –when the average slew rate of switching current is much larger than the average slew rate of load current The switching stage can provide both the DC and AC components of envelope signal.
2) Large signal operation –when the average slew rate of switching current is much smaller than the average slew rate of load current .The switching stage can provide only the DC component while AC component will be provided by linear stage. The average switching frequency of the buck converter is the same as the signal frequency which the current sensor R can detect.
3) Matched slew rate point – when the average slew rate of switching current is equal to the average slew rate of load current [1].

## III. RESULTS- SIMULATION AND ANALYSIS

Table 1 – overall design specifications [1][2][8][31][32]

| | |
|---|---|
| CMOS Technology | 180nm |
| Power supply ($V_{DD}$) | 3 V |
| Output Power | 18.2dBm |
| Frequency | 2GHz |
| Input Power | 8dBm |
| Average Power | 50mW |
| Peak Power | 120mW |
| PAR | 4-6dB |
| PAE | 55-60% |

### *A. Circuit design for envelope amplifier-*

The components of the envelope amplifier comprise of op-amp (linear stage), comparator and buck converter (switching stage) as shown in fig. 3 [1].

The op-amp used in the envelope amplifier has to be used as a simple amplifier with a feedback gain of 2 [1] and thus a simple two-stage op-amp suffices the requirements of the envelope amplifier. Fig.4 shows the schematic of the designed op-amp and fig.5 shows the op-amp feedback linear stage with gain 2.

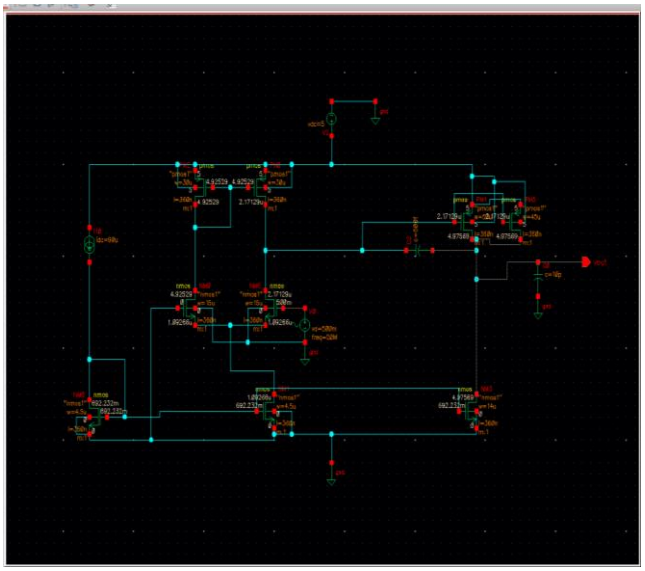

Fig. 4 – designed schematic of op-amp

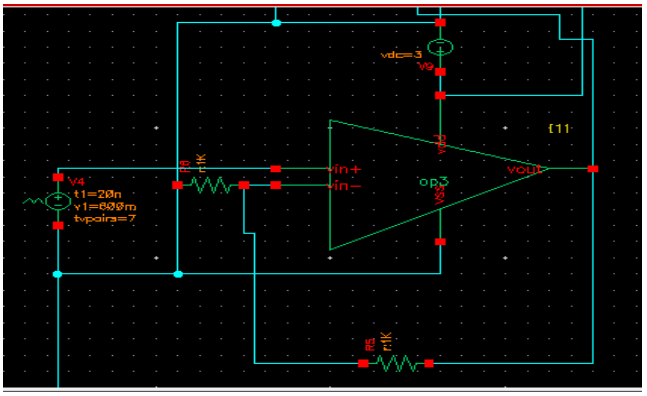


Fig. 5 – designed schematic of linear stage

A comparator is a device that compares two voltages or currents and switches its output to indicate which is larger. Fig. 4.4 depicts the circuit of the latched-type comparator in the EA design. The reason for using a latched-type comparator is that both the inputs to the comparator are expected to be equal at all times and a latched-type comparator helps in saving power as it is switched on only at regular intervals to check the inputs and thus conserving power while its off. Fig.6 shows the designed schematic of the comparator.

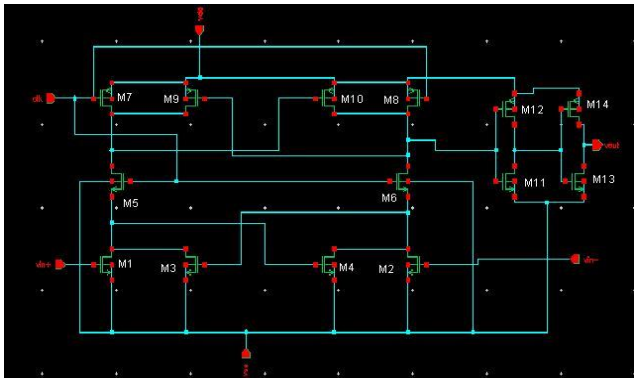


Fig.6 – designed schematic of comparator


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A buck converter in fig. 7[1 and 29] is a step-down DC to DC converter. It is a switched-mode power supply that uses two switches (a transistor and a diode) and an inductor. The conceptual model of the buck converter is best understood in terms of an inductor's "reluctance" to allow a change in current. The variation in the design of the buck converter presented requires it to maintain a constant current supply to the load (PA) of 5mA and keep the voltage variation constant at 1V.

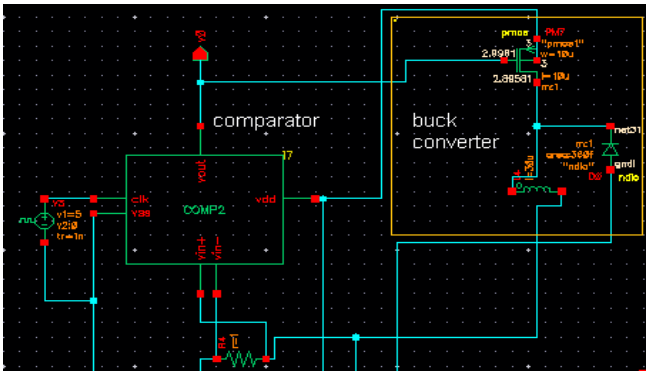


Fig. 7 -Designed schematic of comparator and switching stage

### *B. Circuit design of power amplifier-*

Table 2 – Target specifications of power amplifier [1]

| | |
|---|---|
| Quality Factor | > 1 |
| Frequency | 2GHz |
| Phase | 45-60 deg |
| Input power | 8dBm |
| Output power | 18dBm |
| PAR | 4-6dB |
| PAE | 56-60% |
| Power Supply ($V_{DD}$) | 1.2-2V |

Cascode configuration as shown in fig.8 is a convenient method to increase the output power of amplifiers especially in Class-E amplifiers where high peak drain voltage prohibits the use of high supply voltage. The signal at the output can deliver twice the power than the single ended output. Another advantage is that the current is discharged twice in each cycle minimizing the common mode signal and reducing the substrate coupling effects. To ensure that the envelope of the RF signal varies continuously with respect to its supply voltage, the $V_{DD}$ of the PA is the envelope signal which is also shorted to $M_1$ as its $V_{GG}$.

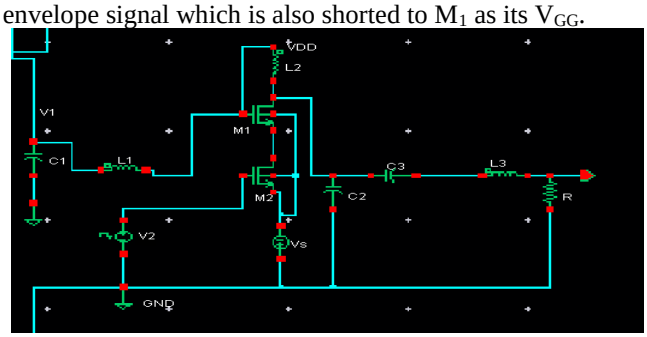


Fig. 8 – designed schematic of PA

### *C. Combining of phase and amplitude signal-*

Fig. 9 shows the complete designed schematic of ET circuit in which net03 denotes the amplitude signal coming from the comparator switching stage and net16 is the phase signal. Both the signals are assumed for combining here as they are generated at the output of the CORDIC processor not dealt with in this project. Vout shows the combining of both signals and it can be observed that the amplitude is limited to 1.25V which is that of net03 and the frequency of 1GHz that of net16 with the same phase.

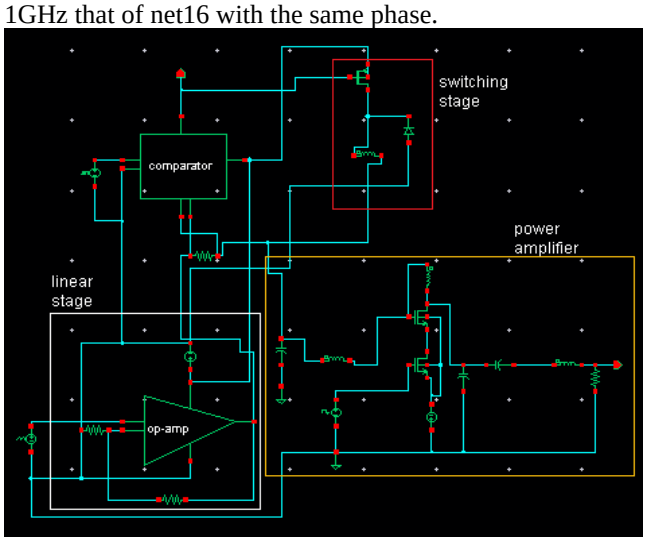


Fig. 9 – designed schematic of ET circuit

Fig. 10 shows the transient analysis response of EA having matched inputs to the comparator. Here, net16 is the envelope input to linear stage, net9 (vin+) and net10 (vin-) inputs to the comparator and v0 is the output of the comparator.net16 is the original envelope signal.

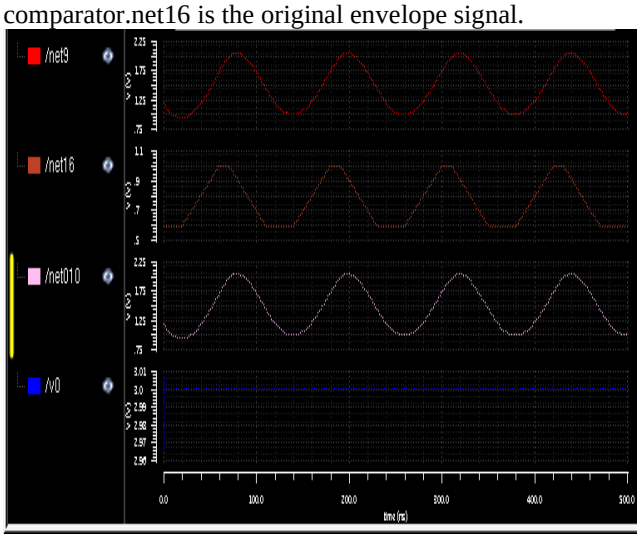


Fig.10 – Transient response of envelope amplifier in ET circuit

Fig. 11 shows the output generated by the power amplifier when a phase signal (net29) is applied to one of its inputs. The frequency of phase signal is 2 GHz at 60 deg phase.


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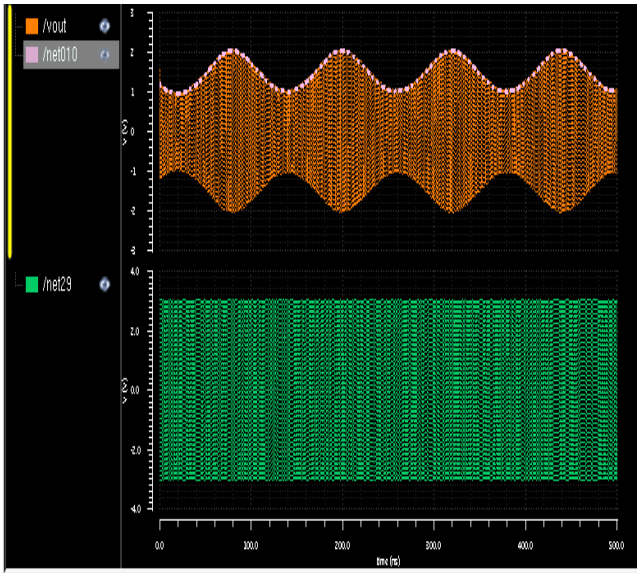


Fig. 11 - Transient response of power amplifier in ET circuit

Fig. 12 shows the DC analysis response of the envelope amplifier for a voltage range of -3V to 3V.

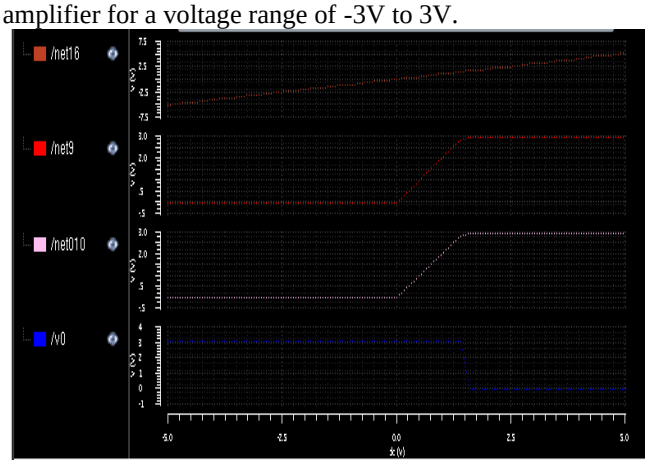


Fig.12– DC response of the ET circuit

Fig. 13 shows the AC analysis response of the ET circuit. The analysis shows a peak in the range of 1-2GHz denoting its required range of operation.

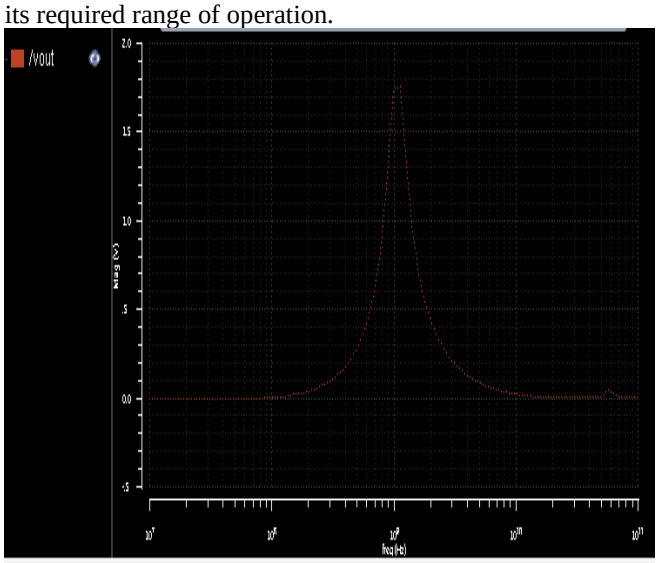


Fig. 13 – AC response of ET circuit

Fig. 14 shows the parametric analysis for the final ET output signal with a variation in power from 1V to 2 V showing how the output remains stable as required in this range.

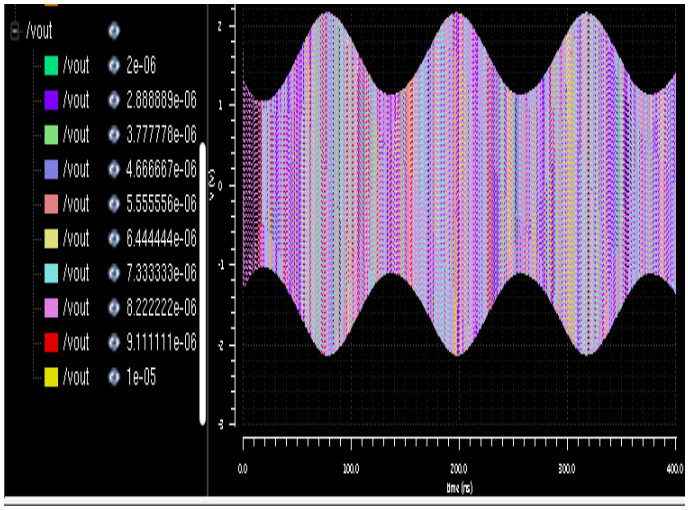


Fig. 14 – Parametric analysis of ET circuit

Fig. 15 shows the power analysis of the ET circuit. The peak power obtained using the calculator in Cadence is 135.4 mW and output power is 30.85dBm.

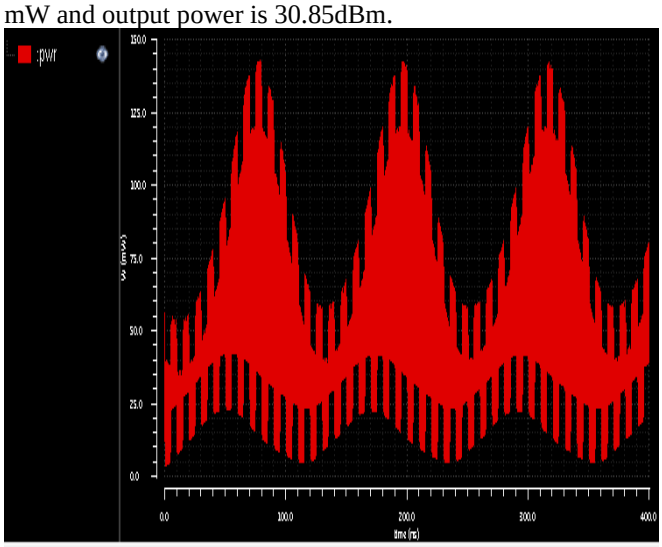


Fig. 15 – Power analysis of ET circuit

Fig. 16 shows the energy of a complete cycle. The energy of a single cycle obtained using the calculator in Cadence is 51.7 e-9 J.

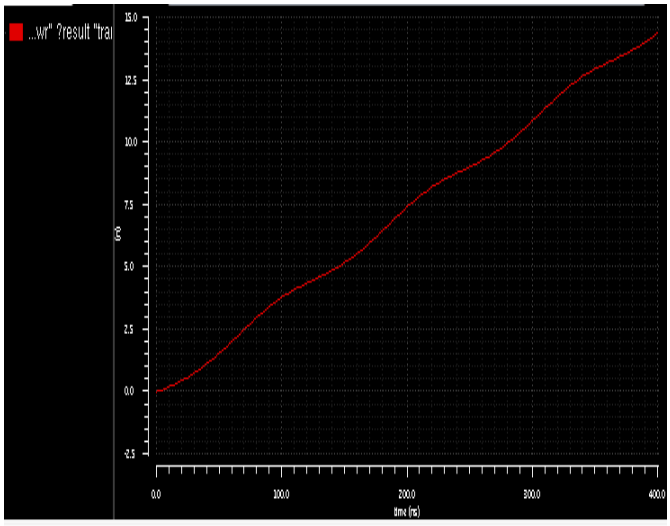

Fig. 16 – Energy analysis of ET circuit



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Fig.17 shows the power spectrum analysis of ET circuit which also gives the following values - SNR = 5.66 dB; SNDR = 31.14 dB; ENOB = 6.431 bits and SINAD = 5.66 dB.

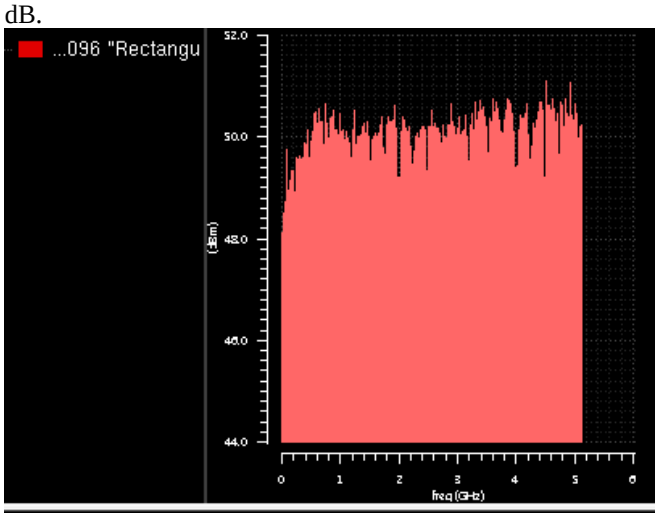


Fig. 17 – Power spectrum analysis of ET circuit

Fig. 18 shows the noise analysis of ET circuit and Fig. 19 shows its noise summary.

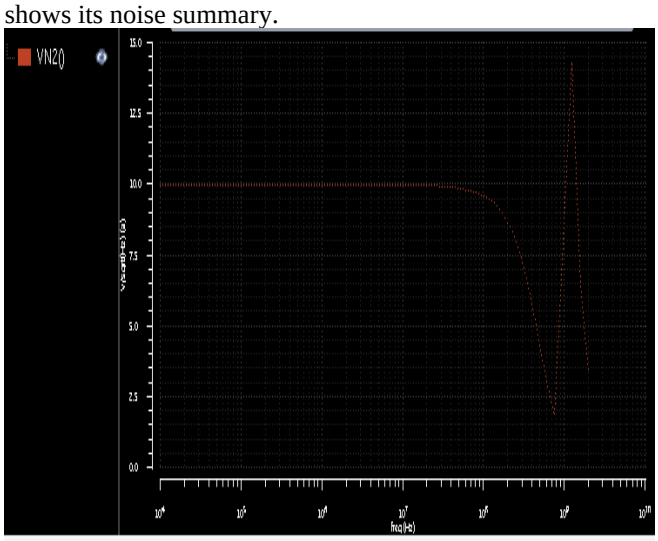


Fig. 18 - Noise analysis of ET circuit

| Device | Param | Noise Contribution | % Of Total |
|---|---|---|---|
| /R7 | rn | 2.71468e-18 | 81.16 |
| /NM9 | id | 3.81394e-19 | 11.40 |
| /NM8 | id | 2.44424e-19 | 7.31 |
| /NM9 | fn | 2.60568e-21 | 0.08 |
| /NM8 | fn | 1.73325e-21 | 0.05 |
| /NM9 | rs | 1.38794e-22 | 0.00 |
| /NM8 | rs | 4.25308e-23 | 0.00 |

Spot Noise Summary (in V^2/Hz) at 20 Hz Sorted By Noise Contributors
Total Summarized Noise = 3.34505e-18
No input referred noise available
The above noise summary info is for noise data

Fig. 19 - Noise summary of ET circuit

Table 3 shows the summary details of all the simulated results of ET circuit with matched inputs to the comparator.

Table 3 – Summary of simulated results from the ET circuit schematic

| Parameters | Expected results | Simulated results |
|---|---|---|
| CMOS Technology | 180nm | 180nm |
| GB of full system | 190MHz | 160MHz |
| Output Power | 18.2dBm | 30.85dBm |
| Frequency | 2GHz | 2GHz |
| Input Power | 8dBm | 9.83dBm |
| Average Power | 50mW | 34.28 mW |
| Peak Power | 120mW | 135.4 mW |
| PAR | 4-6dB | 5.975 dB |
| PAE | 55-60% | 58.823% |

## 1V. CONCLUSION

The designed envelope and power amplifier for envelope tracking achieved the entire bandwidth of 160MHz as opposed to the desired 190MHz as it is in this bandwidth range of 160MHz that the system operates as required achieving a PAR of 5.975dB successfully in the desired range of 4-6 dB and a PAE of 58.823% in the desired range of 55-60% for a GSM system. Also, the design requirements of individual blocks (op-amp, comparator and P.A.) are met. Thus, a design for envelope amplifier and power amplifier for envelope tracking in polar transmitters has been implemented and also individual results have been simulated and analyzed in Cadence Virtuoso platform.

## REFRENCES

[1] J. Lopez, Y. Li, J. D. Popp, D. Y. C. Lie, C. C .Chuang, , " *Design Of Highly Efficient Wideband Polar RF Transmitters Using Envelope Tracking Technique",* IEEE JSSC VOL. 44,NO. 9, pp. 2276-2294, September 2010.

[2] Feipeng Wang ,Donald F. Kimball, Jeremy D. Popp, Annie Hueiching Yang, Donald Y. Lie, Peter M. Asbeck and Lawrence E. Larson " *An Improved Power-Added Efficiency 19-dBm Hybrid Envelope Elimination and Restoration Power Amplifier for 802.11g WLAN Applications" ,* IEEE Transactions on Microwave Theory and Techniques, Vol. 54, No. 12, December 2006.

[3] Chung Chun Chen , Hung Yang Ko , Yi-Chiuan Wang , H.W. Tsao , K.Y.Jheng and Andy Wu, *"Polar Transmitter For Wireless Communication System",* IEEE ISPCS International Symposium , 2005

[4] M. Youssef, A. Zolfaghari, B. Mohammadi, H.Darabi and A.A.Abidi , *"A Low Power GSM/Edge/WCDMA Polar Transmitter In 65-nm CMOS "* , IEEE JSSC , VOL. 46,NO. 12, pp.3061-3074, December 2011.

[5] H. Jensen, A. Zolfaghari, H. Darabi,*" Analysis and Design of Small Signal Polar Transmitters for Cellular Applications ",* IEEE JSSC, VOL. 46, NO. 6, PP. 1237-1249, JUNE 2011.

[6] J.Groe, *"Polar Transmitters For Wireless Communications "* IEEE Conference Magazine,pp. 58-63, September 2007 .

[7] J. Choi , J. Yim, J.Yang , J. Cha , D. Kang , D. Kim , B. Kim , *" A Sigma –Delta Polar Transmitter "* , IEEE TMTT , VOL. 55 , NO. 12, PP. 2679-2690, December 2007.

[8] Till Kuendiger, Joseph Schrey, Iman Taha, Yi Lin,Tao Dai, Li Liang, Song-Tao Huang, Yue Huang,"*Cadence Op-Amp Schematic Design Tutorial for TSMC CMOSP35 ",*December 7, 2001

[9] D. Nageshwarrao, K. Suresh Kumar, Y. Rajasree Rao, G. Jyothi Nizam Institute Of Engineering & Technology, Nalgonda (Dt.), SSJ Engineering College, Sridevi Women's Engineering College, Sri Sidharatha Institute Of Technology, Thumkur, Karnataka, India "*Implementation and Simulation Of CMOS Two Stage Operational Amplifier ".*

[10] R. T. Perry, S. H. Lewis, and A. P. Brokaw *et al., "A 1.4 V supply CMOS Fractional Bandgap Reference," IEEE J. Solid-State Circuits, vol.*42, no. 10, pp. 2180–2186, October 2007.

[11] D. F. Kimball, J. Jeong "*High-Efficiency Envelope-Tracking W-CDMA Base-Station Amplifier Using GaN HFETs",* IEEE Trans. On Microwave Theory and Techniques, vol.54, no.11 ,November 2006.



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[12] F. Wang, *"High Efficiency Linear Envelope Tracking and Envelope Elimination and Restoration Power Amplifier for WLAN OFDM Applications,"*Ph.D. Dissertation, University of California, San Diego (2006).

[13] P. Asbeck, D. Kimball, *"Next Generation High-Efficiency RF Transmitter Technology for Base stations"*, Extended Abstracts of 2007 International Conference on Solid State Devices and Materials, pp. 146-147, September 2007.

[14] P. Draxler, S. Lanfranco, et.al., *"High Efficiency Envelope Tracking LDMOS Power Amplifier for W-CDMA"*, IEEE MTT-S International Microwave Symposium, pp.1534-1537 ,June 2006.

[15] L. Kahn, *"Single-Sided Transmission by Envelope Elimination and Restoration," Proc. IRE, pp. 803*-806, July 1952.

[16] T. Johansen, *"Monolithic Microwave Integrated Circuits for Wideband SAR System*," Ph.D. dissertation, Elect. Eng. Dept., Tech. Univ. of Denmark, Lyngby, Denmark, 2003.

[17] S.C.Cripps,*RF Power Amplifier for Wireless Communications*, Artec House ,1999.

[18] S.C.Cripps, *Advanced Techniques in RF Power Amplifier Design*, Artec House ,2002.

[19] Kanbe, M. Kaneta, H. Kobayashi, H. Yui, YUI, N. Takai, H. Hirata, T. Shimura, K. Yamagishi, *"New Architecture of Envelope Tracking Power Amplifier for Base Station"* IEEE Asia Pacific Conference on Circuits and Systems, Macao, China, pp.296-299,December 2008.

[20] Bakkaloglu, C. Chu, S. Kiaei, *"A 10MHz Bandwidth 2mV Ripple PA Supply Regulator forCDMA Transmitters,"* ISSCC, pp.448-449 ,February 2008.

[21] *Wireless LAN Medium Access Control (MAC) and Physical Layer specifications, IEEE Std. 802.11a/b/g, 1999/1999/2003*

[22] G. B. Yundt, *"Series- or Parallel-Connected Composite Amplifiers",* IEEE Tran. Power Electronics, vol. PE-1, No.1, January 1986.

[23] N.O. Sokal, and A. D. Sokal, *"Class E – A New Class of High Efficiency Tuned Single Ended Power Amplifiers*," IEEE J. Solid State Circuit, SC-10, No.3, pp.168-176, June 1975.

[24] F. Wang, A. Ojo, D. Kimball, P. Asbeck and L. Larson, *"Envelope Tracking Power Amplifier with Pre-distortion for WLAN 802.11g,"* in IEEE MTT-S Int. Digests 2004, pp.1543-1546 ,2004.

[25] F. Wang, A. Yang, D. Kimball, P. Asbeck and L. Larson, *"Design of Wide Bandwidth Envelope Tracking PowerAmplifiers for OFDM Applications ,"* to be published in IEEE Tran. Microwave Theory Tech.648.

[26] H. R. Khan, A. Raheem Qureshi, Q. Wahab , *"A Fully Integrated Class-E Power Amplifier in 0.13um CMOS Technology"* , Electronic Engineering Department, NED University of Engineering & Technology, Division of Electronic Devices, Department of Electrical Engineering, Linköping University, Linköping, Sweden ,IEEE-2011.

[27] Debasis Parida , *"A Novel High Speed CMOS Comparator With Low Power Disipation And Low Offset",* Department Of Electronics & Communication Engineering National Institute Of Technology Rourkela ,2010.

[28] Dr. Paul M. Furth , Vishnu B. Kulkarni*," Low-Voltage CMOS Comparators With Programmable Hysteresis,"* Master Of Science In Electrical Engineering New Mexico State University Las Cruces, New Mexico,2005.

[29] Feipeng Wang, Donald Kimball, Jeremy Popp, Annie Yang, Donald Y. C. Lie, Peter Asbeck and Lawrence Larson, *"Wideband Envelope Elimination and Restoration Power Amplifier with High Efficiency Wideband Envelope Amplifier for WLAN 802.11g Applications* ", Dept. of Electrical and Computer Engineering, University of California at San Diego, La Jolla, CA Space and Naval Warfare System Center (SPAWAR), San Diego, CA.

[30] K. N. Leung and P. K. T. Mok, *"A sub-1-V 15-ppm/deg CMOS Bandgap Voltage Reference Without Requiring Low Threshold Voltage Device," IEEE J. Solid-State Circuits, vol. 37, no. 4, pp. 526–530*, April 2002.

[31] Microchip Technology *,"Buck Converter Design Example " ,* Microchip Technology Web seminars Incorporated,2006.

[32] Jens Ejury *,"Buck Converter Design "* , Infineon Technologies North America (IFNA) Corp. ,v0.1 , January 2013.