

# Mitigation of Total Harmonics Distortion by Using 84 Pulse VSC Configurations

P. Sreenath, Myaka. Narendhar, Tadikamalla. Sanjeev Rao

**Abstract**— This paper analyzes the 84 pulse VSC (Voltage source converter) and static synchronous compensators (STATCOMs) utilize multipulse converters due to the following: 1) lower harmonic injection into the power system and FACTAS; 2) decreased stress on the electronic components due to decreased voltages; and 3) lower switching losses. This paper approach is illustrated on an 84 pulse VSC and the effect on the dynamic performance and the total harmonic distortion (THD) is analyzed. 84 pulse VSC assembled by combining one twelve-pulse VSC, in conjunction with an asymmetric single phase seven level converter plus an injection transformer. With this arrangement, The VSC output's THD in voltage is reduced. The proposed strategy allows savings in the number of employed switches. Simulation and experimental results are provided to show the proposal appropriateness.

**Keywords**— FACT Devices, Multipulse converters, Voltage source converters, STATCOM, IGBT Switches and custom power.

## I. INTRODUCTION

The Static Synchronous Compensator (StatCom) is one of the most useful FACTS devices, since it can synthesize the reactive power from small storing elements [1]. When it is operated within the linear region, it is seen by the system as a synchronous voltage source [2,3]. By regulation of the StatCom's output voltage magnitude, the reactive power exchange between the device and the transmission system may be controlled to improve the power system voltage profile [4,5]. Since the StatCom may cause interference on the system's fundamental sine wave at frequencies that are multiples of the fundamental one, especial care should be taken to ensure not to pollute the system to prevent further harmonic issues. In general, there are three feasible strategies to assemble a VSC: (i) the multi-pulse; (ii) the multi-level; (iii) and the pulse-width modulation (PWM) [9]. Strong efforts have been made in order to reach minimum harmonic distortion in the VSC's output voltage. A strategy to build an 84-pulse equivalent output voltage waveform, which employs a twelve-pulse along with an eight-level reinjection converter is presented. However, the cost for this is 26 extra switch devices and 7 DC voltage sources (capacitors).

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This array makes the control task difficult because of the amount of gate signals needed, and it is prone to unbalance, due to the large chain of capacitors. Multi-Level Voltage Reinjection (MLVR) H-bridge conversion is another option to generate 84 pulses, which requires the use of 5 additional DC voltage sources and 12 switches, as opposed to the conventional 12-pulse converter. It may be easily utilized to attain more levels on the reinjection by adding H-bridges in series.

## II. 84-PULSE VSC TOPOLOGY

Numerous methods have been investigated to increase the number of pulses in the multi-pulse converters' output. The simplest one is by increasing the number of six-pulse converters and the corresponding transformers (4 six-pulses converter results in 24-pulse, 8 six-pulse converter results in 48-pulses operation, and so forth). The harmonic cancellation is carried out by the transformer secondary windings' arrangement.

The weakness of this method is the large size and high cost due to the increased number of bridges and transformers. In order to overcome such difficulty, an auxiliary circuit in the DC link side has been proposed for reinjection. Such topology results through modifying the DC input on the conventional double bridge twelve-pulses shunt converters through a multi-level auxiliary circuit with an injection transformer. In this paper, an asymmetric 7-level array for the auxiliary circuit is used as a reinjection scheme, Fig. 1. The conventional double bridge twelve-pulse operation is assembled by connecting two identical three-phase bridges to three-phase transformers in a parallel VSC configuration. Each branch in the six-pulse converter must have a displacement of 120° among them. The upper switch is conducting while the lower one is open and vice versa (180° voltage source operation). A 30° displacement in the firing sequence of both converters should be considered. Transformer's turn ratios are 1:1 and 1:3 on the YY and Y transformers, respectively. By injecting additional DC pulses via the three-phase bridges' neutral point, an effect of pulse spreading is attained. The auxiliary circuit is common to the three phases, reducing the number of extra components. The configuration description to provide pulse multiplication is detailed in [9]. In Fig. 1, A-B illustrates the auxiliary seven-level inverter utilized as a reinjection circuit. To apply the seven-level inverter output voltage to feed the standard twelve-pulse converter, special care should be taken to not inject negative voltage into VY or V; notice the inclusion of the injection transformer between both arrays.



Thus, voltages at the six-pulse converter inputs can be regulated by adjusting the injection voltage  $U_i$  by:

$$V_y = V_{DC} + U_i \quad (1)$$

$$V_{\Delta} = V_{DC} - U_i \quad (2)$$

The injection voltage is determined by the seven-level inverter switching pattern and the injection transformer turns ratio. By using voltages  $V_Y$  and  $V_{\Delta}$  as inputs to the six-pulse converters, a cleaner VSC's output voltage comes about. Fig.2 exhibits the followed strategy to build  $V_{YU}$  and  $V_{\Delta U}$  as the interaction of the seven-level output and the corresponding six-pulse signals.

Through the 1:1 ratio for the YY TRANSFORMER, 1:3 for the Y TRANSFORMER, and adding their corresponding output signals, the 84-pulse line-to-neutral signal  $V_U$  emerges Fig.3a. the corresponding harmonic spectrum is depicted in Fig. 3b.

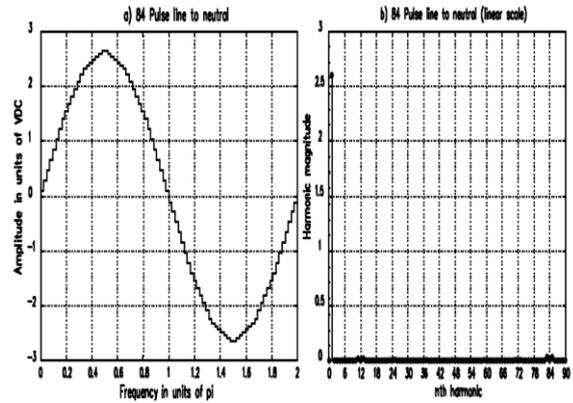


Fig. 3a) 84-pulse line-to-neutral output voltage and b) harmonic content.

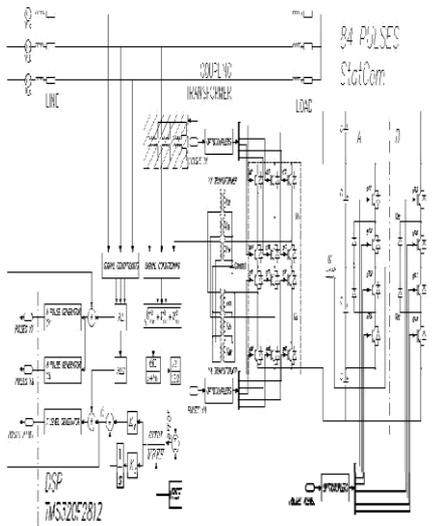
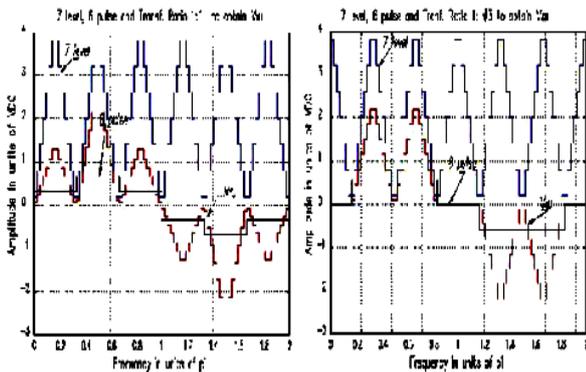


Fig 1. 84 pulse statcom structure.



### III. OPEN LOOP STATCOM STRUCTURE

The connection of the improved VSC to the system requires aspects to be considered. This section deals with such details within an open loop context.

#### A. Phase Locked Loop

The Synchronizing Circuit is responsible for determining the system frequency and the phase-angle of the controlled AC bus fundamental positive sequence. Fig. 2. mixing seven-level, six-pulse signals, and transformer's ratios to attain  $v_{yu}$  and  $v_u$

Voltage. The Phase- Locked-Loop (PLL) utilizes the Stationary Reference Frame in order to reduce the computational cost, and helps to improve the system's dynamic performance.

The digital PLL is an algorithm able to detect the phase of the fundamental voltage, through the synchronization of the output signal to the frequency and phase of the input one, without requiring a zero crossing subroutine at the input voltage, or to generate an internal reference signal for the input current.

#### B. Six-Pulse Generator

The second block is the six-pulse generator, responsible for generating the pulse sequence to fire the three-phase IGBT array. It consists of an array of six-pulse spaced  $60^\circ$  each other. The IGBT will operate at full  $180^\circ$  for the on period and  $180^\circ$  for the off period. Any disturbance on the frequency will be captured by the synchronizing block, preventing malfunctioning.

The falling border in the synchronizing block output signal is added to a series of six  $60^\circ$  spaced signals. The modulus operator with the 2 argument gives the needed on sequence that will be sent to the gate opto-coupler block, which will feed each six-pulse converter. The off sequence turns out on a similar way but waiting  $180^\circ$  to keep the same on and off duration in each IGBT.

#### C. Seven Level Pulse Generator

To operate the seven-level inverter, six times the frequency of the six-pulse generator must be ensured.



This is achieved by monitoring the falling border in the novel PLL output signal, using it along with the modulus operator with the  $\pi/3$  argument. This signal will be the period for the seven-level generator which will change its state each  $\pi/42$  rad.

#### IV. VSC ASSEMBLING

The 84-pulse VSC along with the PLL to synchronize it to the grid has been assembled in a low power lab prototype. It is important to observe that the scale provided by oscilloscope is on decibels and is very close to Fundamental frequency is 60 Hz and the main harmonics are about each 5 kHz, according to expectations.

#### V. CONCLUSIONS

This paper describes the strategy to obtain an 84-pulse VSC three-phase voltage with the associated low THD, by combining one twelve-pulse converter plus a seven-level converter.

The device performance, proven on a lab prototype, allows verifying the harmonic content of the resultant voltage signal. The exhibited low THD, permits the system to be used in especial applications or as basement of FACTS devices. The three-phase digital PLL used to detect the phase of the Fundamental voltage synchronizes the firing signals in all switches within a sample cycle.

#### VI. FURTHER WORK

MLVR-VSC long distance HVDC transmission.

A back to back HVDC link consisting of MLVR-VSC has already been proposed. This scheme shares the same dc side capacitance for both voltage source converters.

This is possible as in the case of a back to back link both converters are housed at the same location. But in the case of long distance HVDC Transmission, sharing of the dc capacitance is not a practical proposition as the two converter stations are far apart, typically few hundreds of kilometers. Therefore dc capacitances have to be installed at each end of the link. This creates a whole new scenario, which is different to the MLVR-VSC back to back link. The modeling and power relationships, closed loop control of the HVDC system is the main research subject.

#### REFERENCES

- [1] Hingorani, N.G. "FACT Technology State of the Art, Current Challenges and the Future Prospects," IEEE Power Engineering Society General Meeting, 24-28 June 2007, Tampa, Florida USA
- [2] Song, Y. H., and Johns, A. T.: 'Flexible AC transmission systems FACTS,' (IEE Power and Energy Series 30, 1999)
- [3] Acha, E., Fuente-Esquivel, C. R., Ambriz, H., Angeles, C.: 'FACTS. Modelling and Simulation in Power Networks.' (John Wiley and Sons, LTD, 2004.)
- [4] Wang, H. F.: "Applications of damping torque analysis to StatCom control", Electrical Power and Energy Systems, Vol. 22, 2000, pp. 197- 204.
- [5] CIGRE, "Static Synchronous Compensator", CIGRE working group 14.19, September 1998.
- [6] Hingorani, N. G., and Gyugyi, L.: "Understanding FACTS," (IEEE Press 2000).
- [7] El-Moursi, M. S., and Sharaf, A. M.: "Novel Controllers for the 48-Pulse VSC StatCom and SSSC for Voltage Regulation and Reactive Power Compensation", IEEE Transactions on Power Systems, Vol. 20, No. 4, November 2005, pp. 1985-1997
- [8] Davalos-Marin, R.: 'Detailed Analysis of a multi-pulse Stat Com', Cinvestav- Internal Report. May 2003, available at [http://www.dispositivosfacts.com.mx/di\\_tesis\\_doc.html](http://www.dispositivosfacts.com.mx/di_tesis_doc.html),

- [9] Pan, W., Xu, Z., Zhang, J.: "Novel Configuration of 60-pulse voltage source converter for StatCom application," International Journal of Emerging Electric Power Systems, Vol 8, Issue 5, 2007, Article 7.

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