International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-3 Issue-1, October 2013

Improvement of the Oscillation Frequency Characteristic of Conventional Voltage Controlled Ring Oscillator

Intissar Toihria, Rim Ayadi, Mohamed Masmoudi

Abstract*— A new design of a Voltage Controlled Ring Oscillator is proposed in this paper in order to improve the oscillation frequency characteristic. The structure and the operation of proposed Voltage Controlled Ring Oscillator have been described. The new VCO is implemented and simulated by using ADS platform with 0.35µm AMS CMOS technology; this circuit uses relatively small devices dimensions and low power supply 2V to operate in a large range frequency. In addition, the proposed structure enables the output signal of the VCO to oscillates between ''0'' and ''1'' for each input value of control voltage Vinvco, varied between 0V to 1,3V, which is difficult to get from the Conventional Voltage Controlled Oscillator. Input control voltage of VCO, Vinvco, it is the analog voltage generated from the Loop Filter if a Voltage Controlled Oscillator circuit is use in Phase Locked Loops (PLLs) systems.

Index Terms*— Voltage Controlled Oscillator, Voltage Controlled Ring Oscillator, CMOS Inverters, Simple Mirror Current.

I. INTRODUCTION

A Voltage Controlled Oscillator is considered one of the most essential basic building blocks in the design of mixed analog and digital systems [1], [2], [3]. This circuit has also received several attentions in recent years by many researches and designers because have been widely used in popular system. Voltage Controlled Oscillator is a very pervasive block exploited in diverse systems and applications, including for example Phase Locked Loops systems [4], Clock Generator circuits [5], and Clock Recovery circuits for serial data communications [6]. The importance of VCO requires the use of a reliable and efficient structure to meet the needs of applications where it is used. There are so many different implementations of voltage controlled oscillator circuit. One of them is the VCO based on a ring oscillator [7], [8] which is usually used in high-speed circuits require on-chip oscillators to generate clocks. Besides of this, system synchronization needs to be realized by Phase Locked Loops.

PLLs structure is presented in Fig.1, which also has a Voltage Controlled Oscillator as a critical part. The Phase Locked Loops (PLLs) architecture consists of a Phase Frequency Detector (PFD), a Charge Pump (CP), a Loop Filter (LF), a Voltage Controlled Oscillator (VCO) and a Divide by N Counter (DBN). The purpose of a PLL is to create an output signal which oscillates at the same frequency as the input signal. A key property of a VCO is that the output frequency is a linear function of the control voltage.

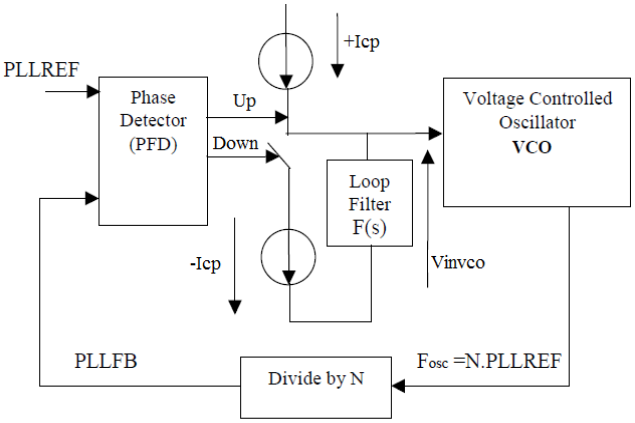

Fig.1. Block Diagram of PLLs

- *Phase Frequency Detector*

PFD is a purely digital system driven by the rising or falling edges of its inputs signals which are respectively reference signal (***PLLREF***) and feedback signal (***PLLFB***). The PFD deliver output signals in the form of three sequential logic states with Up and Down for controlling a 3-state Charge Pump [4].

- *Charge Pump*

Basically, the Charge Pump consists of two CMOS switches controlled by the PFD outputs. It is utilized to converts the sequential logic states of the PFD into analog signal [4].

- *Loop Filter*

The purpose of Loop Filter is to converts the charge pump current (***Icp)*** into a voltage controlled signal (***Vinvco)*** filtering the alternating current component [4]; and to suppress the noise.

- *Voltage Controlled Oscillator*

The VCO generates an output signal with its oscillation frequency proportional to the control voltage provided from loop filter block [4].

- *Divider By N Counter (DBN)*

The oscillation frequency generates from the VCO is then fed to the divide-by-N block which acts as a frequency counter before being fed back to the PFD.

This paper proposes a new design of a VCO based on a ring oscillator. Mainly, this work is focuses on modified a conventional voltage controlled oscillator structure in order to obtained a more stable output signal of VCO with respect to input voltage variations; this characteristic is difficult to get from the conventional voltage controlled oscillator [9], [10].

Manuscript published on 30 October 2013.
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The outline of this paper is the following. Section II describes the different structure of a conventional voltage controlled ring oscillator recently used. Section III presents the basic idea, implementation and design consideration of the new VCO designed. Simulation results of proposed structure are shown in section IV. Finally, a conclusion is mentioned of section V.

II. CONVENTIONAL VCO STRUCTURE

The design of a voltage controlled oscillator based on a ring oscillator topology; ring oscillator consisted of CMOS inverters [11] as shown in Fig.2; requires connecting odd number of inverters with the output of the last stage fed back to the input of the first stage.

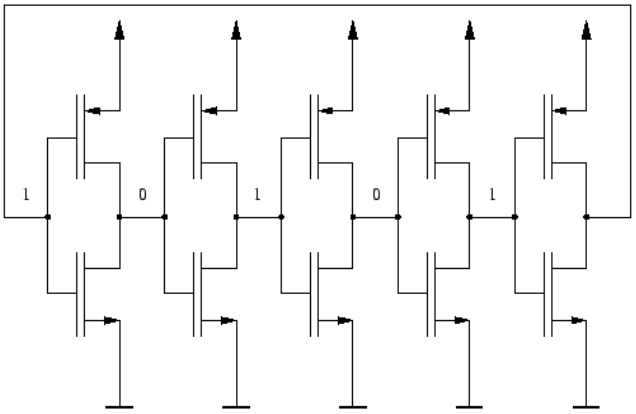


Fig.2. Ring oscillator using an odd number of inverters

A VCO based on a ring oscillator, as Fig.3 shows [7], [12]; is realized by N stages of CMOS inverters where N is an odd number of inverters, with inclusion a control mechanism of control current (***Ictrl***) flowing through the inverters which consisting the voltage controlled oscillator topology.

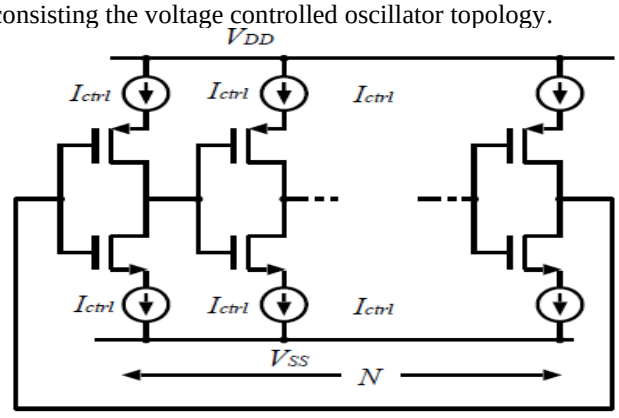


Fig.3. VCO based on a ring oscillator

Generally, we use one PMOS transistor to control the upper side current and an NMOS transistor to control the lower side one. This control current (***Ictrl***) is usually delivers by a simple mirror current circuit; we use one PMOS simple mirror current to generate the upper side controlled current (1) and an NMOS simple mirror current to generate the lower side one (2). A classic structure of voltage controlled ring oscillator associated by a simple mirror current circuit for generates the control current (***Ictrl***) flowing through these inverters; we can found her structure in Fig.4. In this structure, M2 and M3 transistors operate as similar an inverter, while the transistors coupled formed respectively by M1, M6 and M4, M5 are operate as a simple mirror current circuit.

$$I_{ctrl} = \frac{W_1 \times L_6}{W_6 \times L_1} \times I_{bias1} \quad (1)$$

$$I_{ctrl} = \frac{W_4 \times L_5}{W_5 \times L_4} \times I_{bias2} \quad (2)$$

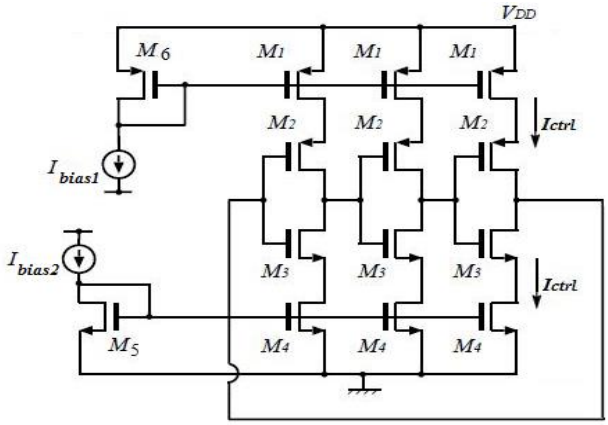
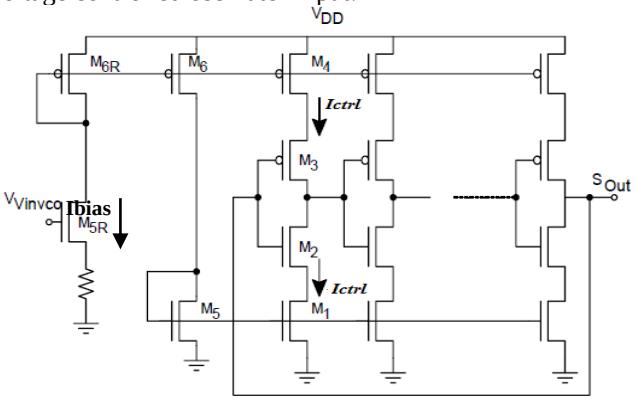


Fig.4. Voltage Controlled Ring Oscillator associated by Simple Mirror Current

The purpose of VCO circuit is to control its oscillation frequency via input control voltage (***Vinvco***) by starving the control current in the ring oscillator's inverter stages. The VCO circuit provides an output signal ***Sout***, whose oscillation frequency is proportional to the analog control voltage (***Vinvco***) applied at its input. Consequently, the oscillation frequency is changed for all variation of input control voltage. In a conventional VCO structure; as shows in Fig.5 [9], [10]; the VCO stops oscillating, neglecting sub threshold currents, when ***Vinvco<Vthn+R×Ibias*** since the input control voltage ***Vinvco*** of VCO is applied to the gate of NMOS transistor (M5R) and NMOS transistor is turned off if ***Vgs<Vthn***. This problem caused a major challenger in VCO designer. For assured a proper performs of VCO and solve this problem it is necessary to find new topology which meets the needs VCO designer and enable to oscillate for each value of the control voltage ***Vinvco*** applied at the voltage controlled oscillator input.



I R. Conventional Voltage Controlled Ring Oscillator

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Electrical simulation results obtained by using ADS platform are presented below, and shown the variation of VCO output signal which varies values of input control voltage ***Vinvco*** comprised between 0V to 1V. Four example of electrical simulation results, as respectively presented in Fig.6, Fig.7, Fig.8 and Fig.9 are showed that the VCO stops oscillating when ***Vinvco<Vthn+R×Ibias***. ***Vthn*** is the threshold voltage of NMOS transistor. Fig.9 showed that the VCO oscillating just one single pulse when ***Vinvco> 0.7V***. The obtained electrical simulation resultants show that the output signal of VCO is insufficient to ensure the proper functioning of the oscillation frequency characteristic of conventional voltage controlled ring oscillator. In order to solve this problem, a novel VCO design based ring oscillator is presented in below section.

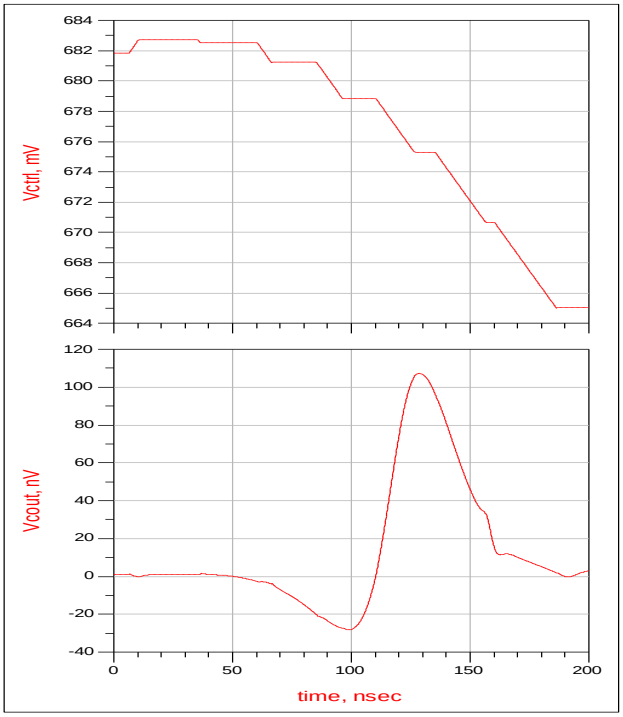

Fig.6. Variation of Output Signal when Vinvco<Vthn+R×Ibias

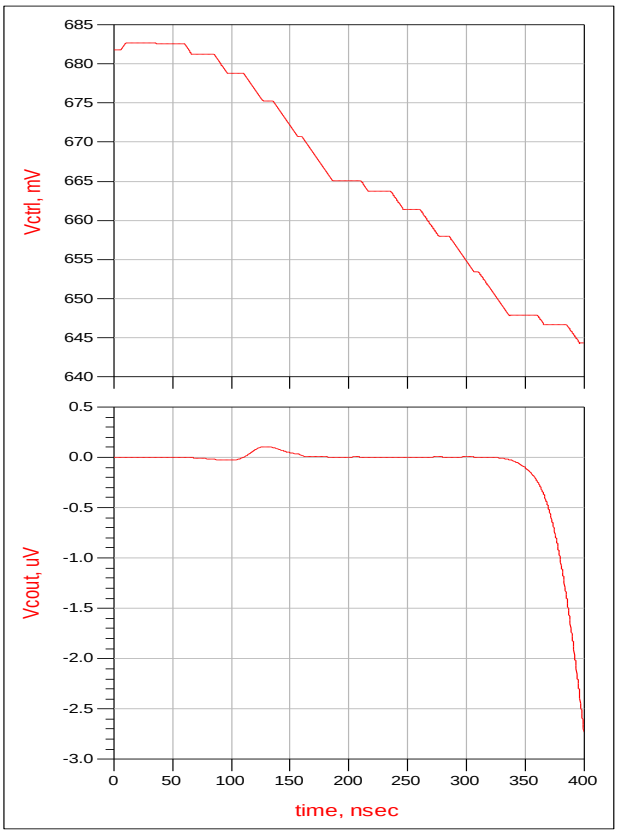

Fig.7. Variation of Output Signal when *Vinvco<Vthn+R×Ibias*

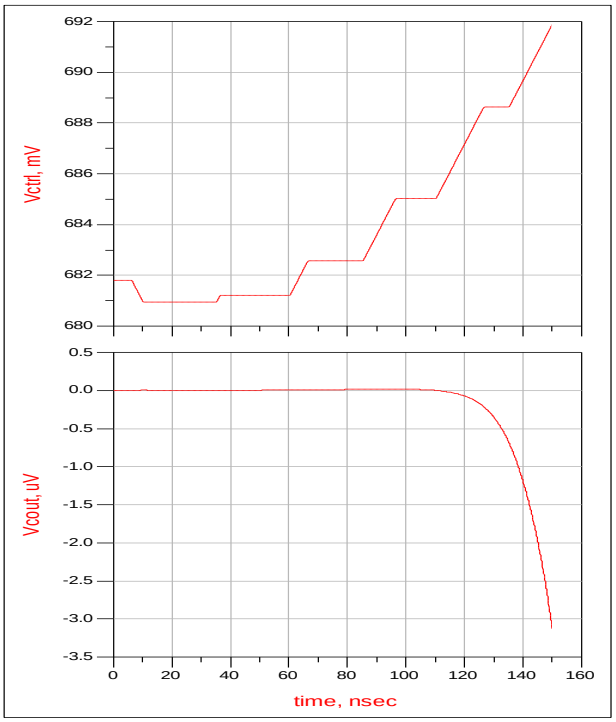

Fig.8. Variation of Output Signal when Vinvco<Vthn+R×Ibias

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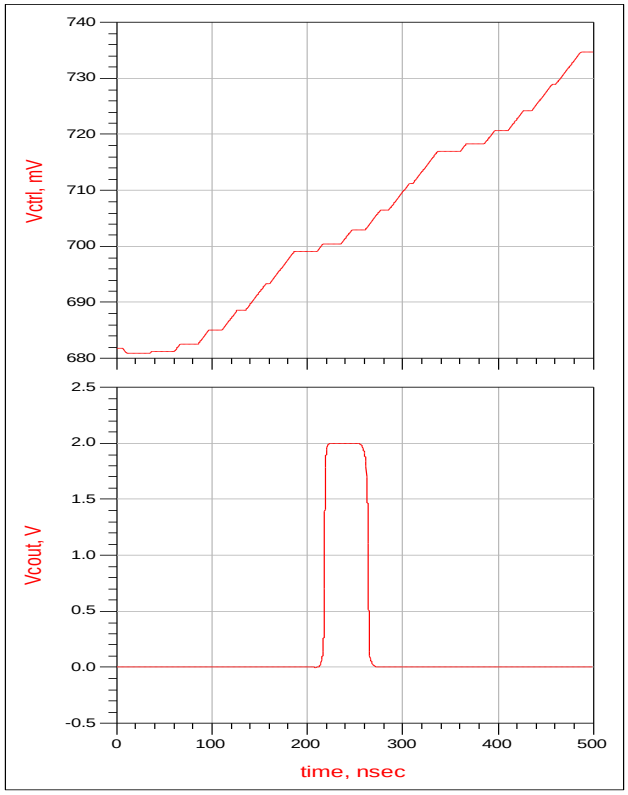

Fig.9. Variation of Output Signal when Vinvco<Vthn+R×Ibias and Vinvco>0.7V

III. PROPOSED VCO STRCUTURE

CMOS implementation of the new VCO design is shown in Fig.8 where five is an odd number and shows the number of CMOS inverters stages. The oscillation frequency of VCO is determined by the control current ***Ictrl***, number of stages ***N***, the oscillation amplitude ***Vosc*** and the parasitic capacitance. The new VCO based on a ring oscillator uses variable control currents to control its oscillation frequency, whose values of the control current is proportional to the analog control voltage ***Vinvco*** applied at its input. In proposed Voltage Controlled Ring Oscillator topology, the control voltage is applied to the input of VCO exactly at the gate of PMOS transistor (M8). Also the source control current is generates by a NMOS simple mirror current circuit where formed respectively by M7 and M5 (Fig.10), instead a conventional PMOS simple current mirror circuit used in recent work [9], [10]; where is formed respectively by M6 and MR6 (Fig.5). Indeed, the input stage; it's a bias block designed by a NMOS simple mirror current; sets the current in the control current sources which in turn sets the current in the inverters stages consisted VCO circuit. The purpose of a NMOS simple mirror current circuit used in the design of VCO is to generate and mirrored the desired control current flowing at each inverter stages consist the VCO. Also, the input control voltage ***Vinvco*** is applied at the input of VCO exactly at the gate of PMOS transistor, this transistor it is turned on when ***Vgs<Vthp*** consequently ***Vinvco<2+Vthp-R2×Ibias***, for assured that the VCO oscillating on all range of input controlled voltage ***Vinvco*** varied between 0V to1.3V.

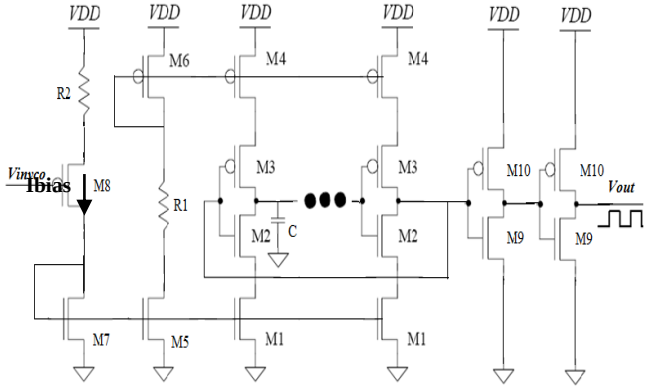

Fig.10. Voltage Controlled Oscillator

To aid in understanding of proposed voltage controlled ring oscillator, we study with detailed the functioning of all her elements. M2 and M3 transistors operate as similar an inverter, while the transistors coupled formed respectively by M7, M1 also M7, M5 and M4, M6 are operate as a simple mirror current circuit. The control current sources, M1 and M4, limit the current available to the inverter, M2 and M3. The input control voltage ***Vinvco*** is applied at the gate of PMOS transistor; it's the M8, for assured that the VCO oscillating on all range of controlled voltage varied between 0V to 1.3V. M7 and M8 transistors drain currents are the same and are set by the input control voltage ***Vinvco***. The currents source turn in M5, R1 and M6 are mirrored in each inverter stage consist the VCO. To limit the current in voltage controlled ring oscillator M5 and M6 transistors are used; this current can be limited by choosing proper W and L of M5 and M6. Finally, R2 resistor is used in this structure to adjust the current in M8 transistor.

To obtain oscillation, the ring oscillator must provide a phase shift of 2p and have unity voltage gain at the oscillation frequency. To determine the oscillation frequency at which this circuit will oscillate, assume that N is the number of inverters and τ is the delay through each inverter. The signal must go through N inverters for a total time of ***N×τ*** to obtain the first p phase shift. Then, the signal must go through each stage a second time to obtain the remaining p phase shift, resulting in a total period of ***2N×τ***. The frequency is the reciprocal of the period, resulting in the oscillation frequency of voltage controlled ring oscillator for N stages. Assume that the gate parasitic capacitances Cg of the NMOS and PMOS transistors are equal; the frequency of the oscillation can be found as (3).

$$F_{VCO} = \frac{1}{2N\tau} \tag{3}$$

Where ***τ*** is the delay for one stage of voltage controlled ring oscillator, which could be given by (4)

$$\tau = \frac{V_{osc} \times C_g}{I_{ctrl}} \tag{4}$$

Vosc is the oscillation amplitude and ***Ictrl*** is the control current. From the above two equations (3) and (4), we can be obtained (5).

$$F_{VCO} = \frac{I_{ctrl}}{2NV_{osc}C_g} \tag{5}$$

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IV. SIMULATED RESULTATS

Voltage Controlled Ring Oscillator minimum and maximum output voltage is obtained by applying a controlled voltage at VCO input signals (***Vinvco***). For an input control voltage (***Vinvco***) varies between 0V and 1.3V, output signal of VCO circuit gives an oscillation frequency which indicates respectively a minimum and a maximum oscillation frequency. Where ***Fvcomax*** is the output frequency corresponding to ***Vinvcomax*** and ***Fvcomin*** is the output frequency corresponding to ***Vinvcomin.*** The output signal of the VCO based on a ring oscillator oscillates between ‘‘0’’ and ‘‘1’’ for each input value of Vinvco varied between 0V to 1.3V. Even though for a case of ***-Vdd<Vinvco<Vthp*** also the oscillations frequency are obtained, and these oscillations are stable compared of other simulation results illustrates in section II. The electrical simulation results for all blocks of new proposed Voltage Controlled Ring Oscillator structure are presented respectively in Fig.11 and Fig.12 using ADS simulator with 0.35µm AMS CMOS processor operate with 2V power supply and indicate the proper operation of presented VCO topology based on a ring oscillator circuit.

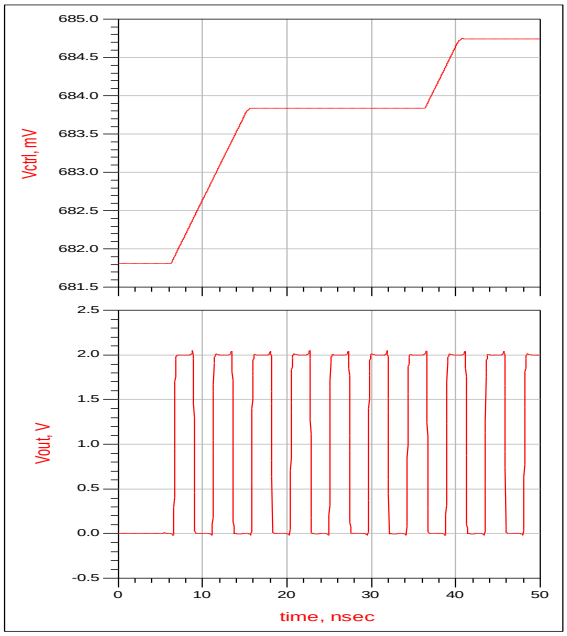

Fig.11. Variation of output signal when Vinvco<2+Vthp-R2×Ibias

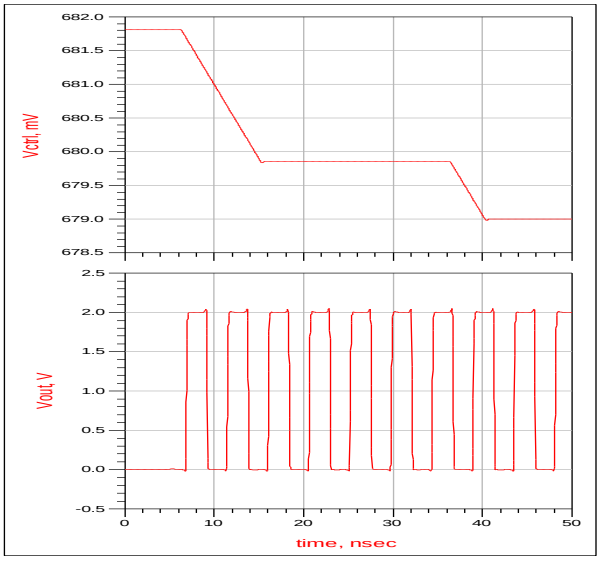

Fig.12. Variation of output signal when Vinvco<2+Vthp-R2×Ibias

V. CONCLUSION

This paper presented a new Voltage Controlled Ring Oscillator design; this circuit is a critical part of the PLL in mixed and RF applications. Proposed Voltage Controlled Ring Oscillator is designed and simulated by using ADS platform with 0.35µ*m AMS* CMOS technology to operate with 2V power supply and electrical simulation results are presented. Obtained results show that the proposed circuit enables the output voltage of VCO circuit to oscillates between ‘‘0’’ and ‘‘1’’ for each input control voltage value of the ***Vinvco*** comprised between 0V to 1,3V which is difficult to get from the conventional VCO structure. Finally, the simulation results showed that the proposed design enable the stability of the output signal of voltage controlled ring oscillator in terms of control voltage variations. For more research we intend to implant this new VCO based on a ring oscillator structure for the designer of a Phase Locked Loops systems used for RF applications.

ACKNOWLEDGMENT

This work was supported by Laboratory of Electronic and Micro-technology Communication (EMC), National School Engineering of Sfax (ENIS), University of Sfax Tunisia.

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Dr. Masmoudi organised several international Conferences and has served on several technical program committees. He has served as Guest Editor for special issue for several journals.

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