A Simplified Svpwm for Five Level Inverter with DC-Link Balancing

B.Sreenivasa Raju, M.Lokesh

Abstract— The objective this paper presents a five level & three-level inverter topology for induction motor loads with dc link voltage stabilization. Presently diode-clamped inverter was used and it is also known as neutral point clamped (NPC) inverter is most favorable among various multilevel configurations. DC-link unbalance may overstress the capacitors and devices during a sudden regenerative load increase, and it can also cause nuisance over voltage or under voltage trips. A space vector based PWM scheme is proposed for power circuit configuration to have the dc link voltage balancing. This PWM scheme requires only instantaneous phase reference voltages for its implementation in the full modulation range. A SVPWM technique is also used to reduce the switching losses. In complete modulation range & power factor the capacitor voltage stabilization at the input side of the inverter is obtained. An open loop control scheme is presented, which uses only availability redundant switching states to obtain three-level inverter DC-link balancing & the current flow model of the five-level inverter to obtain the DC-link balancing. This proposed three-level inverter & five- level inverter SVPWM scheme is studied through MATLAB simulations

Index Terms— DC- link balance, Multilevel Inverter, SVPWM.

I. INTRODUCTION

The need for increased power level ac drive systems in place of conventional two-level inverter configuration is the main requirement of the present days. The standard two-level voltage source inverter is composed of only one switch cell per phase. But in the field of high power driving systems the level of dc current bus voltage constitutes an important limitation of the handled power. Another drawback of the two-level converter is very high dv/dt generated by two-level voltage source inverter. More over as the dc-link voltage of a two-level inverter is limited by voltage ratings of switching devices, the problematic series connection of switching devices is required to raise the dc link voltage. By this the maximum allowable switching frequency has to be more lowered thereby harmonic reduction becomes more difficult. Hence the need for high performance ac drive systems, at increased power level high quality inverter output with low harmonic loss and torque pulsation has arisen. Multi-level converters come as a solution to these problems. Their performance depends on the PWM method that is used.

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The blocking voltage of each switch is clamped to the half of dc-link voltage thus the multilevel inverter's performance depends on the PWM algorithm. The Space vector PWM has more advantages comparing to triangular sinusoidal and hysteresis PWM.

Several works apply the Space vector modulation to multi-level inverters [7–10]. These works use a typical method that approximates the output voltage using three nearest output vectors. When the reference vector changes from one region to another it may cause intense changes in output voltage. In addition we need to calculate the switching sequences and switching time of the states at every switching period. Thus the computation time increases with the increasing number of reference vectors. This is a main limitation to the application of typical SVPWM. Recently several attempts have been made to explore a simple, fast and generally applicable multi-level SVPWM algorithm. One of the new trends is to convert SVPWM into a new form using an appropriate coordinate system [11-15]. In [11] a method of SVPWM for high level inverters that represents output vector in three dimensional Euclidean space is presented. The method is based on the fact that increasing the number of levels by one always forms an additional hexagonal ring of equilateral triangles, which surrounds the outermost hexagon. In [12], the used method transforms the space vector diagram from Cartesian coordinates system to 60^0 coordinate system. In [13], sum manipulations allow to simplify space vector diagram of three-level inverter into space vector diagram of two-level inverter. In [14], the hexagon representing space vector diagram is flatten and the reference voltage vector is normalized in order to reduce computations of the algorithm. The method used in [15] adds to SVPWM a predictive current control loop. The load current is predicted for all output voltage vectors of the inverter. The current error is calculated and the switching state that ensures the smallest value of this error is selected. Although these methods propose general SVPWM algorithms for multi-level inverter, the coordinate transformations used in these algorithms are somewhat complicated.

In this paper a new simplified, very efficient multi-level SVM method for five-level diode clamped inverter and three-level diode clamped inverter is developed using simulink block sets of MATLAB and this algorithm is used to generate gating pulses for multi-level inverters and also the performance of the three induction motor is studied based on the developed algorithm .

II. CONVENTIONALTWO-LEVEL SPACEVECTOR MODULATION

A. Generation of the SVPWM Switching Signals:

With the three-phase Inverter shown in the fig.1, output voltage is produced by switching only one switch in each leg

at any instant of time. There are six possible switching sequences to produce an output voltage.

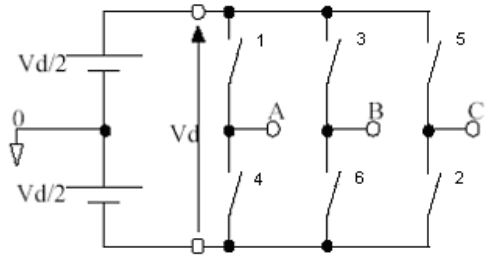

Fig.1: Three-phase inverter

The switching sequence of an inverter is in the order 1-2-3,2-3-4,3-4-5,4-5-6,5-6-1,6-1-2…. Each switch conducts over 180° in a period. This indicates the inverter in 180° mode of conduction. Switching from one sequence to another takes place at every 60 degrees. There are two more possible sequences that produce no voltage are 1-3-5 and 4-6-2. So that there 6 active states and 2 inactive states.

Space vector modulation is obtained by switching adjacent switching sequence number of times in every 60^0. Positive group switches: 1,3,5,Negative group switches: 4, 6,2. Let us assume switching vector a, b, c for the three legs represented by 1's and 0's.1 indicates positive group switches are on, 0 indicates negative group switches are on. Possible switching sequences are represented by switching vectors are shown in table 1.

S.No.	a	b	c	V_{ac}	V_{bo}	V_{co}	V_{ab}	V_{bc}	V_{ca}
1.	0	0	0	-Vd/2	-Vd/2	- Vc/2	0	0	0
2.	0	0	0	V3/2	-Vd/2	- Vc/2	Vd	0	-Vd
3	1	1	0	V3/2	Vd/2	- Vc/2	0	Vd	-Vd
4.	1	1	0	-Vd/2	Vd/2	- Vc/2	- Vd	Vd	0
5.	1	1	1	-Vd/2	Vd/2	Vd/2	- Vd	0	Vc
6.	0	0	1	-Vd/2	-Vd/2	Vd/2	0	- Vd	Vc
7.	0	0	1	V3/2	-Vd/2	Vd/2	Vd	-Vd	0
8.	1	1	1	V3/2	Vd/2	Vd/2	0	0	0

Table 1: Switching Patterns and Output Voltages of a 3-Phase Inverter

For instance, in Fig. 1 the upper switch of the inverter's pole A is on, whereas the other legs both have the lower switch turned on. Hence the pole voltages are $(\frac{1}{2}Vd, -\frac{1}{2}Vd, -\frac{1}{2}Vd)$ for poles A, B, C respectively. This state is denoted as (1,0,0) and, space vector is given by

$$\vec{V} = V_\alpha + jV_\beta = \frac{2}{3}\left(V_{AO}\vec{a}^{0} + V_{BO}\vec{a}^{1} + V_{CO}\vec{a}^{2}\right)$$

Where $\vec{a} = e^{j\frac{2\pi}{3}}$.

It is easily shown that the six non-null states called as active states, are represented by space vectors $\overrightarrow{V_k} = \frac{2}{3}V_d e^{j(k-1)\frac{\pi}{3}}$ With (k=1… 6)

forming a regular hexagon and dividing it into six equal sectors denoted as I, II, III, IV, V, VI in Fig 2.

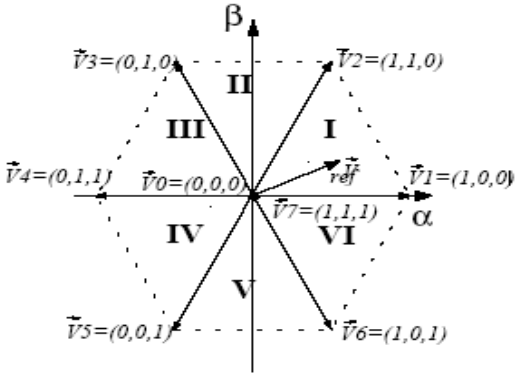

Fig 2: Representation of the Inverter States in Stationary Reference Frame

Switch State			Basic Vector	Value
A	B	C		
0	0	0	$\bar{v}_0(000)$	0
0	0	0	$\bar{v}_1(100)$	$\frac{2}{3}V_d e^{j0}$
0	0	0	$\bar{v}_2(110)$	$\frac{2}{3}V_d e^{j\frac{\pi}{3}}$
0	0	0	$v_3(010)$	$\frac{2}{3}V_d e^{j\frac{2\pi}{3}}$
0	0	0	$\bar{v}_4(011)$	$\frac{2}{3}V_d e^{j\pi}$
0	0	0	$\bar{v}_5(001)$	$\frac{2}{3}V_d e^{j\frac{4\pi}{3}}$
0	0	0	$\bar{v}_6(101)$	$\frac{2}{3}V_d e^{j\frac{5\pi}{3}}$
0	0	0	$\bar{v}_7(111)$	0

Table 2: Representation of Inverter States in Space Vectors

III. SIMPLIFIED SPACE VECTOR PULSE WIDTH MODULATION METHOD

A. Simplified SVPWM for Fiive Level Inverter:

The space vector diagram of multilevel inverter can be divided into different forms of sub-diagrams, in such a manner that the space vector modulation becomes more simple and easy to implement, as made in several works [11–15]. But these works do not reach a generalization of the two level SVPWM to the case of multilevel inverters; either they divide the diagram into triangles, or into interfered geometrical forms. In this work, we present a simple and fast method what divides the space vector diagram of five-level inverter, within two steps, into several small hexagons, each hexagon being space vector diagram of two-level inverter, as shown in Figure 3.9. This method is the extension of that presented in [16] for the case of three-level inverter. We have to make two simplifications: Firstly, the space vector diagram of five-level inverter is divided into six space vector diagrams of three-level inverters. Secondly, each one of these three-level inverter diagrams is divided into six space vector diagrams of two level inverters.

Doing so, the space vector modulation of five-level inverter becomes very simple and similar to that of conventional two-level inverter space vector modulation. To each this simplification, two steps have to be done. Firstly, from the location of a given reference voltage, one hexagon has to be selected among the hexagons secondly; we translate the origin of the reference voltage vector towards the centre of the selected hexagon. These steps are explained in the next section.

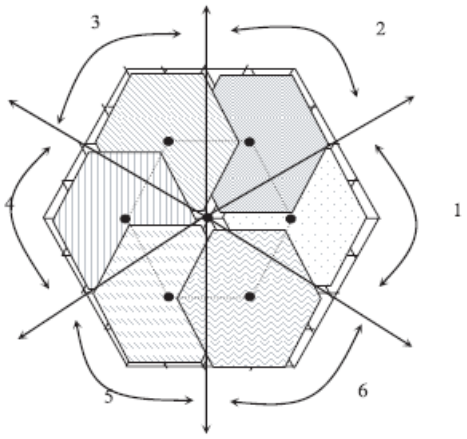

Fig 3. Division of Overlapped Regions

B. First Correction of Reference Voltage Vector:

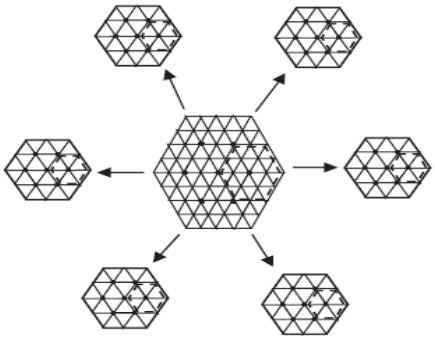

Fig 4: Decomposition of Space Vector Diagram of a Five-Level Inverter to Six Hexagons

Having the location of a given reference voltage vector, one hexagon is selected among the six small hexagons that contain the five-level space vector diagram Fig. 4. There exist some regions that are overlapped by two adjacent small hexagons. These regions will be divided in equality between the two hexagons as shown in Figure 3. After selection of one hexagon, we wake a translation of the reference vector ***V**** towards the center of this hexagon, as indicated in Figure 5. This translation is done by subtracting the center vector of the selected hexagon from the original reference vector. Table 3 gives the components *d* and *q* of the reference voltage **V**ref* after translation, for all the six hexagons.

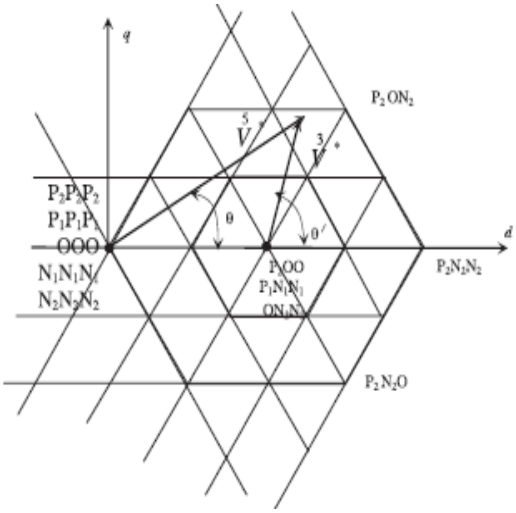

Fig 5. First Translation of Reference Voltage Vector

S	$\overset{3}{V}_d^*$	$\overset{3}{V}_q^*$
1	$\overset{5}{V}_d^* - \frac{1}{2}E.\cos(0^0)$	$\overset{5}{V}_q^* - \frac{1}{2}E.\sin(0^0)$
2	$\overset{5}{V}_d^* - \frac{1}{2}E.\cos(\pi/3)$	$\overset{5}{V}_q^* - \frac{1}{2}E.\sin(\pi/3)$
3	$\overset{5}{V}_d^* - \frac{1}{2}E.\cos(2\pi/3)$	$\overset{5}{V}_q^* - \frac{1}{2}E.\sin(2\pi/3)$
4	$\overset{5}{V}_d^* - \frac{1}{2}E.\cos(\pi)$	$\overset{5}{V}_q^* - \frac{1}{2}E.\sin(\pi)$
5	$\overset{5}{V}_d^* - \frac{1}{2}E.\cos(4\pi/3)$	$\overset{5}{V}_q^* - \frac{1}{2}E.\sin(4\pi/3)$
	$\overset{5}{V}_d^* - \frac{1}{2}E.\cos(5\pi/3)$	$\overset{5}{V}_q^* - \frac{1}{2}E.\sin(5\pi/3)$

Table 3: First Correction of Reference Voltage Vector

C. Determination of Dwelling Times:

Once the corrected reference voltage V2* and the corresponding hexagon are determined, we can apply the conventional two-level space vector PWM method to calculate the dwelling times, the only difference between the two-level SVPWM and the three-level SVPWM is the factor 4 appearing at the first two equations as shown below.

$$T_1 = 4 * \left[\frac{\left| \vec{V}^{2*} \right| \cdot T_s \cdot \sin\left(\frac{\pi}{3} - \alpha\right)}{\sin\left(\frac{\pi}{3}\right)} \right]$$

$$T_2 = 4 * \left[\frac{\left| \vec{V}^{2*} \right| \cdot T_s \cdot \sin(\alpha)}{\sin\left(\frac{\pi}{3}\right)} \right]$$

$$T_0 = T_s - T_1 - T_2$$

Remaining all procedures are implemented like conventional two-level inverter SVPWM method and two level equivalent pulses are obtained.

IV. DC-LINK BALANCING SCHEME

A three-phase -level DCMC consists of 2x(m-1)x3 switches and (m-1) capacitors in the input dc-link, as shown in Fig. 6. Theoretically, for each phase of the converter there exist $2^{(m-1)}$ different switching states. However, as it is shown here, only m switching states are valid and hence will be considered in the modeling process. If capacitors' voltages are balanced(m-1), capacitors in the dc-link will provide m different voltage levels, which are accessible by the load through the switching power converter. In DCMCs, a combination of turned-on power switches and some clamping diodes connect each output phase to one of the voltage levels provided by capacitors. The converter should be capable of operating in four quadrants that requires a switching logic. A switching state is called valid when it follows the following switching logic: "Counting from the top, at any switching instant and in each converter leg(m-1), consecutive switches are on, and all other witches in the same leg are off." As shown in Table 4, all such switching states are valid, because in this case the output voltage does not depend on the output current direction. Any other combinations of the switching states leads to surprising output voltage jumps, and also output voltage-output current dependency will occur. These voltage jumps deteriorate the output voltage quality that can

damage the load. A good modulation strategy should avoid improper switching states.

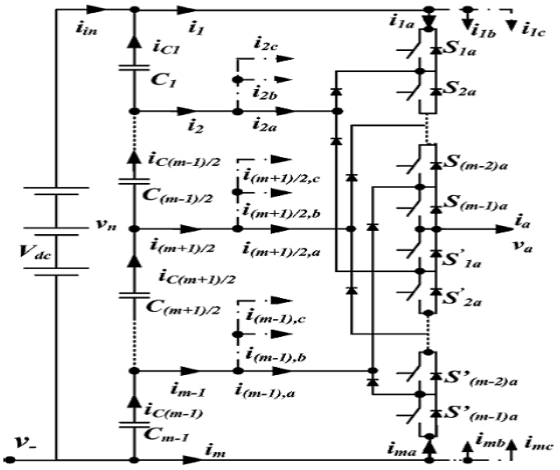

Fig 6 One Leg of three-phase, *m*-level DCMC *m* Odd

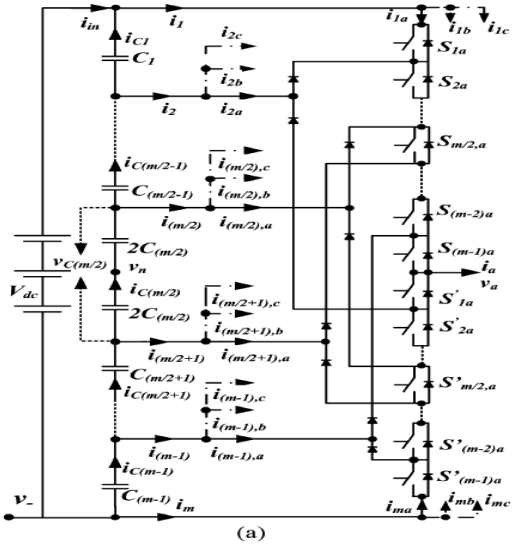

Fig 7 One Leg of three-phase, *m*-level DCMC *m* even

State	d1α	$d_{2\alpha}$		d(m-1)1α	dmα
1	1	1	…….	1	1
2	0	1	…….	1	1
. . .			. . .		
m-1	0	0	…….	0	1
m	0	0	…….	0	0

Table 4 : Definition of different switching state:

Consider an improper switching combination in a five-level DCMC, as follows:d_{1a}=1,d_{2a}=0,d_{3a}=1,d_{4a}=1, where switching functions are defined as d_{ja}=1when a switch S_{ja}=1and d_{ja}=0 when a switch S_{ja} is off, j=1….4 a positive output current results in a zero output voltage, while a negative output current results in an output voltage equal to v_{c1}+ v_{c2} that means the output voltage depends on the output current. The space vector pulse-width modulation (SVPWM) and all sinusoidal pulse-width modulation (SPWM) techniques, excluding the phase-shifted carrier SPWM, generate valid switching states. Table 4 shows all switching states of an-level DCMC that satisfy the aforementioned switching rule and Table 5 shows the corresponding output voltages and MP currents. Therefore, regardless of the modulation technique used for the converter, as long as the modulation technique generates valid switching states, the switching combinations are limited to the switching states shown in Table 4. Consequently, it is possible to claim that for any possible switching states the currents and voltages are formulated as shown in Table 5.

State	i_{1a}, i_{2a},……i_{ma}	V_{an} (m=odd)	V_{an} (m=even)
1	i_a o ……..o	$\sum_{j=1}^{\frac{m-1}{2}} v_{cj}$	$\frac{1}{2}v_c\frac{m}{2}+\sum_{j=1}^{\frac{m}{2}-1} v_{cj}$
2	o i_a……..o	$\sum_{j=2}^{\frac{m-1}{2}} v_{cj}$	$\frac{1}{2}v_c\frac{m}{2}+\sum_{j=2}^{\frac{m}{2}-1} v_{cj}$
. . .	. . .	. . .	. . .
m	o o …….. i_a	$\sum_{j=\frac{m+1}{2}}^{m-1}(-v_{cj})$	$-\frac{1}{2}v_c\frac{m}{2}-\sum_{j=\frac{m}{2}+1}^{m-1} v_{cj}$

Table 5 : DCMC Output voltages and MP Currents for all states:

We propose a new, general, and simple current flow model or, equivalently, a switching function model. The advantage of this new modeling scheme is that it achieves generality without the loss of simplicity. In our analysis, all equations are derived for phase "a" and then extended for three phases. From Table II the currents as i_{1a}..... i_{ma} can be written as

$$i_{1a}=d_{1a}i_a,\quad i_{ma}=(1-d_{(m-1)a})i_a$$
$$i_{ka}=d_{ka}(1-d_{(k-1)a})i_a;\ k=1,....,m-1 \quad \text{---(1)}$$

Where d_{ja}(j=1…4)are switching functions pertinent to leg "a" that can take zero or one value. Applying KCL at the capacitors' middle points.

$$i_{ck}=\sum_{j=1}^{k} i_{ja}-i_{in};\quad k=1,....,m-1 \text{ ……..(2)}$$

By defining d_{0a} = 0 and using (1) and (2), one can obtain the following set of equations:

$$i_{ck}=\sum_{j=1}^{k} d_{ja}(1-d_{(j-1)a})i_a-i_{in};\ k=1,....,m-1 \text{ ….(3)}$$

Using KVL in the dc-Link $vd.c=\sum_{j=1}^{m-1} vcj$ $vd.c=\sum_{j=1}^{m-1} vcj$ taking the derivative of both sides results in

$$\frac{dV_{dc}}{dt}=\sum_{j=1}^{(m-1)}\frac{dV_{cj}}{dt}\Rightarrow\sum_{j=1}^{(m-1)}\frac{i_{cj}}{C_j}=0 \text{ …..(4)}$$

The input current i_{in} can easily be found by combining (3) and (4) as shown in the following

$$\sum_{k=1}^{(m-1)}\sum_{j=1}^{k} d_{ja}(1-d_{(j-1)a})\frac{i_a}{C_k}-\sum_{k=1}^{(m-1)}\frac{i_{in}}{C_k}=0 \text{ …..(5)}$$

Therefore, assuming

$$C_{tot}=1\Big/\sum_{k=1}^{m-1}(1/C_k)\quad,$$

$$i_{in}=C_{tot}\sum_{k=1}^{(m-1)}\sum_{j=1}^{k} d_{ja}(1-d_{(j-1)a})\frac{i_a}{C_k} \text{ …..(6)}$$

We further propose a Lemma that plays a key role in simplifying (3) and (6) and thus the proposed modeling scheme. Lemma 3.1: For valid switching states, the following equation holds true:

$$\sum_{j=1}^{k} d_{ja}\left(1-d_{(j-1)a}\right)=d_{ka} \quad .....(7)$$

The same procedure can be used to derive analogous equations for the other two phases (phases "b" and "c"). For the three-phase system, with the help of Lemma 3.1, (3) and (7) are simplified as follows:

$$i_{in}=C_{tot}\left(i_a\left(\sum_{i=1}^{m-1}\frac{d_{ia}}{C_i}\right)+i_b\left(\sum_{i=1}^{m-1}\frac{d_{ib}}{C_i}\right)+i_c\left(\sum_{i=1}^{m-1}\frac{d_{ic}}{C_i}\right)\right) \quad \textbf{--(8)}$$

$$i_{cj}=d_{ja}i_a+d_{jb}i_b+d_{jc}i_c-i_{in}$$

$$=\left(d_{ja}-C_{tot}\sum_{i=1}^{m-1}\frac{d_{ia}}{C_i}\right)i_a+\left(d_{jb}-C_{tot}\sum_{i=1}^{m-1}\frac{d_{ib}}{C_i}\right)i_b+\left(d_{jc}-C_{tot}\sum_{i=1}^{m-1}\frac{d_{ic}}{C_i}\right)i_c, \quad j=1,\ldots,(m-1)$$

This model is valid for the SVPWM and all SPWM techniques excluding the phase shifted carrier. Therefore, (8) is independent of modulation strategies. Moreover, it is important to note that in deriving (8) there was no assumption on the capacitors' voltages or capacitors' values. Thus, the equations in (8) hold true even if the capacitor voltages or values are not equal. If v_n is midpoint of the dc link capacitors as shown in Fig. 7, using Table 4, the following equations can be derived for odd and even number of levels:

$$v_a-v_n=\sum_{j=1}^{\frac{m-1}{2}} d_{ja}v_{cj}+\sum_{j=\frac{m+1}{2}}^{m-1}\left(d_{ja}-1\right)v_{cj} \quad .....(9)$$

$$=\sum_{j=1}^{m-1} d_{ja}v_{cj}-\sum_{j=\frac{m+1}{2}}^{m-1}v_{cj} \quad \text{if m is odd}$$

$$v_a-v_n=\sum_{j=1}^{\frac{m-1}{2}} d_{ja}v_{cj}+v_{c\frac{m}{2}}\left(d_{\frac{m}{2}a}-\frac{1}{2}\right)+\sum_{j=\frac{m}{2}+1}^{m-1}\left(d_{ja}-1\right)v_{cj} \quad .....(10)$$

$$=\sum_{j=1}^{m-1} d_{ja}v_{cj}-\sum_{j=\frac{m}{2}+1}^{m-1}v_{cj}-\frac{1}{2}v_{c\frac{m}{2}}, \quad \text{if m is even.}$$

On the other hand, the voltage difference between n and the negative point of the dc source is obtained from

$$v_n-v_-=\sum_{j=\frac{m+1}{2}}^{m-1}v_{cj}, \quad \text{if m is odd} \qquad ..(11)$$

$$v_n-v_-=\sum_{j=\frac{m}{2}+1}^{m-1}v_{cj}+\frac{1}{2}v_{c\frac{m}{2}}, \quad \text{if m is even.}$$

By comparing (4.17)–(4.19), it can be observed that the following equation is true for both even and odd m:

$$v_a-v_-=\sum_{j=1}^{m-1} d_{ja}v_{cj} \qquad \textbf{---(12)}$$

Based on (8) and (12), the switching function model of the three-phase DCMC is derived and demonstrated in Fig.8. For the sake of simplicity, it is assumed that all dc link capacitors are equal . The current flow model formulates the capacitor currents as well as input dc current as a function of the switching functions and output currents. This relation provides that take place in the converter structure and helps to predict the performance of the converter. The current flow model, as can be seen from Fig. 8, is very simple and straightforward, thus can be used in any simulation software instead of the converter itself and considerably reduces the simulation run time and eliminates any convergence problem. Moreover, it provides an easy-to-design tool for the design and performance evaluation of the converter and its control mechanism. To demonstrate the effectiveness of the model and to show how it simplifies the calculations and predicts the overall performance, the derivation of the average current passing through capacitors in a five level DCMC is given as an example. For the SPWM strategy, the switching signals, d_{ja} j=1…4 are found and shown in Fig. 7. By neglecting higher order harmonic components in this signal can be approximated by the following function:

$$d_{1a}=\begin{cases}2m_a\sin(\omega t)-1, & \text{if } \alpha<\omega t<\pi-\alpha\\ 0, & \text{otherwise}\end{cases} \quad .....(13)$$

Where m_a is modulation index and $\alpha\sin^{-1}(1/2m)$ a) . Similar equations can be found for d_{1b} and d_{1c} . For sinusoidal output currents ($i_a(t)=I.\sin\omega t-\varphi$), the current flow model shown in Fig. 8 and (13) result in an average capacitor current given by

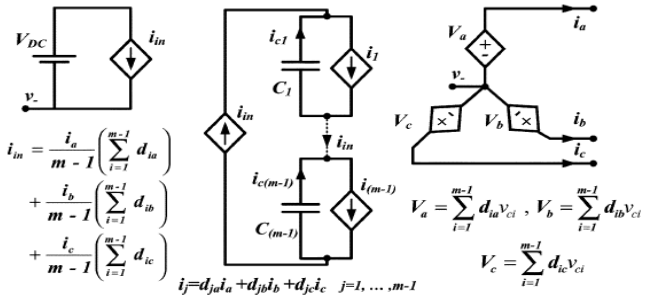

Fig 8: Proposed current flow model of an m-level DCMC

$$\bar{I}_{c1a}=\frac{3}{2\pi}\int_{\alpha}^{\pi-\alpha}\left(2m_a\sin(\omega t)-1\right)\left(\hat{I}\sin(\omega t-\phi)\right)d(\omega t)-\bar{I}_{in} \qquad \text{--(14)}$$

$$P_{in}(t)=P_{3-phase}(t)\Rightarrow\bar{I}_{in}=\frac{P_{out}^{3ph}}{V_{DC}}=\frac{3}{4}m_a\hat{I}\cos(\phi) \qquad \text{--(15)}$$

According to (14) and (15), the average current is found from

$$\bar{I}_{c1a}=\frac{3\hat{I}\cos(\phi)}{4\pi m_a}\left[m_a^2\pi-\sqrt{4m_a^2-1}-4m_a^2\sin^{-1}\left(\frac{1}{2m_a}\right)\right] \quad ..(16)$$

Fig. 9 depicts the normalized average currents, $I_c/(3I\cos(\varphi))$, as a function of m_a, and demonstrates that with the phase opposition disposition (POD) modulation strategy, the capacitors $C_1$and C_4 (C_2 and C_3) are being charged (discharged) all the time regardless of the modulation index. Similar results are obtained in the literature but with much more effort and calculations involved. The proposed current flow model paves the road for us to develop a new voltage balancing strategy based on SVM which is proposed.

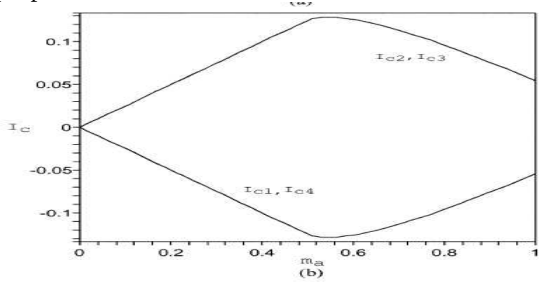

Fig 9 Capacitors average currents

V. MATLAB/SIMULINK RESULTS

The below Figure 9 shows the proposed system which is designed in MATLAB.

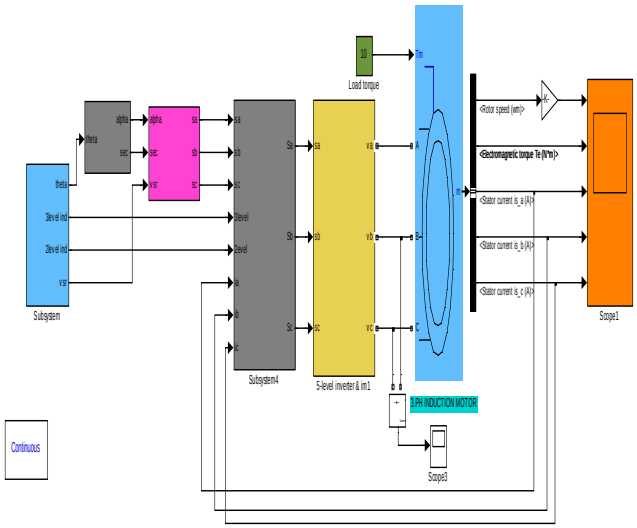

Fig 9-MATLAB/SIMULINK MODEL OF THE PROPOSED SYSTEM

Figure 10 Shows the Five-level inverter output voltage at 0.6 modulation index at 0.3 power factor (No-Load)

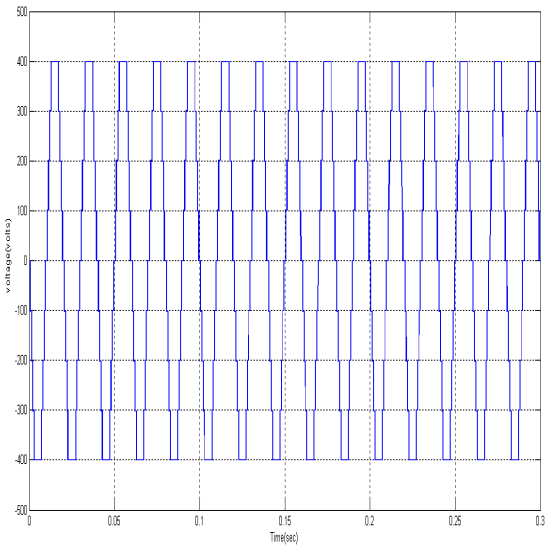

Fig 10. Five-level inverter

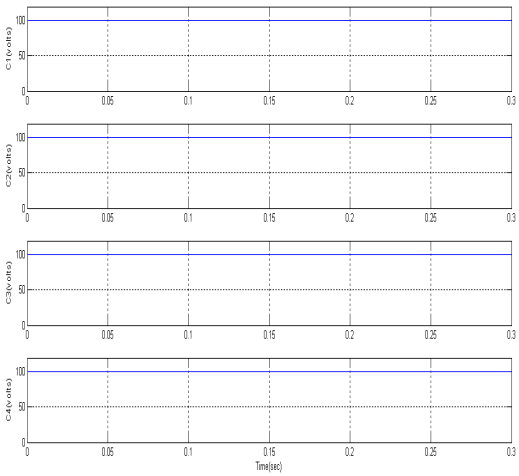

Fig 11. Five-level inverter fed DC-Link capacitor voltage

Above Shows the Five-level inverter fed DC-Link capacitor voltage at 0.6 modulation index ,0.3 power factor (No-Load)

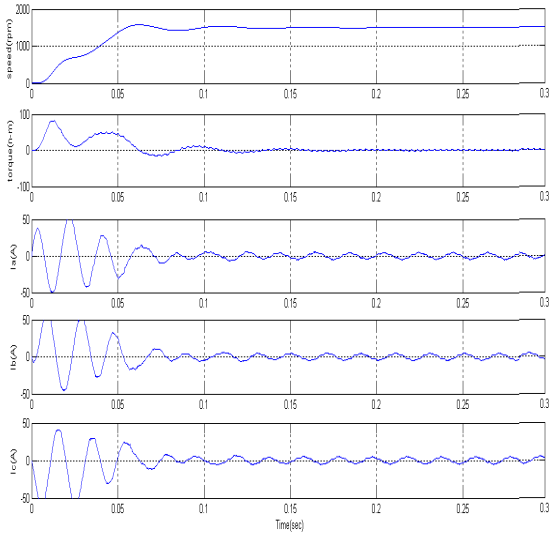

Fig 12 - Five-level inverter fed induction motor Characteristics.

Figure 12 Shows the Five-level inverter fed induction motor characteristics & stator currents at 0.6 modulation index, 0.3 power factor (No-Load)

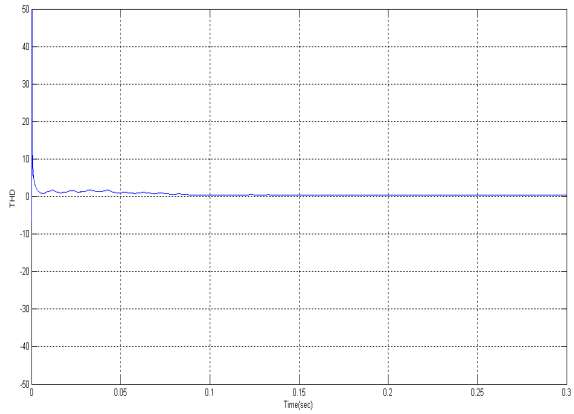

Fig 13. Five-level inverter output voltage THD

Above Shows the Five-level inverter output voltage THD at 0.6 modulation index,0.3 power factor (No-Load)

VI. CONCLUSION

In this paper a simplified Space Vector Pulse Width Modulation (SVPWM) algorithm has been described and applied to Five-Level Inverter & in addition to this DC-link balancing method is also adopted. Through the decomposition of the Space Vector diagram the complicated Five-Level Space Vector Modulation algorithm is simplified into two level cases. This simplified method has the following advantages. It reduces the execution time of the five-level inverter modulation. It allows having memory of the controller in case of experimental realization. DC-link balancing method adopted for three-level inverter is most effective and balancing can be obtained for complete modulation index range. The generalized current flow model of multilevel inverter & its cost function is used for DC-link balancing of five-level inverter. The most important aspect of this algorithm lies in its generality. It can be used in any high-level inverter.

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