

# Improving the Response of a DC/DC Converter by Providing a New Structure for Embedded Schottky Diode

Hamed Sepahvand, Soghra Raisi

**Abstract—** Paper In this paper, a new schottky diode with high speed switching is presented. Reverse recovery current and reverse recovery time are two parameters to determine the switching speed of power diodes. If a method could control the depletion of majority carriers in cut off time, it can enhance the switching speed. In this work, some islands, with non-similar type to bulk, are implemented in the bulk of the diode. These islands can gather and recombine the abandon majority carriers. So, the reverse recovery current can be limit by this way. To test this structure a simple fast schottky diode is applied in a DC/DC converter. The simulations are done in Silvaco software.

**Index Terms—** Schottky diode, Reverse recovery, DC/DC converter, Recombination.

## I. INTRODUCTION

Today, Schottky diodes are widely used in industrial [1]. The main advantage of the Schottky diode relate to a  $p-n$  diode is reverse recovery current and time; when the diode switches from conducting to cut off state [2]. In a  $p-n$  diode the reverse recovery time can be in the order of hundreds of nanoseconds and less than 100 ns for fast diodes, this time is very small for Schottky diodes, because there is no charge carrier depletion region at the junction [3]. The switching time is up to tens of nanoseconds for special high-capacity power diodes. EMI noise will be increased in high power devices by high reverse recovery current. With Schottky diodes switching essentially instantly with only slight capacitive loading, this is much less of a concern. It is often said that the Schottky diode is a "majority carrier" semiconductor device. This means that if the semiconductor body is doped  $n$ -type, only the  $n$ -type carriers (mobile electrons) play a significant role in normal operation of the device. The majority carriers are quickly injected into the conduction band of the metal contact on the other side of the diode to become free moving electrons. The bulk is largest part of a diode, so, the carriers must cross to reach the end of device, in a long distance. It causes to a delay and maybe returns the carriers to reach the junction in  $p-n$  diodes. But in the schottky diode there isn't any bulk in the metal side. Therefore no slow, random recombination of  $n$ - and  $p$ - type carriers is involved, so that this diode can cease conduction

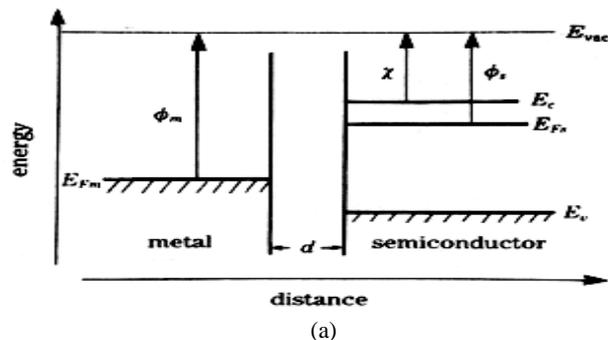
faster than an ordinary  $p-n$  rectifier diode [4]. This property in turn allows a smaller device area, which also makes for a faster transition. This is another reason why Schottky diodes are useful in switch-mode power converters; the high speed of the diode means that the circuit can operate at frequencies in the range 200 kHz to 2 MHz, making possible the use of small inductors and capacitors with greater efficiency than would be possible with other diode types [5].

The metal-semiconductor junction that leads to Schottky diode is one of the oldest semiconductor structures. Applying this structure returns to pre-1900. The action of the potential barrier at the surface of the semiconductor space charge was realized in 1938 separately by Schottky [6] and Mott [7]. In the recent years, some works are done to improve the power schottky diode performance. This work focuses on structures that increase the switching speed of schottky diode. Sic diode among other structures is faster and can sustain higher reverse voltage [8]-[9]. In DC/DC inverters the switching speed influence on output DC level. In [10] a good structure is presented which reduce the forward resistance. So, the output response of inverter is improved.

In this work, a new structure is presented that can decrease the reverse recovery current in a schottky diode. This approach is earned by make some islands in the diode structure. They can recombine the majority carriers when the diode will cut off. This structure is applied in a DC/DC inverter to show its performance. This method is a general and it can be used in any structure to deplete the carriers in order to decrease the reverse recovery current. Actually, this work presents a method to decrease the reverse recovery time and especially current.

## II. BASIC PRINCIPLE OF SCHOTTKY DIODE AND DC/DC CONVERTER

After contact between metal and semiconductor a schottky barrier will be implemented. It prevents the crossing of electrons from metal to semiconductor. Fig.1 shows this phenomenon.



Manuscript published on 30 August 2013.

\* Correspondence Author (s)

Hamed Sepahvand\*, Department of Electrical and Electronic, Abadan Branch, Islamic Azad University, Abadan, Iran.

Soghra Raisi, Department of Electrical and Electronic, Shoushtar Branch, Islamic Azad University, Shoushtar, Iran.

© The Authors. Published by Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP). This is an open access article under the CC-BY-NC-ND license <http://creativecommons.org/licenses/by-nc-nd/4.0/>.

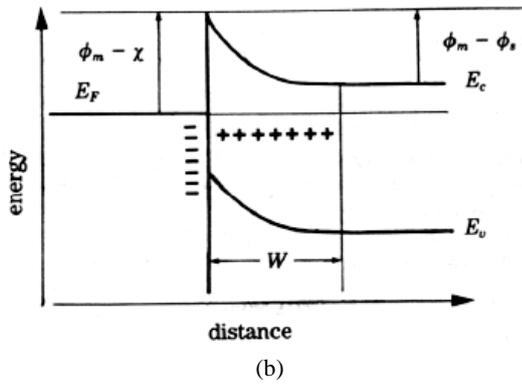


Fig.1. Energy diagram of metal and semiconductor  
a) before contact b) after contact [11]

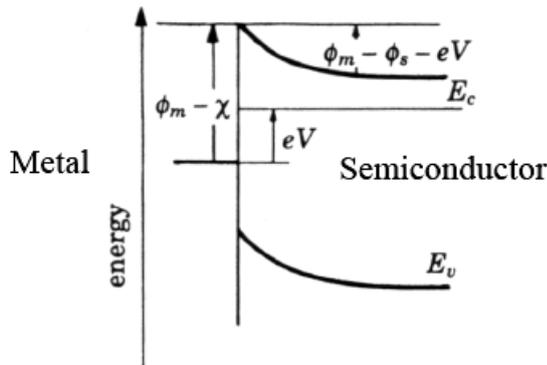


Fig.2. Energy diagram in forward bias

If a positive bias voltage will be exerted to the metal, width of the depletion region and Potential barrier are reduced and electrons are flowing from the semiconductor to the metal as shown in Fig. 2.

In most switching applications, a diode is switched from direct bias to reverse mode and to the contrary. An important result is that a much larger current than reverse saturation current of the diode, during the time required for the displacement of the stored charge, can be passed from diode. If a Schottky diode be stimulated by a square wave between  $-E$  to  $E$  and frequently switched, like Fig. 3, whereas  $E$  is positive, the diode current  $I_f$  will pass. If  $E$  is much more than a schottky junction potential, the current will be  $E/R$ . After reversal of the supply voltage, the current must reach to  $-E/R$ . this large reverse current is due to the stored charges that can't change instantaneously. Hence, as soon as reverse current flows, low voltage of forward bias in junction remains the same. The KVL in the loop show the value of reverse current as  $-E/R$ , it will pass temporary. Because of negative value of current through the schottky junction, the  $\Delta p$  slope in boundary must be positive.

After depletion of stored charge near the junction, the below equation can calculate the potential junction [Error! Bookmark not defined.].

$$\Delta p_n(t) = p_n \left( e^{qV(t)/kT} - 1 \right) \quad (1)$$

According to equation (1) when the  $\Delta p_n$  is positive the  $V(t)$  must be more than zero and small. So, the current will be  $-E/R$  till  $\Delta p_n$  approach to zero.

When the stored charge depleted and  $\Delta p_n$  be negative, the junction gets a negative potential and due to a big potential in junction the total voltage may divided between junction and

R. By increase in time the value of voltage on junction will increase and the reverse current will fall to reverse saturation current. The required time for depletion of stored time is named as storage delay time ( $t_{sd}$ ). This delay time plays a significant role to evaluate diodes in switching applications. The  $t_{sd}$  is depended to life time of the carriers. The exact solution to calculate the  $t_{sd}$  is so complicated. But assuming a semi-stable state can estimate to reach an easier conclusion.

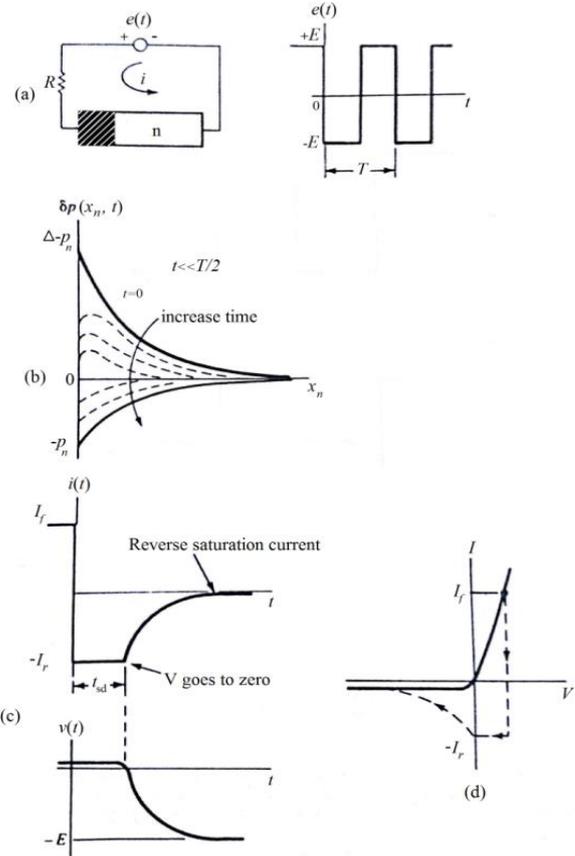


Fig.3. Storage delay time in a schottky diode

- a) a circuit for input square wave
- b) hole distribution in n region as a function of time in transient mode
- c) transient variation of voltage and current
- d) current versus voltage by I-V characteristics

Now, to start the calculating of  $t_{sd}$ , at first the equation (2) show the current in a schottky junction:

$$i(t) = \frac{Q_p(t)}{\tau_p} + \frac{dQ_p(t)}{dt} \quad Q_p = I_f \tau_p \quad (2)$$

By Laplace transform,

$$-\frac{I_r}{s} = \frac{Q_p(s)}{\tau_p} + sQ_p(s) - I_f \tau_p \quad (3)$$

$$Q_p(s) = \frac{I_f \tau_p}{s + 1/\tau_p} - \frac{I_r}{s(s + 1/\tau_p)}$$

Therefore,



$$Q_p(t) = I_p \tau_p e^{-t/\tau_p} + I_r \tau_p (e^{-t/\tau_p} - 1) \tag{4}$$

$$= \tau_p [-I_r + (I_f + I_r) e^{-t/\tau_p}]$$

By assuming the  $Q_p(t) = qAL_p \Delta p_n(t)$  and Shockley relation, can be say:

$$\Delta p_n(t) = \frac{\tau_p}{qAL_p} [-I_r + (I_f + I_r) e^{-t/\tau_p}] \tag{5}$$

By determine equation--- to zero in  $t = t_{sd}$ :

$$t_{sd} = -\tau_p \ln \left[ \frac{I_r}{I_f + I_r} \right] = \tau_p \ln \left( 1 + \frac{I_f}{I_r} \right) \tag{6}$$

This equation shows a direct relation between life time and  $t_{sd}$ . So, to reduce the storage delay time, that lead to reverse recovery current, can be reduce the life time by adding some recombination centers in semiconductor part. Fig. 4 shows the  $t_{sd}$  for a schottky diode with square wave input.

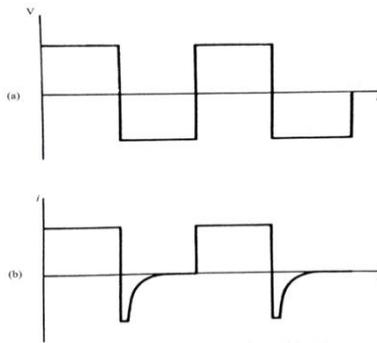


Fig.4. The effect of storage delay time on switching signal  
a) switching voltage b) diode current

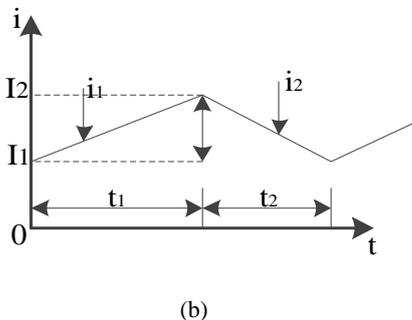
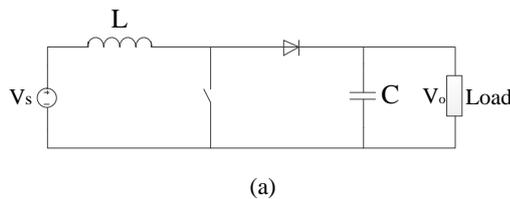


Fig.5. a) a chopper (DC/DC converter) in boost mode,  
b) current of the inductor

As mentioned above, when the diode placed in reverse bias after forward bias, some of the majorities carriers that have not yet entered in the depletion region will return and make reverse recovery current. If these carriers can be eliminated by a method, their destructive effect in applications such as a DC/DC converter will be deleted. Reverse recovery current

through the output capacitor will reduce the output DC voltage level. This leads to requiring a larger inductor to achieve the desired voltage. Fig. 5 shows a chopper in boost mode.

The output voltage is calculated by the following equation:

$$V_o = V_s + L \frac{\Delta I}{t_2} = V_s \left( 1 + \frac{t_1}{t_2} \right) \tag{7}$$

$$= V_s \left( \frac{1}{1-K} \right)$$

Where  $K$  is calculated by  $\tag{7}$

$$K = t_1 / T = \frac{t_1}{t_1 + t_2} \tag{8}$$

The hardware or actually applied schottky diode, limits the value of  $K$ . According to equation (7), if  $K$  value increases above 0.5, the  $V_o$  voltage increase more than  $V_s$ . In following a sample schottky diode is applied in this DC/DC converter.

### III. PROPOSED STRUCTURE

It is expected that a new structure can increase the output DC level by decreasing the reverse recovery current. Fig. 6 shows a sample schottky diode structure [12].

As is mentioned above, reverse recovery current cause to decrease the output DC voltage. Because, abandon carriers moves in opposite direction and depletes the capacitor.

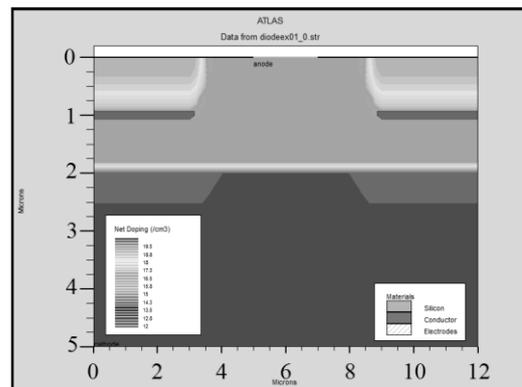


Fig.6. A sample schottky diode structure

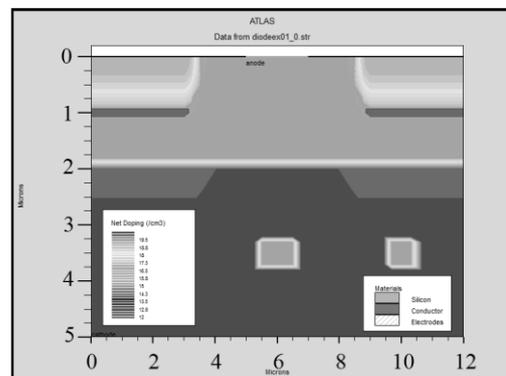


Fig.7. Proposed schottky diode structure

In this work, some *p*-type islands are built in *n*-region. They can collect and recombine the abandon carriers. However, this method is limited only by the size and number of islands. If the number and size of the islands increases, inordinately, tolerated reverse voltage is reduced. Thus, small size and low number will be selected. Fig. 7 shows the proposed structure with islands to collect the carriers and decrease the reverse recovery current.

In this structure the ring contacts and  $n^+$  junctions beneath them have been considered. The reason for choose a ring is eliminating the edge effect in high fields [Error! Bookmark not defined.]. Three recombination centers (islands) are embedded in *n*-region to recombine the abandon majority carriers. The distance and size of islands determine by considering to no change in maximum reverse voltage and approximately 80% recombination. Simulation results show the performance of this new structure well.

IV. SIMULATION RESULTS

To show the reverse recovery current, a circuit shown in Fig. 8 is suggested. In this circuit, the value of R2 varies from 1MΩ to 1mΩ, instantly. In this case, the current of the current source is passed through the R2 and Vs source places the diode in reverse bias.

Table 1 present the values of parameters in the reverse recovery test circuit.

Fig. 9 shows the varying of diode current by varying the value of R2. Be careful that the value of R2 is varied, instantly.

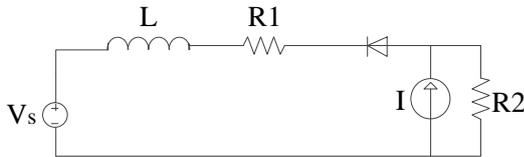


Fig.8. A sample circuit to show reverse recovery time and current of schottky diode

Table 1.Values of parameters in the reverse recovery test circuit

Parameter	value
L	3nH
R1	1mΩ
R2	1MΩ to 1mΩ
I	500A
Vs	1200V

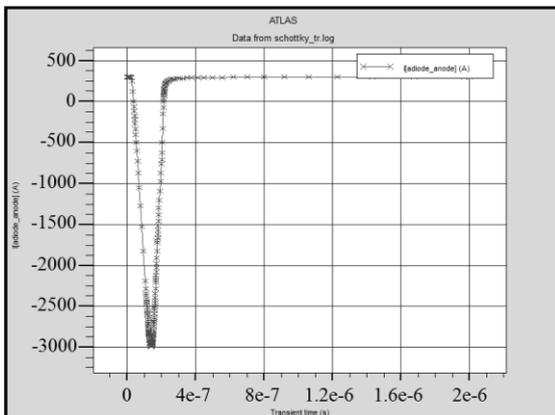


Fig.9. Reverse recovery of sample schottky diode in test circuit

Now, this diode is applied in a chopper circuit like Fig. 5 that its parameters are listed in Table 2. The output voltage in an 8Ω load presented in Fig. 10. The *K* value is calculated 0.52. Now, the new structure diode (Fig. 7) is applied in the test circuit of Fig. 8. Its reverse recovery current and time are presented in Fig. 11.

The reverse recovery current is decreased till about 90%. Now, if the diode apply in the chopper circuit the output can chive to a higher DC level. This improvement in output response is the result of collecting the abandon carriers. Fig. 12 shows a 35% increase in output DC voltage.

Table 2.Values of parameters in the chopper circuit

Parameter	value
L	48mH
F	2KHz
Vs	96V
Time constant of the Load	6ms

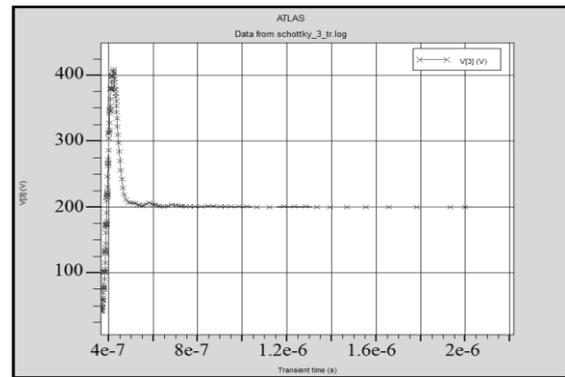


Fig.10. output voltage of chopper circuit with sample schottky diode

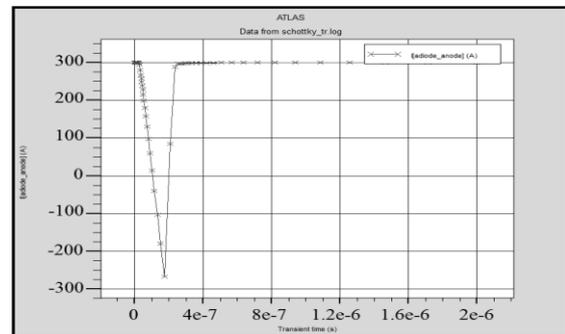


Fig.11. Reverse recovery of proposed schottky diode in test circuit

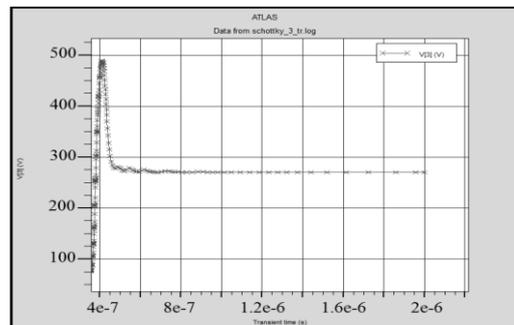


Fig.12. Output voltage of chopper circuit with proposed schottky diode



## V. CONCLUSIONS

Eliminating the DC/DC converters problems plays a significant role in industry. In this work, was tried to analyze the reverse recovery in schottky diode as a particular part of a DC/DC converter. A test circuit was suggested to show reverse recovery current and time. By making some islands in *n*-region of diode, the reverse recovery current was decreased. By embedding the new schottky diode in a chopper, the DC level of output voltage increased about 35% in relation with conventional structure.

## REFERENCES

- [1] Yan Liu, Zhitang Song, Houpeng Chen, Guangping Wu, Chao Zhang, Lianhong Wang, Lei Wang, Songlin Feng, "Schottky-barrier diode array fabrication with self-aligned Ni silicidation for low power phase-change memory application", 2012 International Workshop on Information Storage and Ninth International Symposium on Optical Storage, Fuxi Gan; Zhitang Song, Shanghai, China | October 21, 2012.
- [2] G. Spiazzi, S. Buso, M. Corradin, "Performance evaluation of a Schottky SiC power diode in a boost PFC application", Power Electronics, IEEE Transactions on, Volume:18 Issue:6. Nov. 2003.
- [3] B. Ozpeneci, L. M. Tolbert, "Comparison of Wide-Band gap Semiconductors for Power Electronics Applications", Oakridge National Laboratory, Dec. 2003.
- [4] B. Ozpineci, A. M. Tolbert, "Characterization of SiC Schottky diodes at different temperatures", Power Electronics Letters, IEEE, Volume:1, Issue: 2, June 2003.
- [5] Seong- Jin Kim "Breakdown Voltage Characteristics of SiC Schottky Barrier Diode with Aluminum Deposition Edge Termination" Woosuk University Journal of the Korean Physical Society pp. S768 – S773 Vol 49 Dec 2006.
- [6] W. Schottky, *Naturwissenschaften*, 26, 843 (1938).
- [7] N. F. Mott, "Note on the contact between a metal and an insulator on semiconductor," *Proc. Camb. Phi/os.Soc.*, 34, 568(1938).
- [8] Francesc N. Masana, "SiC Schottky Diode Electrothermal Macromodel" *Microelectronics Reliability*, Vol. 47, No 12, pp 2122-2128, Dec. 2011.
- [9] G. Majumdar and T. Oomori, "Some key researches on SiC device technologies and their predicted advantages", *Power Semiconductors* 6, 18–229 (2009).
- [10] T. Nakamura, M. Aketa, Y. Nakano, M. Sasagawa, T. Otsuka, "Novel developments towards increased SiC power device and module efficiency", Energytech conference, ISBN:978-1-4673-1836-5, May 2012
- [11] E. M. Sze, *Physics of semiconductor devices*, 2<sup>nd</sup> Ed., Wiley, New York, 1980.
- [12] Marc C. Tarplee "Design Rules for Field Plate Edge Termination in SiC Schottky Diodes" *IEEE Transactions on Electron Devices* Vol 48. No. 12, pg. 2659-2654 December 2001.

**Hamed Sepahvand** received B.S.c and M.S.c degree in electrical engineering from the Shahid Chamran University, Ahvaz, Iran 2007 and 2010 respectively. In 2011, joined the Islamic Azad University- Abadan Branch as a Lecturer.

**Soghra Raisi** received the B.S.c in electrical engineering from Isfahan University of Technology, Isfahan, Iran, in 2007 and the M.S.c. in electrical engineering from Shahid Chamran University, Ahvaz, Iran, in 2010. In 2011, joined the Islamic Azad University- Shoushtar Branch as a Lecturer.