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Review on: Low Power VLSI Design of Modified Booth Multiplier

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***Abstract*— Low power VLSI circuits became very vital criteria for designing the energy efficient electronic designs for prime performance and compact devices. Multipliers play a very important role for planning energy economical processors that decides the potency of the processor. To scale back the facility consumption of multiplier factor booth coding methodology is being employed to rearrange the input bits. The operation of the**

***booth decoder is to rearrange the given booth equivalent. Booth decoder can increase the range of zeros in variety. Hence the switching activity are going to be reduced that further reduces the power consumption of the design. The input bit constant determines the switching activity part that's once the input constant is zero corresponding rows or column of the multiplier ought to be deactivated. When multiplicand contains more number of zeros the higher power reduction can takes place. So in modified booth multiplier high power reductions will be achieved*.**

***Keywords*—Digital signal processing(DSP); Carry Save Adder(CSA); Full Adder(FA),Column Bypass Multiplier(CBM)**

I. INTRODUCTION

Portable multimedia and digital signal processing (DSP) Systems, which typically require flexible processing ability, Low power consumption, and short design cycle, have Become increasingly popular over the past few years. Many Multimedia and DSP applications are highly multiplication Intensive so that the performance and power consumption of These systems are dominated by multipliers. The computation of the multipliers manipulates two input data to generate many partial products for subsequent addition operations, which in the CMOS circuit design requires many switching activities. Thus, switching activity within the functional unit requires for majority of power consumption and also increases delay. Therefore, minimizing the switching activities can effectively reduce power dissipation and increase the speed of operation without impacting the circuit's operational performance. Besides, energy - efficient. Multiplier is greatly desirable for many multimedia applications [6],[9]. Multiplication is an expensive and time consuming operation. The performance of many computational problems is dominated by the speed at which a multiplication operation can be executed [20]. This observation has for instance prompted integration of complete multiplication unit in state of art digital signal processors and microprocessors. Multipliers are in effect complex adder.

Arrays. The analysis of multiplier is carried out to optimize the performance of complex circuit topologies. The simplest and most popular multiplication method is added and shift algorithm [21] . In parallel multipliers numbers of partial products to be added is the main parameter that determines the performance of multiplier.

The number of gates per chip area keeps on increasing, while the gate switching energy does not decrease at the same rate. So the power dissipation rises and removal of heat becomes difficult and expensive. The dynamic power of CMOS circuits is becoming a major concern in the design of devices. There are different multiplier structures which can be classified as Serial Multipliers, Parallel multipliers, Array multipliers, Tree multipliers and so on[24],[25]. Multipliers are categorized in relative to their architecture, applications, and the way of producing partial products and summing up of partial products to produce the final result.

Low power multipliers with high clock frequencies play an important role in today's digital signal processing [3],[5],[6].Digital signal processing (DSP) is the technology at the heart of the next generation of personal mobile communication systems.

To reduce the power consumption of digital multipliers based on row by pass scheme a method was proposed[14].Even though it eliminates redundant signal transitions using bypassing technique but it needs extra circuits.In an array multiplier, futile computations occur on those columns or rows of adder corresponding to zero bits in the input operands. To save the power, we must first disable the futile computation and second bypass results from the previous stage [8],[13]. The computation can be disabled by either freezing its inputs or gating the logic evaluation. The former approach requires either input gating or multiplexing circuits while the latter approach needs extra gating logic along the evaluation path. The output signal bypassing must be realized by a multiplexer.

II LITERATURE SURVEY

A. Array multiplier

Array multiplier is an efficient layout of a combinational multiplier. Multiplication of two binary number can be obtained with one micro-operation by using a combinational circuit that forms the product bit all at once thus making it a fast way of multiplying two numbers since only delay is the time for the signals to propagate through the gates that forms the multiplication array. With its good structure, this multiplier is based on the standard add and shift operations. Each partial product is generated by taking into account the multiplicand and one bit of multiplier each time.

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The impending addition is carried out by high-speed carry-save algorithm and the final product is obtained employing any fast adder – the number of partial products depends upon the number of multiplier bits.
Conclusion: Array Multiplier gives more power consumption as well as optimum number of components required, but delay for this multiplier is larger. It also requires larger number of gates because of which area is also increased; due to this array multiplier is less economical [17] [23].Thus, it is a fast multiplier but hardware complexity is high [11].

B. Wallace Tree Multiplier

A fast process for multiplication of two numbers was developed by Wallace [21]. Using this method, a three step process is used to multiply two numbers; the bit products are formed, the bit product matrix is reduced to a two row matrix where sum of the row equals the sum of bit products, and the two resulting rows are summed with a fast adder to produce a final product. In this architecture, all the bits of all partial products in each column are added together to a set of counters in parallel without propagating the carries. Another set of counters reduces this new matrix until a two row matrix is generated. A fast adder is at the end produces the final result.
Conclusion: In the Wallace tree method, the circuit layout is not easy although the speed of the operation is high since the circuit is quite irregular [20]. Wallace tree styles are generally avoided for low power applications, since excess of wiring is likely to consume extra power.

C. Baugh Wooley Multiplier

Baugh-Wooley Two's compliment Signed multipliers is the best known algorithm for signed multiplication because it maximizes the regularity of the multiplier and allow all the partial products to have positive sign bits[5].Baugh–Wooley technique was developed to design direct multipliers for Two's compliment numbers [9].When multiplying two's compliment numbers directly, each of the partial products to be added is a signed numbers. Thus each partial product has to be sign extended to the width of the final product in order to form a correct sum by the Carry Save Adder (CSA) tree.
Conclusion: According to the Baugh wooley approach, an efficient method of adding extra entries to the matrix is suggested to avoid negatively bits in the partial product matrix which results in extra circuitry and increase in power consumption.

D. Braun Multiplier

Braun multiplier is well known due to its regular structure. It is a simple parallel multiplier that is commonly known as carry save array multiplier. This multiplier is restricted to performing multiplication of two unsigned numbers. It consists of array of AND gates and adders arranged in iterative structure that does not require logic registers. This is also known as the non-additive multiplier since it does not add an additional operand to result of multiplication
Conclusion: One of the major disadvantages of the Braun's multiplier is that the number of components required increases quadratically with the number of bits which will make the multiplier to be inefficient. It cannot stop the switching activity even if the bit Coefficient is zero that ultimately results in unnecessary Power dissipation.

E. Booth Multiplier

The Booth recoding multiplier is one such multiplier; it scans the three bits at a time to reduce the number of partial products [19]. These three bits are: the two bit from the present pair; and a third bit from the high order bit of an adjacent lower order pair. After examining each triplet of bits, the triplets are converted by Booth logic into a set of five control signals used by the adder cells in the array to control the operations performed by the adder cells. The method of Booth recording reduces the numbers of adders and hence the delay required to produce the partial sums by examining three bits at a time. To speed up the multiplication Booth encoding performs several steps of multiplication at once. Booth's algorithm takes advantage of the fact that an adder subtracted is nearly as fast and small as a simple adder.
Conclusion: The drawbacks of booth multiplier are number of add subtract operations and the number of shift operation becomes variable and becomes inconvenient in designing parallel multipliers. The algorithm becomes inefficient when there are isolated 1's.which results in more power consumption due to large number of adders. summing the partially redundant partial products requires as much hardware as representing them in the fully redundant form . Along the evaluation path.

III. PROPOSED WORK

A. Modified Booth Multiplier

Booth encoding is a method of reducing the number of partial products required to produce the multiplication result. To achieve high-speed multiplication, algorithms using parallel counters like modified Booth algorithm has been proposed and used. This type of fast multiplier operates much faster than an array multiplier for longer operands because it's time to compute is proportional to the logarithm of the word length of operands. By recoding the numbers that are to be multiplied, Modified Booth multiplier allows for smaller, faster multiplication circuits. The number of partial products is reduced to half, by using the technique of Booth recoding [10],[14]. Reduction in the number of partial products depends upon how many bits are recoded and on the grouping of bits.

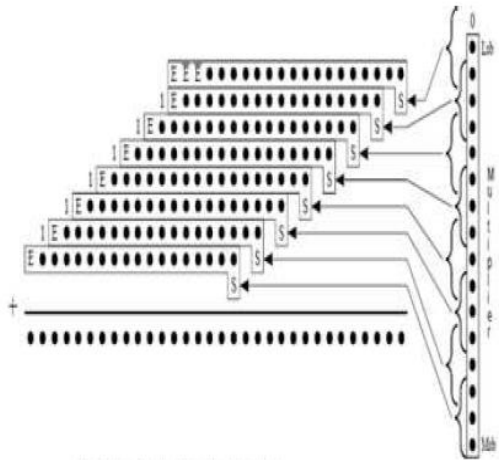

Figure 1:Modified Booth Encoder

The grouping considers each three bits of the multiplier bits starts from the LSB bit and the first considers only two bits. From the next it considers three bits in which one bit will be overlapped on the previous group.

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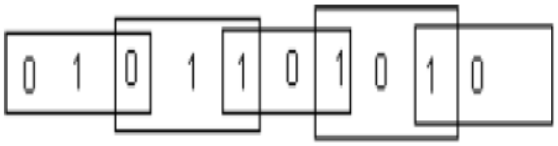

Figure 2:Grouping Of Bits From The Multiplier Term

Thus grouped multiplier will result in the production of bits between these five bits as followsas -2,-1, 0, +1, and +2.The advantage of this method is making the number of partial products into half of the multiplier term size by grouping.

Block	Re - coded digit	Operation
000	0	0
001	+1	+1
010	+1	+1
011	+2	+2
100	-2	-2
101	-1	-1
110	-1	-1
111	0	0

Table1:Recoding Table

Figure3:example of modified booth multiplier

IV. POWER CONSUMPTION IN CMOS CIRCUITS

Power is the most important parameter in digital circuits to fabricate chips and portable devices. CMOS technology is used in digital circuits due to its less power consumption. Power consumption in CMOS circuits can be divided into dynamic and static power consumption shown in eq (1).

$$P_s = \alpha F_{clk} Vdd^2 C_L + I_{sc} V_{DD} + I_{LEAKAGE} V_{DD} \quad \text{.....(1)}$$

Where α is the switching activity, fclk is the clock frequency, CL is the output capacitance, VDD is the supply voltage, ISC is the short circuit current, and Ileakage is the leakage current. In micrometer technology dynamic power is the dominant Parameter while in the submicron technology, leakage current is the most dominant parameter in total power. The concentration of this paper is on dynamic power reduction [9],[10],[13],[14].

V. BYPASSING TECHNIQUE

Dynamic power consumption can be reduced by bypassing method when the multiplier has more zeros in input data. To perform isolation, transmission gates can be used, as ideal switches with small power consumption, propagation delay similar to the inverter and small area [3]. To study the proposed design we have consider column bypassing multiplier in which columns of adders are bypassed. In this multiplier, the operations in a column can be disabled if the corresponding bit in the multiplicand is 0. The advantage of this multiplier is it eliminates the extra correcting circuit [1].

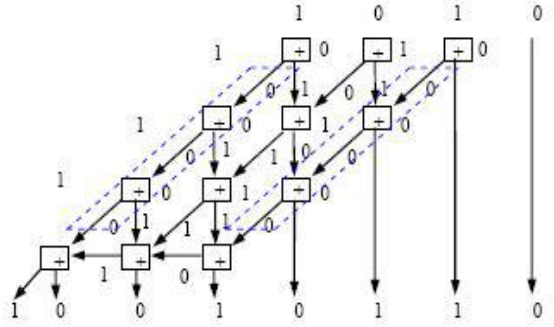

Figure 4. A column-bypassing example

A. Column Bypassing Technique

Instead of bypassing rows of full adders, we propose a Multiplier design in which columns of adders are bypassed. In this approach, the operations in a column can be disabled if the corresponding bit in the multiplicand is 0. There are two advantages of this approach. First, it eliminates the extra Correcting circuit as shown in Fig. 8. Fig. 9 shows the modified FA is simpler than that used in the row-bypassing multiplier.

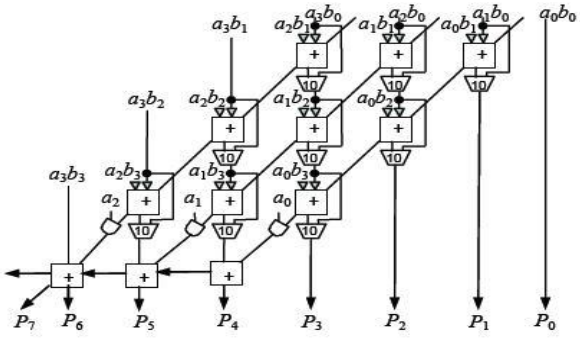

Figure.5. Column Bypassing Multiplier

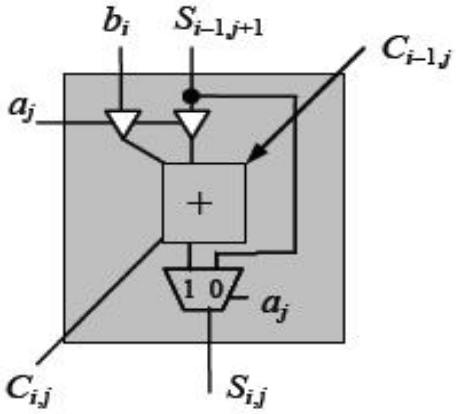

Figure. 6. Modified Full Adder Cell for Column Bypassing

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VI. CONCLUSION

Considering all facts of the multipliers above, combinations of multiplier can give good result for operands which have greater number of bits. Its dynamic power saving is a main advantage in Low power VLSI design world with great battery backup. This work can be further extended with the analysis of power and area when considered for ASIC implementation.

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