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Design and Implementation A Digital Sine-Cosine Generator Based FPGA

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Abstract— This article proposes a new way to generate a sine and cosine waves based FPGA. These signals can be used to generate a PWM signals that can be used in SDR and DSP. It can be used in control system like control DC and AC motors. The problem is how can generate a sine and cosine waves that are composed of the positive and negative part. Any hardware accepts the values 0, 1 and can't accept the negative values, we used the mode two's components of numbers to represent the positive and negative samples and converted these results to decimal numbers, and we shifted a one half wave 8 bit to obtain the wave without distortion. We used MATLAB to generate the data of sine and cosine wave. We saved the data in ROM memory using VHDL language and we applied the results onto board spartan-3A FPGA.

Index Terms— comparator, counter, sine and cosine generator, lookup table, PWM, rom memory, VHDL.

I. INTRODUCTION

We know, the sine and cosine waves are the fundamental building block of communications and signal processing system (modulation, demodulation, FFT spectral analysis). There are many methods to generate sine-cosine waves; lookup table and CORDIC algorithm are very common in SDP and SDR [1]. CORDIC process is fast but implements the algorithm in the hardware and requires a long program and energy.

Usage of microcontroller in SDR, SDP and control system is very wide, but sometimes, when designers need to control a large digital system, the number of input/output in one microcontroller limits the expansion of control system and they must to use several microcontrollers to complete the design which needs additional functions, these will be expensive. If the design has been completed, the stress of designers will stay in what functionality they can add to the control system and maybe they can't add any function. So the microcontroller is going to disappear with the appearance FPGA. With an FPGA, the designer can add all control system features to a single chip and even add new functions after he has completed this control system.

Usage of FPGA needs a large knowledge in hardware description language VHDL or VERILOG. Sometimes, there are cores that implement an algorithm as CORDIC core [2] [3], this core can generate a several algorithms like sin and cos, sinh and cosh, square root.

These cores need to build a project scheme, if the user doesn't know the hardware description language. The published articles on the subject of generating a sin-cosine waves using VHDL are few .on the other hand, a lot of articles used a microcontroller and C language to generate a sin and cosine waves.

We will discuss the data algorithm in our design and how can convert integer numbers and fraction portion to binary system. We will also convert the negative value to binary system using 2's complement system. The conversion data will be in MATLAB and save these data in rom memory that will be main element generates the sine and cosine waves. Our design has been implemented using MATLAB and ISE design suite14.4 XILINX. We applied the design onto board SPARTAN3AN and monitored the signals using ChipScope pro core.

II. DATA ALGORITHM OF SIN-COSINE GENERATOR

From the following simple relations:

$$x = \sin(\Phi) \quad (1)$$

$$y = \cos(\Phi) \quad (2)$$

We generate the data that will be used to form and build the sin and cosine signals.

The figure.1 illustrates the degrees circle, there are 360 degrees, and the step of the samples is 10 degrees. The next angle will be as:

$$\Phi_{n+1} = \Phi_n + 10^{o} \quad (3)$$

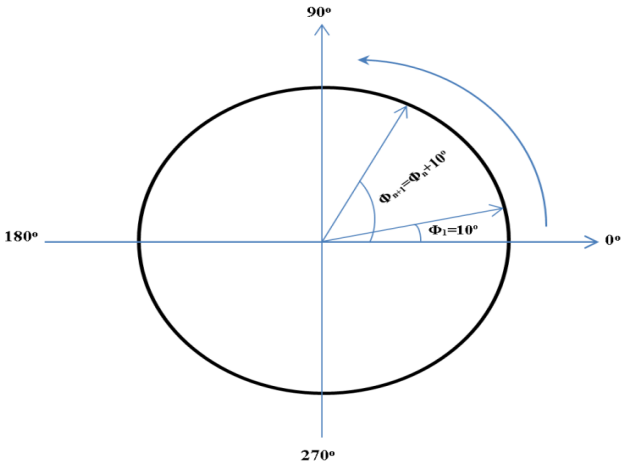

Figure.1: degrees circle

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The number of samples will be 36+1 from 0 to 360. We convert the samples from degrees to radians using MATLAB.

In order to explain the architecture of our design, we will now take the degrees in the below table and convert them to radians:

Table.1:values of sine and cosine main angles

angle	radians	Sin(Φ)	Cos(Φ)
0°	0	0	1.0000
45°	0.7854	0.7071	0.7071
90°	1.5708	1.0000	0.0000
180°	3.1416	0.0000	-1.0000
270°	4.7124	-1.0000	-0.0000
315°	5.4978	-0.7071	0.7071
360°	6.2832	-0.0000	1.0000

We know that any number is given in fixed point as:

$$N_r = (a_{n-1}a_{n-2}\cdots\cdots a_2a_1a_0 \cdot a_{-1}a_{-2}\cdots\cdots a_{-m})_r \quad (4)$$

Where the radix, r, is the total number of digits in the number. The radix point separates n integer digits on the left form m fraction digits on the right [4].

The value of the number in equation (4) is given in polynomial form by:

$$N_r = \sum_{i=-m}^{n-1} a_i r^i = (a_{n-1}r^{n-1} + \ldots + a_2r^2 + a_1r^1 + a_0r^0 \cdot a_{-1}r^{-1} + a_{-2}r^{-2} + \ldots\ldots + a_{-m}r^{-m} \quad (5)$$

In the binary system radix, r=2 and a=0 or 1 .therefore, the equation (5) can be written as:

$$N = \sum_{i=-m}^{n-1} b_i 2^i \quad (6)$$

From the previous table, we see some values are composed of integer portion and fraction portion. In addition, these values are signed. Therefore, we have to convert these values to signed binary numbers because the hardware only accepts the logic numbers 0 and 1.

We can reform the equation (4) to obtain the signed-magnitude number as the following:

$$N_{rSM} = (a_{n-1}a_{n-2}\cdots\cdots a_2a_1a_0 \cdot a_{-1}a_{-2}\cdots\cdots a_{-m})_{rSM} \quad (7)$$

Where a_{n-1} is the sign of the number. In decimal system the sign symbol is (+ or -) but in binary system, the sign symbol will be 0 if the number is positive and 1 if the number is negative.

In order to represent the numbers of our design, we used the radix complement NrC where it is obtained by the following relation:

$$N_{rC} = r^n - N_r = \overline{N}_r + 1_{LSD} \quad (8)$$

Application of this equation to the binary and decimal systems requires that for 2's complement representation $N_{2C} = \overline{N}_2 + 1_{LSD}$ and for 10's complement $N_{10C} = \overline{N}_{10} + 1_{LSD}$.

The radix complement for binary is the 2's complement (2C). In 2's complement the MSB is the sign bit, 1 including a negative number and 0 a positive one. The decimal range of representation for n integer bits in 2's complement is from $-(2^{n-1})$ to $+(2^{n-1}-1)$. From the equation (8), the 2's complement is formed by:

$$N_{2C} = 2^n - N_2 = \overline{N}_2 + 1_{LSD} \quad (9)$$

For any binary number N2 of n integer bits, the 2's complement of a binary number is obtained by replacing bit ai in N2 by (1-ai) and adding 1 to the LSB of the result.

We can convert the values of sine and cosine in the table.1 using MATLAB to 2's complement (2C) with fixed point and 6 bits fraction. The following table shows the values of sine and cosine in 2's complement:

Table.2: The values of sine and cosine in 2's complement

Sin(Φ)	sin(Φ) in 2's component	Cos(Φ)	cos(Φ) in 2's component
0	00000000	1.0000	01000000
0.7071	00101101	0.7071	00101101
1.0000	01000000	0.0000	00000000
0.0000	00000000	-1.0000	11000000
-1.0000	11000000	-0.0000	11111111
-0.7071	11010010	0.7071	00101101
-0.0000	11111111	1.0000	01000000

With the fixed point 8 bits with 6 bits fraction the range of decimal number is from -2 to 1.9844. This range is sufficient to convert the decimal numbers of sine-cosine Φ where the range of Φ is (0 to 360°) and the range of sine and cosine is (-1 to +1).

The hardware will see binary numbers without fraction portion. Therefore, the processor reads the binary numbers from the rom memory as in the following table:

Table.3: The values of sine and cosine Φ in real time

sin(Φ) in 2's component	Values read from rom	cos(Φ) in 2's component	Values read from rom
00000000	0	01000000	64
00101101	45	00101101	45
01000000	64	00000000	0
00000000	0	11000000	192
11000000	192	11111111	255
11010010	210	00101101	45
11111111	255	01000000	64

And if we monitor the data of real time to obtain the sine and cosine waves, we will see the signals as in figure.2.

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As this figure illustrates, this signal has not a negative portion and it is not homogeneous.
If we shift the positive portion of sin and cosine wave 255 decimal or 8 bits, we will obtain a homogeneous waves that will represent the sin and cosine wave.
The figure.3 shows the sin-cos waves before and after the shifting.

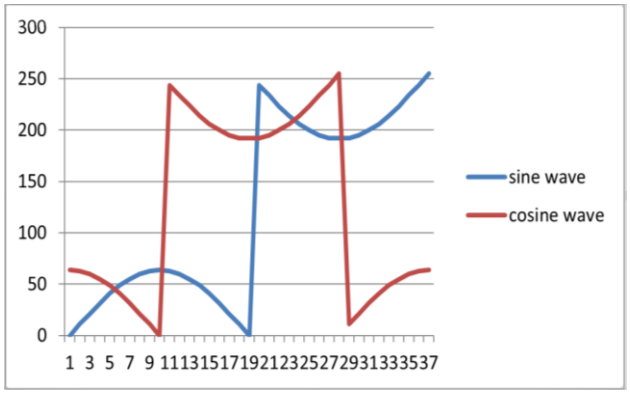

Figure.2: The sine and cosine waves in real time

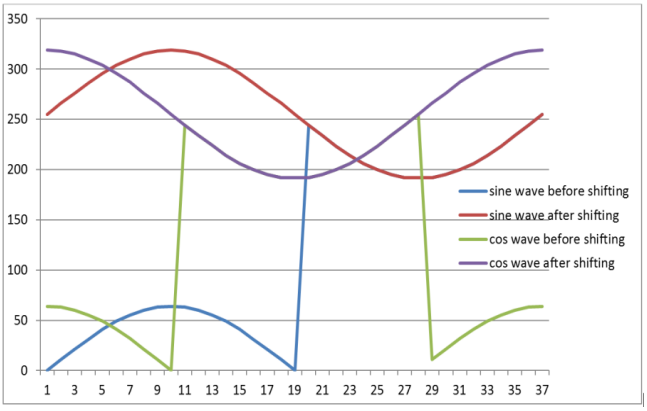

Figure.4: the sine-cosine waves before and after the shifting

After the shifting of positive portion, the maximum value of sine or cosine will equal 319 decimal. This number is composed of 9 bits" 100111111", therefore we have to 9 bits in the rom memory, in order to scan all the samples saved in the memory.

III. SCHEME OF DESIGN

Figure.5 illustrates the scheme design is used to monitor the sine and cosine waves
The scheme is composed of:

A. *Digital clock manager (DCM)*

Digital clock manager provides advanced clocking capabilities to FPGA application [5].

B. *Rom memory*

We designed this memory using VHDL language [6], it is two arrays: first array (37X9) saves the data samples of sin angles from 0 to 360° with step 10°. Second array (37X9) saves the data samples of cosine angles in the same way. The sampling frequency is 50 MHz from digital clock manager in order to eliminate the clock skew. This memory also contains a counter that increases from 0 to 38 , it begin to send the samples if it is greater than 1 and less than 37, therefore all data samples will be scanned during the rising edge of clock.
When the sampling time is "20 ns/sample", then the time need to generate the digital signal is:

$$\tau_{sw} = \tau_s * n_s \quad (9)$$

Where τ_{sw} is cycle of sine wave in ns, τ_s is the sampling time where $\tau s = 1/f_s = 1/50MHz = 20ns/sample$.
N_s is the number of samples equals 37 samples in our design. From the equation (9), we can calculate the frequency of sine and cosine wave:
$\tau_{sw} = 20*37 = 740$ ns, then we can calculate the wave frequency as:

$$f_{sw} = 1/\tau_{sw} = 1/740 \approx 1.35MHz \quad (10)$$

A. *Control data C*

This block is too designed using VHDL [7], we used two buttons to control the counter of output data. If counter is greater than 0, we can decrease the value of output data using button (0), and when the counter is less than or equal 16777215, we can increase the value of output data of this block using button (1) on the board SPARTAN3AN.

B. *Comparator*

This comparator is also written in VHDL. This block receives the samples of sin and cosine signals. In addition to, it receives the output of control data C. The output of comparator is two PWM. The output of first PWM drives a led on the board. PWM1 will be high, if the value of data in block control data is greater than the value of sin signal. The output of second PWM also drives a led on the mentioned board.PWM2 will be high, if the value of data in block control data is greater than the value of cosine signal.

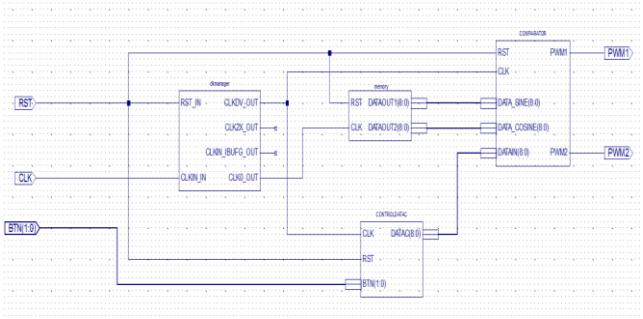

Figure.5: Scheme of test the data in real time

Before the download this design onto the board, we have to build the user constraint file (UCF). This file is an instruction given to the FPGA implementation tools to direct the mapping, placement of main clock, buttons, leds and all peripherals is used in the design [8].
The figure.6 illustrates the UCF of our design.

```
2  # PlanAhead Generated physical constrai
3
4  NET "CLK" LOC = E12;
5  NET "PWM1" LOC = R20;
6  NET "PWM2" LOC = T19;
7  NET "RST" LOC = T14;
8  NET "BTN[1]" LOC = U15;
9  NET "BTN[0]" LOC = T15;
10
```

Figur.6: User constraint file of the scheme design

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IV. SIGNALS AND DATA OUT

We used a ChipScope pro core to monitor the data of our design [9].

Figure.7 shows the wave form of all data that transfer in real time when we apply the software onto SPARTAN3AN. This figure contains the entire processing signal (signals of sampling data in rom memory, signals of control data c, signals of comparator and signals of PWM12).

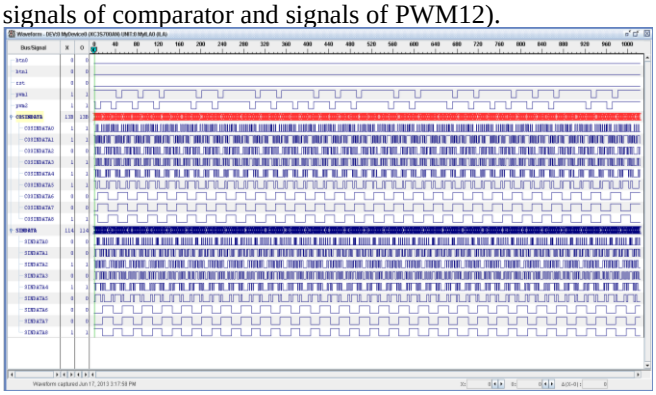


Figure.7: wave form of entire processing signals in the design

The signals will have some distortion, because the clock skews and time delay in electronic elements.

From the mentioned figure we can build the bus plot shows the sine and cosine signals in bus-plot mode as the following figure shows:

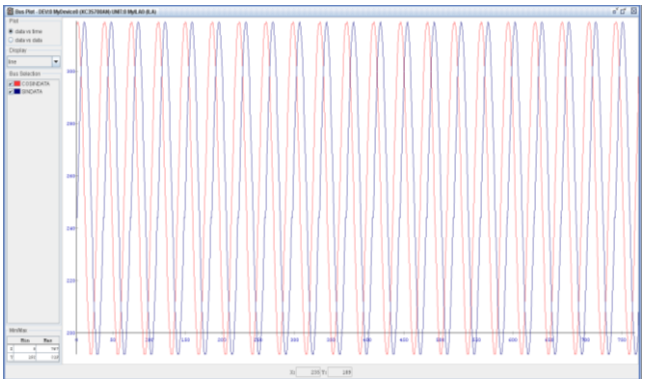
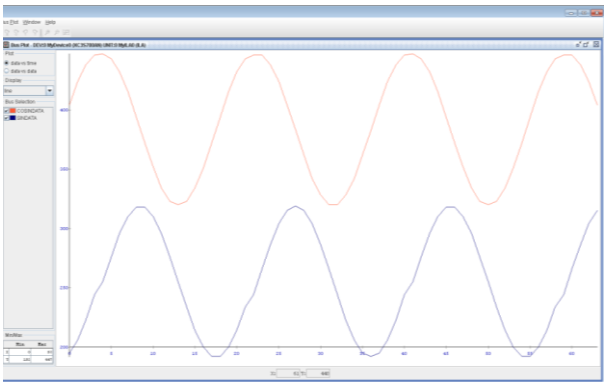


Figure.8: sine and cosine signals in bus-plot mode

And when we use to processors in the block memory the signals will be as:



Figue.9: sin-cos signals when used two processors in rom

V. CONCLUSION

This article proposed a new way to generate a sine and cosine signals that can be used in DSP, SDR, and control system as the control AC and DC motors, we used the hardware description language VHDL to build the blocks of design. The main bock is the rom memory contains the sampling data that has been generated in MATLAB.

We expected the form of sin-cos signals before the shifting using excel. We shifted the positive portion in both signals 8bits. This shifting was sufficient in order to obtain homogeneous signals that are identical with the signals in practical life.

This design can not only generate sin-cos signals but also can generate all the signals which we can meet in the life, 3 phases sin waves, saw wave, triangular wave, that can be used in modulation. This only needs to generate the data every signal in MATLAB and changes the dimensions of arrays in the block memory.

VI. ACKNOWLEDGMENT

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