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Fault Diagnosis of Analog Circuits Using dc Approach

Vaibhav Sharma, Ankit Verma

Abstract- ***Fault diagnosis of circuit is a key problem of theory of circuit networks and especially with the development of electronic technique at high speed, the increasing complexity of electronic equipment and altitudinal integration of electronic circuit, it is of importance in particular. Testing and diagnosis of electronic devices are fundamental topics in the development and maintenance of safe and reliable complex systems. In both cases, the attention is focused on the detection of faults affecting a subsystem whose appearance generally impairs the global system safety and performance. In a complete fault diagnosis procedure, fault detection and isolation must be carried out together; the effectiveness of the procedure depends on fault detection and isolation performance as well as the complexity of the test phase. While there are established techniques to obtain an automatic diagnosis for a digital circuit, the development of an effective automated diagnosis tool for analog or mixed circuits is still an open research field. For more than two decades, the subject of fault location in analog circuits has been of interest to researchers in circuits and systems. In recent years this interest has intensified and a number of promising results has emerged.***

I. INTRODUCTION

The analog circuit fault location problem can be an extremely difficult problem. This is because of the difficulty of measuring currents in situ (without breaking connection), the lack of good fault models for analog components similar to the stuck-at one and stuck-at-zero fault models, which are widely accepted by the digital test community , by the nonlinear nature of the problem. If, for example, a parameter value changes by a certain factor, the responses do not change by the same factor, i.e. the relationship between the circuit responses and the component characteristics in non-linear. Even though the circuit may be, linear. By a fault we mean, in general, any change in the value of an element with respect to its nominal value which can cause the failure of the whole circuit. Theory of fault diagnosis consists of fault diagnosis of analog circuit and digital circuit. Fault diagnosis of analog circuit started from the 1967s, and became an active field of inquiry in the 1970s. At present, the ways of fault diagnosis includes simulation before test (SBT) and simulation after test (SAT).

Simulation before test is also called fault dictionary approach or fault simulation. Fault dictionary is effective in digital circuit, because digital circuit has only two estates: 0 and 1, and fault character can be showed well and exactly with Boolean function.

Hard fault of analog circuit mainly comes down to two estates: short circuit and open circuit, which can be showed with 0 and 1. So conventional fault dictionary is comparatively applicable for hard fault.

Fault diagnosis of analog circuit was quite time-consuming in the past, because modeling this kind of consecutive system was very complex, and nonlinear effects and component tolerance made the model unreliable. However, these difficulties make the application of neural network to this area very appealing because no precise model or little knowledge of characteristic of the circuit is required. Therefore, neural network offers a very promising approach to future research in fault diagnosis.

In neural-network based fault diagnosis, network works as a fault dictionary. A fault dictionary is constituted by a series of feature vectors and its corresponding fault classes. Features extracted from circuit outputs naturally inherit faulty behavior, component tolerances and nonlinear effects and are presented together with the fault classes to the neural network as input-output pairs. In actual testing, the fault class of an analog circuit can be detected from the output of network when the feature is fed into its input layer.

In most of recent research, there are two main methods to define the neural network output layer. One is to aim at detecting which component is at fault, but we can't get the value information of the faulty component further more. It is uncertain whether it's greater or smaller than nominal value. The other is to take these two situations as different fault classes, which costs more neurons than the former method, and the output layer would become heavy and complicated, which results in longer time for training and testing. About the value of faulty component. Our work provides a new idea of network architecture design and valuable direction for engineers in analog circuit testing.

The preceding section demonstrates an organized technique for generating an analog fault dictionary, selecting input stimuli, and minimizing the number of test points. However, the entire approach is based upon adequate Pre selection of device failure modes. The dc method serves only to guarantee that these preselected failures can be detected and isolated by means of the input stimuli and test points determined by the method. A decision to employ this approach must therefore be based all most entirely on whether or not a sufficiently large number of potential fault modes can be included in the set of pre-selected failures. Analog failures are classified as the following.

1. Hard failures which occur 80-90 percent of the time. 50-60 percent of these involve open resistors, shorted (or high leakage) capacitors, and shorted diodes and transistors. The remaining failures in this category are open capacitors, diodes and transistors.

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***** Correspondence Author (s)
Vaibhav Sharma*, is pursuing M.Tech in Communication Engineering at Shobhit University, Meerut (U.P) and completed B.Tech (ECE) from CERT, Meerut affiliated to G.B.. Technical University, Lucknow (U.P).
Ankit Verma obtained his M.Tech Degree in Communication Engineering at Shobhit University, Meerut (U.P) and completed B.Tech (ECE) from MIT, Moradabad affiliated to U.P.

2. Soft and intermittent failures which occur lo-20 percent of the time. Soft failures include large value changes of resistors and low gain transistors. Intermittent failures are noisy transistors, capacitors that open or short intermittently, and temperature sensitive component parameter value changes.

1.1 Fault location techniques

According to (Bandler and salama, 1985) [1], fault location techniques in general can be categorized in to five groups in figure1.1.

1- Fault dictionary techniques
2- Approximation techniques
3- Fault verification techniques
4- Parameter identification techniques
5- Artificial intelligence techniques

The main techniques location and identification are:

1.1.1 Fault dictionary techniques

Fault dictionary are techniques completely based on quantitative calculations. Once the universe of fault to be detected is defined (fault1, fault2,……fault m), selected characteristics of the measured or simulated outputs are obtained from the systems for each considered fault and stored in a table. This set of output characteristics is known as fault signature. The groups of fault signatures considered constitutes the fault dictionary. The following diagram represents the fault location techniques and with the help of any one technique we can analyze fault detection and isolation.

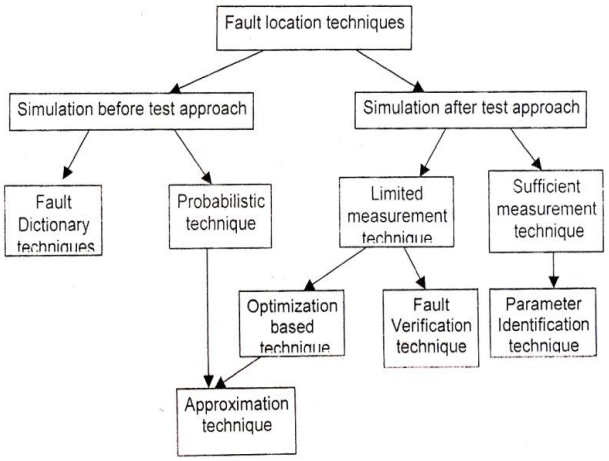

Figure 1.1 Fault location techniques

1.1.2 Approximation techniques

There are two main categories, approximation techniques that obtain a fault probability index related to each component and techniques that estimate system parameter including the faulty ones, from a reduced number of measurements. Both approaches have limited accuracy depending on the estimation that is used.

1.1.3 Fault verification techniques

This assumes that there are a limited number of measures in the sense that there are not enough to determine all the network parameters. They use network theory and mathematical theory to check the consistency of the equation set after simulation. The inconsistency implies a fault in one or more of the components related to the equation. Logical relations between inconsistency conclusions give the faulty components. The decomposition for large circuits can be classified in this group.

1.1.4 Parameter identification techniques

When the number of measures is sufficient the parameters of the system values can be calculated using parameter identification techniques. these values are obtained from the circuit measurements after simulation. The number of parameters that can be identified in a particular circuit is called the testability.

1.1.5 Artificial intelligence techniques

Due to increase in circuit complexity system malfunction, detection and isolation are becoming more difficult. Fig 1.2 represents this technique.

1-Traditional approach: these are the most common techniques used in the industry and are based on heuristics. The expert experience is collected in a rule base or as a decision tree. These approaches have been well tested and they are very simple and understandable. On the other hand faults that are not predicted in advance will not be detected.

2- Model based approaches make use of the model to predict fault in the real circuit. Its main disadvantage is its inability to deal with un-simulated faults and expert knowledge acquisition when causal models are needed. Since they are not able to learn from new situations, they have a fixed performance level. Fault dictionaries are included in this group.

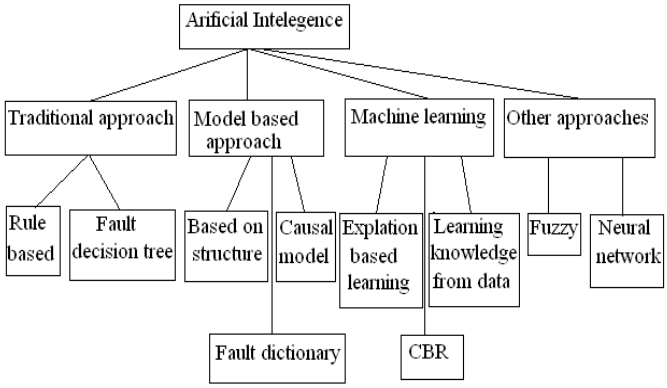

Figure 1.2 Artificial intelligence classifications

3-Machine learning approaches take advantages of previous successful or failed diagnosis and they use this knowledge in order to improve the systems performance. But in general big data bases with suitable data base is necessary if good result are desired. Case base reasoning (CBR) systems can be classified in this group.

4- Other approaches, fuzzy and neural network techniques can be cited in this group. The former provides a very intuitive way of representing knowledge, and they are normally combined with other techniques. Neural network techniques have the power to model unknown predicted faults when they are trained.

II. DC APPROACH TECHNIQUE

The usual method of automatically testing digital networks compares failed-board output levels with a set of prestored outputs on the Automatic Test Equipment. Similar techniques are developed for fault location of analog networks. These techniques are based upon pattern recognition methods.

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The first step in constructing the dictionary (look-up table) is fault definition, where the most likely faults are anticipated. This is a very critical aspect of the entire approach since only these faults could be identified. Large numbers of potential faults must be included. This, of course, will have an impact on the size of the dictionary and impose a limitation on the approach.

The circuit under test (CUT) is then simulated for these hypothesized faulty cases, in order to develop sets of stimuli and responses which will detect and isolate the faults. The signatures of the responses are stored in a dictionary for use in the on-line identification of faults. The optimum choice of stimuli, responses [2], and signatures is required to store the minimum amount of data that achieves the desired degree of detection and isolation.

At the time of testing, the faulty CUT is excited by the same stimuli that are used in constructing the dictionary. The signatures obtained are compared with those stored in the dictionary. A fault isolation criterion is implemented to identify the faulty CUT to one of prestored faults or to an ambiguity set that contains a set of possible faults. Selected characteristics of the measured or simulated outputs are obtained from the simulation for each considered fault and stored in a table. This set of output characteristics is known as fault signature.

The group of fault signatures considered constitutes the fault dictionary.

2.1 DC approach for dictionary construction

This method uses the dc voltages at the nodes of the circuit under dc stimulus to constructing dictionary. The approach is summarized in the following steps, which are given as,

Step-1 The test engineer provides the network description, fault definition, and the input stimuli.

Step-2 Different fault situations (single, hard, or soft faults) are inserted one at a time into the circuit simulator. The simulator computes dc nodal voltages and component overstresses resulting from the faults.

Step-3 From the ambiguity sets for every measurement node using the different input stimuli.

Step-4 Manipulate the ambiguity sets to find out the level (degree) of isolation and the unnecessary measurement nodes.

Step-5 Construct the fault dictionary using the reduced set of measurement nodes. Indicate the ambiguity groups and the secondary overstresses caused by faults.

The construction of the dictionary is initiated by choosing the input signals to the circuit, the domain of analysis, and the responses to be measured General-purpose computer-aided design simulator, to compute the dc voltages at the nodes of the circuit under arbitrary dc stimulus. The following diagram represents the preparation of fault dictionary with the use of this flow chart. And this flow chart is used for preparation of fault dictionary representation. For preparation of fault dictionary we have to take the node voltages for different kind of characteristics of the circuit i.e. fault or non faulty and after that we will prepare the fault dictionary. A block diagram of the overall dc approach is shown in Figure. 2.1 Which shows that the flow chart of dc approach for preparation of fault dictionary.

2.2 Flow chart for construction of fault dictionary

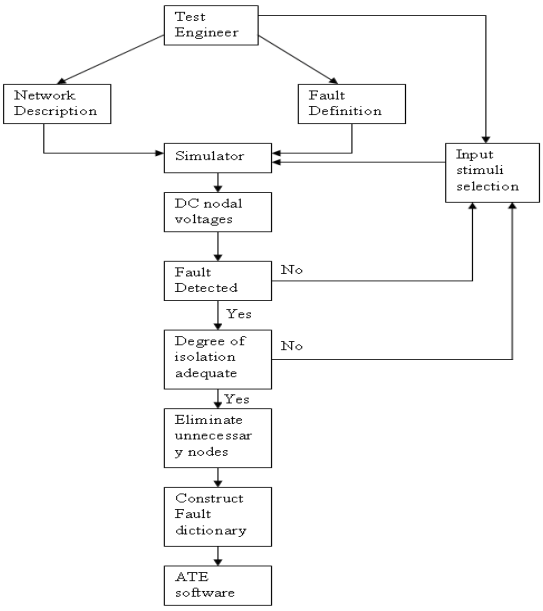

Figure 2.1 Chart for construction of fault dictionary

2.3 Theoretical diagnosis scheme

When the fault injected into the mathematical model is the same fault that affects the real circuit, and then the two circuits will present a very close behavior. Therefore, when the error output in figure 2.2 is minimal, the fault location is identified, since the algorithm is tracking the components into which faults are injected.

Faults are injected into the model one-by-one. As opposed to, the mathematical model is not modified to implement a new circuit topology due to a hard fault in a component. Only component deviations are injected into the mathematical model, changing every part of the model where the faulty component appears.

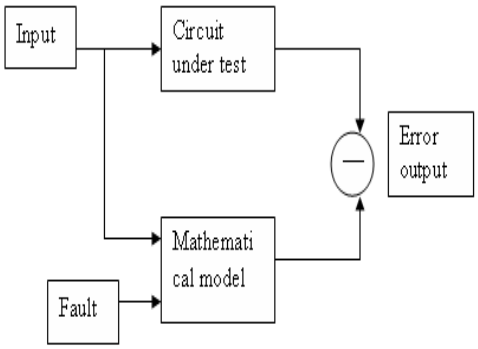

Figure 2.2 Theoretical diagnosis

2.4 Practical diagnosis scheme

In the experiments made according to the diagnosis method presented in the previous sessions, the circuit under test of figure 2.2 was in fact replaced by some practical data that had been previously obtained from the adaptive testing of the real circuit. It was noticed that there is an intrinsic difference between the real circuit and its mathematical model. This difference varies according to the fault, and it exists even for a fault-free circuit and the ideal model.

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One of the reasons for this disagreement is that the physical circuit uses non-ideal components (resistors with 5% tolerance tolerance, for example). Moreover, the A/D converter used to bring information from the analog to the digital world also introduces some phase distortion. Because of this, it is not possible to directly compare these two models, as originally intended. Therefore, a new step is necessary before the diagnosis phase takes place. It consists on learning the difference between the real and the ideal circuits by using an adaptive filter (figure 2.3(a)). This learning phase must also be performed when comparing the faulty circuit with the model into which a fault was injected, as it can be seen from figure 2.3(b). Notice that modeling error in figure 2.3(a) is just the difference between the models. However, diagnosis error in figure 2.3(b) embodies both the modeling error and the difference between the faulty circuit and the mathematical model into which the fault was injected.

Then, when the model has the same fault of the faulty circuit, diagnosis error must be very close to modeling error. The new error output is thus the difference between the modeling error and the error associated to the fault injected into the model. When this value is minimal, then the fault is located (figure 2.3(c)).

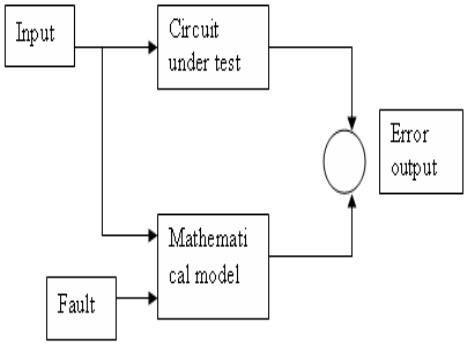

Figure 2.3(a) Practical diagnosis scheme

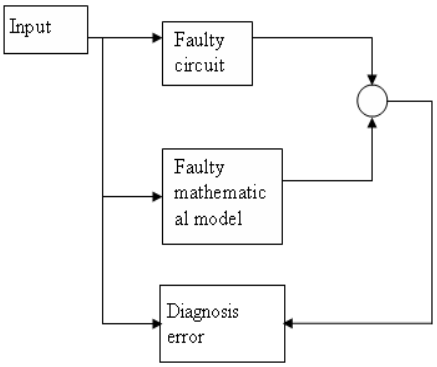

Figure 2.3(b) Practical diagnosis scheme

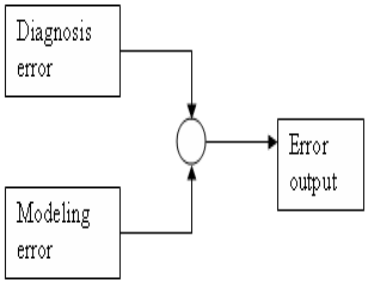

Figure 2.3(c) Practical diagnosis scheme

1 Training graph

The graph shown in figure represents that we apply all the data from fault dictionary to implementing the back propagation algorithm we achieved the performance of training. From the graph the black line show that network performance at fault free condition and blue pattern represents the training condition. It reached at black line after 60 repetitions to achieve the goal.

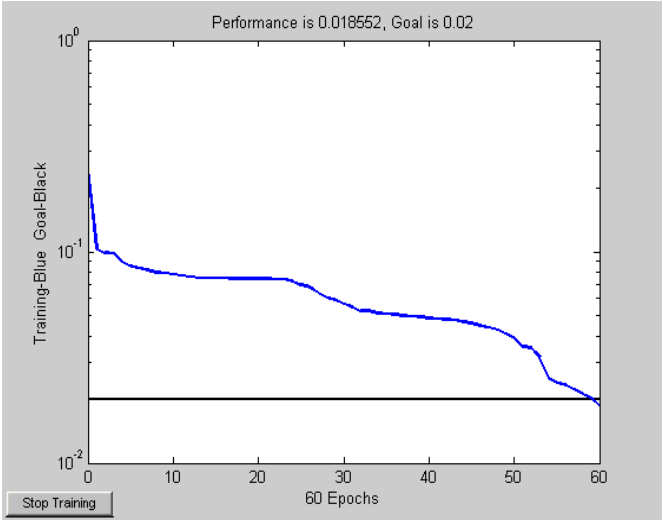

Figure 1 Training graph

8.2 Error Performance

The error pattern represents that the error between the network input to the target. This error is called as mean square error i.e. the graph shown in figure represents that the when we trained the simulated data with BP algorithm, after 60 repetition the squared error in between input and target is less than 0.05 to achieve the performance.

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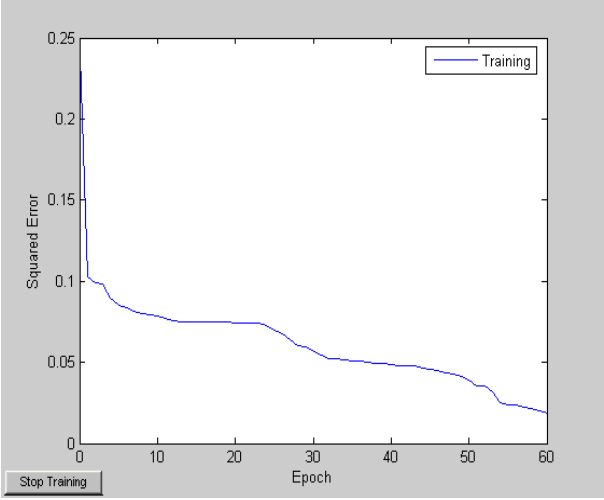

Figure 2 Error Performance

III. CONCLUSION

The example presented in the circuit for the passive circuit show the effectiveness of the proposed approach in locating various types of faults. The main features of this method are:

a) It is applicable to small & large circuits.
b) AC & DC extreme and drift faults may be located under the proper current excitation and corresponding voltage measurements.
c) The simulated result is trained with back propagation neural network.
d) The computation is minimal and the diagnosis is directly carried out from the neural network.
e) The elements are assumed to be non-faulty. However a faulty element can be located either before test, with some practical measurement.
f) The connection terminals must be included in the set of measurement nodes.

It is proposed a neural network learning mechanism into diagnosis of circuit. Results of simulation show: neural hard fault diagnosis of circuit is similar to dictionary approach, but dictionary approach with neural network make formation of dictionary and inquiry finish automatically, and is more quickly than conventional dictionary approach. Results indicated that the structure of BP network influents not only training process, but also assorting effecting. Overfull or fewer more neurons in hidden-layer would also reduce order of accuracy. On the condition of same training sample, two-hidden-layer is more quickly than single hidden-layer, but sometimes there would be agitation in network with two-hidden-layer. When being trained, network must have proper performance target, because higher target reduced accuracy, but lower target make training period longer and effect of network upon improving diagnostic. In a word, capability of information processing at high speed of Bp network which can approach random continuous mapping, has simple structure, and is easy to be accomplished makes the speed of diagnosis after test so higher that real-time diagnosis could be accomplished.

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Vaibhav Sharma is pursuing M.Tech in Communication Engineering at Shobhit University, Meerut (U.P) and completed B.Tech (ECE) from CERT, Meerut affiliated to G.B.. Technical University, Lucknow (U.P). His area of research includes Analog Ciruits.

Ankit Verma obtained his M.Tech Degree in Communication Engineering at Shobhit University, Meerut (U.P) and completed B.Tech (ECE) from MIT, Moradabad affiliated to U.P. Technical University, Lucknow (U.P).

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