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An Architecture for Low Power Binary Motion Estimation Architecture

V.Prathap Reddy, **MahendraVucha**

Abstract: **As technology increases, there is a need of fast computing systems to enhance multimedia applications. In this paper, architecture is designed for fixed block size and Variable Block Size (VBS) Motion Estimation Algorithm (MEA). The proposed architectures perform Motion Estimation (ME) by applying Diamond search (DS) algorithm on 1-Bit Transform (1-BT) image frames. The DS based 1-BT ME architecture reduces the minimum clock frequency required and overall power consumption compared with other ME architectures. So, the proposed architectures can be suitable for low power portable video application. The behavior of proposed architecture described in Verilog HDL and functional verification is done using Modelism simulation tool.**

Keyword- HDL, VBS, MEA

1.INTRODUCTION:

Motion Estimation (ME), which is the most essential part of any video coding technique, which exploits and tries to minimize the temporal redundancy present between successive frames. Block Matching Motion Estimation (BMME) is one of the most efficient and popular techniques to remove the temporal redundancy present between successive frames In literature, many one-bit transformation (1-BT) kernels are available that convert an image with 8 bits/pixel representation into a binary image with 1 bit/pixel representation. The first 1-BT kernel was proposed by Natarajan et al. [4]. A multiplication free one-bit transformation (MF-1BT) kernel has been proposed in [5]. Binary ME with an early termination scheme have been proposed in [6]. Two bit transformation (2-BT) has been proposed in [7] for an enhanced accuracy in ME. The constrained one bit transformation (C-1BT) has been proposed in [8] for a better performance than 1-BT, but at the same time with a reduced complexity than 2-BT.The implementation of 1-BT based ME on hardware has been proposed for the first time by Natarajan et al. [4]. A high performance VBS ME architecture for MF-1BT has been proposed in [9]. In [10], MF-1BT and C-1BT ME architectures for fixed block size (FBS) are presented. Both the architectures[4] and [10] are based on 16 processing elements (PEs). The application of fast search algorithms like diamond search(DS) on 1-BT frames can further reduce the computational load to a great extent as compared to applying full search (FS) on 1-BT frames. It has been shown in the present paper that the combination of 1-BT with DS results in a very small degradation in the peak signal to noise ratio (PSNR) as compared to FS.

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***** Correspondence Author (s)
V.Prathap Reddy, Department of Electronics & Communication Engineering, KL University,Vijayawada(A.P.), India
MahendraVucha, Department of Electronics & Communication Engineering, KL University, Vijayawada (A.P.), India

In the present paper, we have presented an in depth analysis of performing ME on 1-BT binary frames by applying DS. VBS motion estimation. In the proposed architectures, the pixels from the current block (CB) are read only once from the external memory and are stored into the local memories of the ME hardware. Thereafter, the pixels from the CB are supplied to the appropriate PEs periodically. The overlap between the neighboring search locations for DS is also exploited in a novel way to reduce the number of external memory accesses. The proposed architectures are faster than a recently reported 1-BTbased ME architecture. The implementation of 1-BT based ME on hardware has been proposed for the first time by Natarajan et al. [4]. A high performance VBS ME architecture for MF-1BT has been proposed in [9]. In [10], MF-1BT and C-1BT ME architectures for fixed block size (FBS) are presented. Both the architectures[4] and [10] are based on 16 processing elements (PEs).

The application of fast search algorithms like diamond search(DS) on 1-BT frames can further reduce the computational load to a great extent as compared to applying full search (FS) on 1-BT frames. It has been shown in the present paper that the combination of 1-BT with DS results in a very small degradation in the peak signal to noise ratio (PSNR) as compared to FS.

2.DIAMOND SEARCH ALGORITHM:

The original image frame shaving 8 bits/pixel representation is converted into binary image frames with 1 bit/pixel representation. This is done by filtering the original image frame by a multi band-pass filter. The filtered image is then compared with the original image to obtain the binary image. In the original work by Natarajan et al. [4], the kernel used for filtering was having 25 non-zero elements and required expensive floating point multiplications.

MF-1BT has been proposed in [5] in which the complex floating point multiplications were replaced by simple shifting operations.(square) for LDSP (SDSP).As DS algorithm is highly center biased, it is very fast as compared to FS algorithm. On the other hand, unlike other fast search techniques such as the new three step search, where the number of search steps are fixed, in DS the number of search steps are not fixed and thus its performance is very much close to that of FS in terms of the PSNR The work on development of ME architecture as reported in the present paper is based on a novel combination of 1-BT and DS. ME is usually performed on 1-BT frames by full search only], [10]. In the present work, several fast search techniques (e.g. three step search TSS), new three step search (NTSS), four step search (4-SS), and diamond search (DS)) have been applied on1-BT frames.

The performance of fast ME on 1-BT frames is evaluated based on PSNR and the average number of search points.It can be observed from Table I that the combination of DS and 1-BT displays PSNR performance similar to the application of FS on 1-BT in most sequences with less than 0.21 dB degradation except for the sequences with complex motion like Foreman and the Coastguard for which the performance degrades by 0.31 dB and 0.59 dB respectively.

3.DATA FLOW ANALYSI FOR DS ALGORITHM:

Due to the regularity in data-flow, FS motion estimation (FSME) is generally preferred from the implementation point of view. However, due to its high computational power requirements, many fast but sub-optimal search algorithms have been proposed. These fast search algorithms can reduce the computational power by up to 60%, but as a side effect introduce irregular data flow. In our experiment, it has been found that DS based 1-BT ME provides acceptable quality at much lower complexity than FS based 1-BT ME. Therefore, DS algorithm shown in Figure 1 is one of the most preferred fast search algorithm & its pixel coordinates are shown in Figure 2.

The implementation of DS in hardware imposes considerable challenge for a VLSI designer. The search points for DS algorithm are arranged in a diamond like shape. This makes memory access mechanism for DS to be completely different from the FSME.

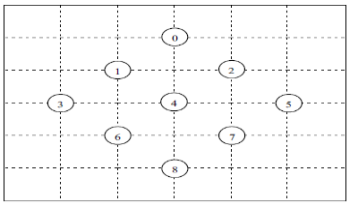

Fig.1. Search locations for DS algorithm. The center of search is denoted by '4'.

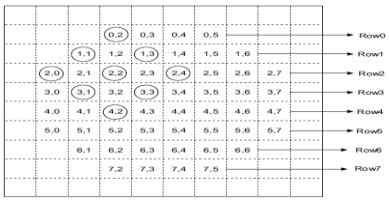

Fig.2. Data flow example for DS with pixel coordinate (2,2) as the center of search

The technique by which the data reuse is done for FS cannot be applied to DS in the same way .It is possible to reduce the overall power consumption of the ME hardware by reducing the number of external memory accesses. In the present section, a novel data-flow has been presented, which reduces the power consumption by maximizing the data reuse. In order to reduce the processing time for 1-BT based ME, it is desirable to process an entire row of data from the current block as well as the search block simultaneously ([4], [10]). In that case, one has to access an entire row of data from both of the blocks simultaneously.

It may be noted that the second row corresponding to the search location '0' in Fig. 1 has the pixel coordinates (1,2), (1,3),(1,4), and (1,5) in Fig. 2. Thus, the second row of data corresponding to the search location '1' can be only a new row of data has to be read in the Sub-sequent steps of ME. Therefore, by exploiting the overlaps of the search pixels for different search locations the number of memory accesses for search pixels can he reduced down to 8(5+1+1+1), whereas 36 (9×4) memory accesses (corresponding to the fact that there exist 9 search locations and the block size is of DS algorithm.

4.PROPOSED VLS IARCHITECTURE FOR 1-BT BASED FIXED BLOCK SIZE MOTION ESTIMATION

The block diagram of the proposed architecture for performing FBS ME on binary frames by applying DS has been shown in Fig. The architecture includes 8 RAMs for storing all the pixels from the search window (SW), a register array for storing the current pixels, a register array for storing the search pixels termed as the 'search register array', a data selector array, nine PEs, a comparator and a process control unit. In the proposed scheme, the evaluations of the matching criterion for all the search locations shown in Fig. 1 are done in parallel. As there are9 search locations for DS algorithm, a total of 9 PEs are used. Before the start of ME process for each MB, the search pixels from the entire SW are loaded into the internal memory of the ME hardware which consists of 8 RAMs. The CB pixels are also loaded into the register array for storing the current pixels. In the first step of ME, the center of search is chosen as the origin and the search pixels required for computing the matching criteria at the center are loaded into the search register array from 8 RAMs.

The comparator finds the minimum NNMP value as well as the corresponding location and sends it to the process control unit. The process control unit controls the entire process of ME by sending proper control signals to all the hardware modules.

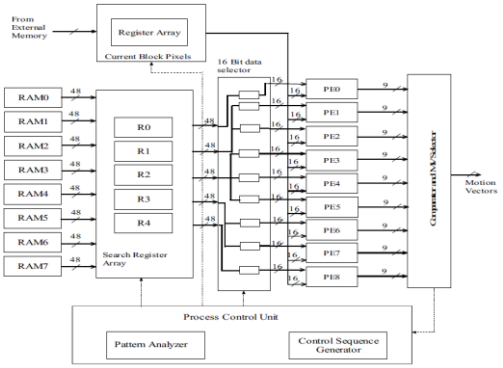

Fig.3.Overall VLSI architecture for the proposed FBS ME

A. Processing Element

The architecture of the PE is shown in Fig. 4. The PE possesses two input ports namely, C and S for reading two 16-bitvectors from the CB and the SW respectively. There are two 8-bit XOR arrays in the PE. The number of ones as a result of the XOR operation is obtained by using two look-up tables (LUTs) with 28 entries. The outputs of the LUTs are then applied to a 4-bit adder. The output of the adder is then applied at the input of the accumulator.

The output of the accumulator provides the value of the NNMP for a particular location after 16 clock cycles for a MB of size 16×16.

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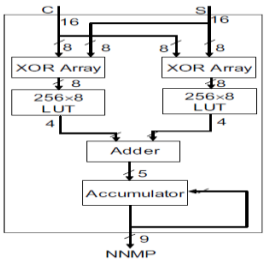

Fig.4. PE architecture for 1-BT FBS ME

B. Memory Interleaving

In order to provide the required search pixels to all the PEs simultaneously, memory interleaving technique similar to [19]is exploited.

The search pixels from the SW are interleaved among 8 RAMs (indexed from 0 to 7). For a single MB of size16×16 pixels and for a search range of [-16,16] pixels, the size of the SW will be 48×48 pixels. Here, since each pixel is represented by one bit, the actual size of the SW would be48×48 bits. The distribution of the search pixels among these8 RAMs is depicted in Fig. 5. All the pixels from the first location of SW are stored into the first location. of the RAM0. Similarly, all the pixels from the second location of the SW are stored into the first location of the RAM1.

This process is repeated for all the first eight locations of the SW (i.e. for the locations 0 to 7). After the eighth location, the search pixels from the next location (i.e. address 8) are stored into the second location of the RAM0 (i.e. address 1). This process is repeated for the entire SW. In Fig. 5 (b). Using the above memory organization, it becomes very easy for one to locate the particular RAM and the location in that RAM where the search pixels from the SW with a given location are stored.

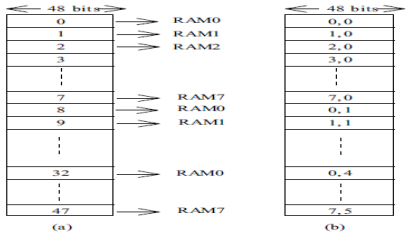

Fig. 5.Memory interleaving for parallel access of the search pixels.

(a) Search block for MB of size 16×16 and search range of [-16,16].

(b) Modified memory arrangement with the first index indicating the RAM number and the second indicating the location of 48-bit word stored in the RAM.

C. Register Array for the Current Block Pixels

The pixels from the CB are read only once from the external memory and are stored into an array of sixteen 16-bitregisters. The current pixels are then provided to the proper PE by the register array, and no further external memory access is required.

In this way, the proposed architecture significantly reduces the number of external memory accesses for the current pixels.

D. Search Register Array

It reduces the number of external memory accesses to a great extent. At the start of each search, the data are loaded into the register array from the RAMs independently and at the same time. From the next step onwards, no external memory read operations are required for the registers R0-R3 as shown in Fig. 6.

Register R0 is now connected to register R1 via one Multiplexer and register R1 is connected to register R2 via another multiplexer. This is the case for all the registers except for the last register R4, which is always connected with one of the RAMs. The register R0 always provides the search pixels required for the computation of the NNMP at location '0' (vide Fig. 2).

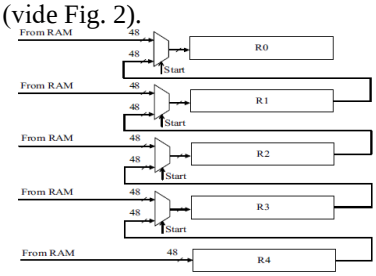

Fig. 6.Register array for search pixels

Computation of NNMP at location '0' is done by PE0.Therefore, register R0 is connected to PE0 via one 16-bit data selector. In a similar way, R1 supplies the search pixels required for the computation of NNMP at the locations '1' and'2'. Therefore, register R1 is connected to the processing elements PE1 and PE2 via two 16-bit data selectors. RegisterR2 is connected to PE3, PE4 and PE5 via three 16-bit data selectors. In a similar way, register R3 is connected to PE6and PE7, while register R4 is connected to PE8 via data selectors.

E. Comparator Unit

The outputs of all the PEs are connected to a comparator. The comparator selects the best MV from the computed values of the matching criteria. It generates the coordinates of the best matching point.

It also generates a number ranging from 0 to 8 indicating the location where the best match is found. For example, with reference to Fig. 1, if the best match were found at the center of the search, then it will generate the number 4.

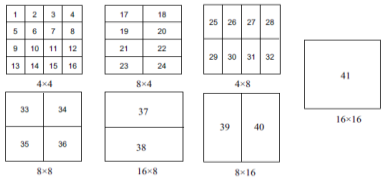

Fig. 7.Partition of a MB into 41 blocks

F. Process Control Unit

This is the most critical part of the architecture. There are two parts in this unit. One is the pattern analyzer and the other is the control sequence generator. The pattern analyzer unit takes the decision regarding whether to perform LDSP or SDSP in the next step of the search depending upon the location of the best match as obtained from the comparator unit. It also generates the center of the new search and the new points where the matching criteria are to be evaluated.

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5. Results & Discussions:

This section discusses about the functional verification of the system.

Pattern Analyzer: The functionality of Pattern analyzer is described in table 1 & table 2.

Table 1: input to pattern Analyzer

Port Name	Size of port(in bits)	Value
Clock	1	1
Reset	1	0
en	1	1
Ext_RAM	48	000000000000H
R00	48	00000000003FH
R01	48	000000000032H
R02	48	000000000028H
R03	48	000000000015H
R04	48	000000000010H
R05	48	000000000029H
R06	48	00000000002dH
R07	48	00000000003FH

Table 2: output to pattern Analyzer

Port Name	Size of Port(in bits)	Value
Reg_in_0	48	000000000025H
Reg_in_1	48	000000000013H
Reg_in_2	48	00000000002bH
Reg_in_3	48	000000000011H
Reg_in_4	48	000000000000H

RAM: The functionality of RAM is described in table 3 & table 4.

Table 3: input to RAM

Port Name	Size of Port(in bits)	Value
cs	1	1
we	1	1
Clock	1	0
Reset	1	0
Detain	48	000000000000H

Table 4:output to RAM

Port Name	Size of Port(in bits)	Value
R00	48	00000000003FH
R01	48	000000000032H
R02	48	000000000028H
R03	48	000000000015H
R04	48	000000000010H
R05	48	000000000029H
R06	48	00000000002dH
R07	48	00000000003FH

Register Array: The functionality of Register Array is described in table 5, table 6, table7 & table 8.

Table 5: input to External Memory

Port Name	Size of Port (in Bits)	Value
Clock	1	1
Reset	1	0
Data_in	16	00FFH 00F2H 00a8H 0095H 0090H 00a9H 00edH 00FFH

Table 6: output to External Memory

Port Name	Size of Port(in bits)	Value
Data_out	16	00FFH 00F2H 00a8H 0095H 0090H O0a9H 00edH 00FFH

Table 7: input to Current Block

Port Name	Size of Port(in bits)	Value
cs	1	1
we	1	1
clock	1	0
Reset	1	0
Data_in	16	00FFH 00F2H 00a8H 0095H 0090H O0a9H 00edH 00FFH

Table 8: output to Current Block

Port Name	Size of Port(in bits)	Value
Data_out	16	0000H 00FFH 00F2H 00a8H 0095H 0090H O0a9H 00edH

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Search Register Array : The functionality of Register Array is described in table9& table 10.

Table 9: Input to Search Register Array

Port Name	Size of Port(in bits)	Value
Clock	1	1
Reset	1	0
Start	1	0
Ram_in	48	000000000000H
Search_loc_0	48	000000000025H
Search_loc_1	48	000000000013H
Search_loc_2	48	000000000011H
Search_loc_3	48	000000000000H

Table 10:output to Search Register Array

Port Name	Size of Port(in bits)	Value
R0out	48	000000000025H
R1out	48	000000000013H
R2out	48	000000000011H
R3out	48	000000000025H
R4out	48	000000000015H
R5out	48	000000000000H

6.CONCLUSION:

In the present paper, low power ME architectures have been developed for implementing DS on 1-BT frames with FBS and VBS support. The clock frequency of the proposed ME architectures therefore can be effectively reduced for low power designs. In particular, the required clock frequency for the proposed VBS ME architecture for processing SDTV frames (1280×720 @ 30 fps) is 16.63 MHz. On the other hand, the frame size and the frame rate supported by the proposed architectures can also be extended subject to a clock frequency constraint. For the proposed VBS ME architecture, the required clock frequency for processing SHDTV (1920×1080 @ 60 fps) is74.84 MHz.

The maximum operating frequencies of the proposed architectures for FPGA implementation are found to be 135 MHz and 129 MHz for FBS and VBS respectively.

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V.Prathap Reddy was born on 7th december 1989 at Ongole, India. He received his, B.Tech in Electronics & Communication Engineering from TRR College of Engineering, affiliated to JNTU, Hyderabed, Inole , AP, India and Pursuing M.Tech in VLSI at K L University, Vijayawada, AP, India.His research interests in, Digital VLSI Design and Low Power VLSI Design and Digital Signal Processing.
vennaprathap@gmail.com

MahendraVucha received his B. Tech in Electronics & Communication Engineering from JNTU, Hyderabad in 2007 and M. Tech degree in VLSI and Embedded System Design from MANIT, Bhopal in 2009. He is currently working for his Ph. D degree at MANIT and also working as Asst. Prof in K L University, Dept. of Electronics and Communication Engineering, Vijayawada, AP, India. His areas of interest are Hardware Software Co-Design, Analog Circuit design, Digital System Design and Embedded System Design.
mahendra.v@kluniversity
mahendra158@gmail.com

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