Low Power CMOS Counter Using Clock Gated Flip-Flop

Upwinder Kaur, Rajesh Mehra

Abstract—The synchronous designs operates at highest frequency that derives a large load because it has to reach many sequential elements throughout the chip. Thus clock signals have been a great source of power dissipation because of high frequency and load. Clock signals do not perform any computation and mainly used for synchronization. Hence these signals are not carrying any information .So, by using clock gating one can save power by reducing unnecessary clock activities inside the gated module. A new counter using clock gated flip-flop is presented in this paper. The circuit is based on a new clock gating flip flop approach to reduce the signal's switching power consumption. It has reduced the number of transistors. The proposed flip-flop is used to design 10 bits binary counter. This counter has been designed up to the layout level with 1V power supply in 90nm CMOS technology and have been simulated using Microwind simulations. Simulations have shown the effectiveness of the new approach on power consumption and transistor count

Index Terms—Clock gating, master- slave configuration, power consumption, and switching activity.

I. INTRODUCTION

The digital circuit used for counting pulses is known as counter. Counter is the widest application of flip-flops. A counter is one of the more useful digital circuits. Counters are used in many applications. Examples include frequency dividers, and frequency counters. A digital counter has the following characteristics:

i. A maximum number of counts before it rolls over (returns to zero.) This is referred to as the counter's modulus.

ii. It can count in either direction (ascending, from low to high, or descending, from high to low.)

iii.it is either synchronous or asynchronous. That is, it counts with the system clock, or it counts independently of the system clock.

iv. It can function either as a monostable or an astable circuit. The first means that it runs once and stops. The later means that it will run forever, or until interrupted.

In many applications, the continuous increase of clock Frequency has led to more power consumption despite the use of lower supply voltages. Power consumption has a static component coming from the leakage of inactive devices and a dynamic component coming from the switching of active devices. It has been proved that clock signal consumes a high dynamic power as the clock net has one of the highest switching densities.

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Today's consumer demands more functionality, energy efficient device and optimized power devices as time goes, so in order to optimize power of a device the simplest control technique is to shut off the clock of the sequential block of the device where there is no function required from that section for some duration.

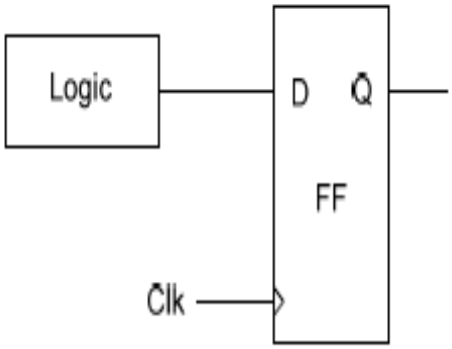

Figure 1. Block Diagram of Flip-Flop

Fig. 1 shows a conventional flip-flop connected to a logic block through its input terminal. The clock signal keeps changing its state in certain time points according to its frequency even if the logic output doesn't change "hold mode". A promising technique to reduce the power consumption of the clock signal is called clock gating, it depends on deactivating the clock signal on portions of the circuit that are inactive for certain periods of time. Different clock gating techniques have been used to minimize the clock power consumption as it is the main source of chip power dissipation. Deactivating the clock signal leads to reduced power dissipations of both its internal nodes and clock lines, but the overhead involved limits its use in low data switching situations. [1]The main purpose of this paper is to reduce the clock gated flip-flop overhead and make it applicable to data signals with higher switching activity. In synchronous digital circuits the clock net is responsible for significant part of power dissipation up to 40%. This paper is organised as follows. Previous work on clock gated flip-flops is reviewed in section II. Section III describes the proposed work. Section IV provides the simulation results in 90 nm CMOS technology to verify the performance of proposed circuit. Finally, conclusion is provided in section V

II. PREVIOUS COUNTERS

An analysis of previous clock gating flip-flops was carried out , Pointing out the advantages and drawbacks exhibited for each scheme, in terms of speed and power dissipation. In [3] clock gated edge triggered flip-flops are used but in that circuit delay is large .to overcome the delay enlargement the idea of clock gating a pulse triggered flip-flop was used.

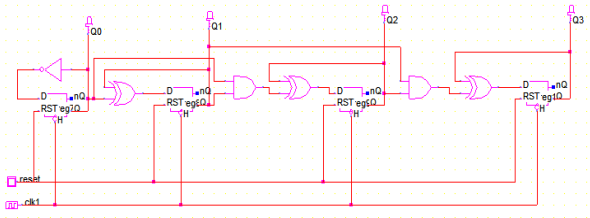

Figure 2. Schematic of counter without clock gating

The binary synchronous counter described in [9] is one of the essential building blocks in very large scale integration design. Its operation is usually based on a synchronous timing principle in which the data signal is evaluated at each clock cycle and assigned to its associated flip-flop. This counter has a lot of redundant transitions because the switching activity of the counter bits is decreased by half as the significance of each bit increases.

Switching activity of K^{th} bit= 2^{-k} (1)

As a consequence, many techniques have been proposed to reduce the clock system's power dissipation. Clock-gating is a technique that reduces dynamic power dissipation by selectively stopping the clock signal to portions of the circuit that are inactive at certain periods of time, and it can be applied to different hierarchical levels. By disabling the clock signal that drives a big functional unit reduces the power dissipation of both its internal nodes and clock lines [2]. On the other hand, it has been shown in [3, 4] that an important reduction of power dissipation is achieved by applying clock gating to individual flip-flops if it's input signal is sufficiently low.

III. PROPOSED CLOCK GATED COUNTER

The new design is based on comparing the flip-flop input and output using a XOR gate which generates a comparison signal Table I illustrates the relation among the clock signal (clk), the comparison signal (cmp), and the generated gated clock signal (clkg) for a positive flip-flop. If clk is 0, and cmp is 0, then the gated clock (clkg) holds its state. When clk is 0 and cmp is 1, then clkg is pulled down. When clk is one, then clkg is pulled high.

TABLE I. GATED CLOCK STATES

Clk	Cmp	Clkg
0	0	Hold
0	1	0
1	x	1

The D-latch in this proposed circuit is very compact. A very compact design of D-Latch is obtained by using original two inverter memory loop and by adding the minimum hardware to its state. Usually, latches proposed in cell libraries propose designs based on transmission gates rather than on the single pass transistors. The single pass transistor approach leads to more compact designs. However, the volage amplitude is degraded, so the noise margin is reduced, and the switching speed is slower. Consequently. Low power designs would prefer the pass transistor approach.

In order to overcome the limitation of latches when trying to build registers, edge triggered latches are used, wherein the information flows from the input D to the output Q only at a rising or falling edge of the clock. The latch is commonly known as D- Flip Flop or D-register.

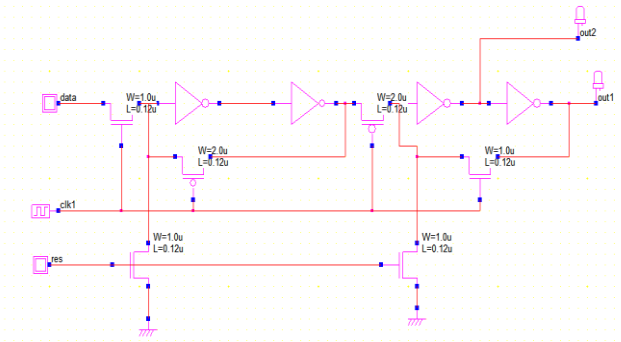

Figure 4. Schematic of D- Flip Flop

The reset function is obtained by a direct ground connection of the master and slave memories, using nMOS devices. This added circuit is equivalent to an asynchronous Reset, which means Q will be reset to 0 when Reset is set to 1, without waiting for an active edge of clock.

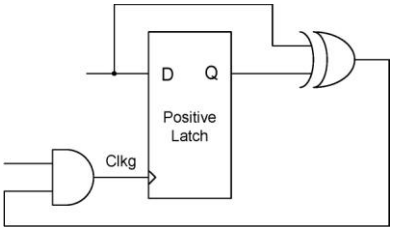

Figure 3. Clock gated latch

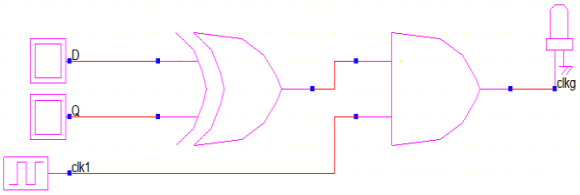

Figure 5. Schematic of clock gating circuit

This D-latch and clock gating module is used to design the proposed circuit of clock gated counter.

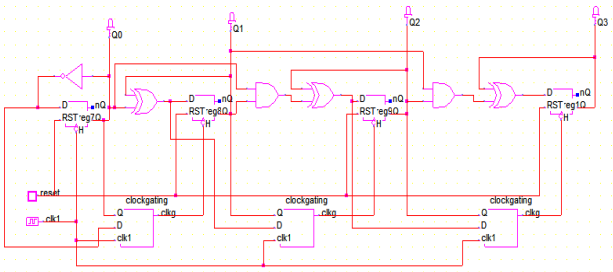

Figure 6. Schematic diagram of clock gated counter

IV. SIMULATION RESULTS AND DISCUSSIONS

Proposed circuits Implementation of figure 6 have been designed up to the layout level for a 90nm technology with 5v supply voltage. Proposed flip-flops are compared with a conventional non gated flip-flop.

Simulation results have been obtained through microwind simulations of the circuits extracted from the layout.

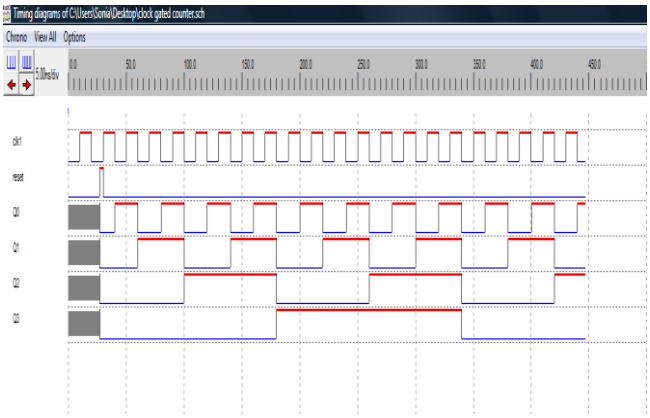

Figure 7. Timing diagram of clock gated counter

Timing diagram of clock gated counter is obtained by using Dsch 3.1 .Verilog file is generated in Dsch 3.1 using make a verilog file option. In Microwind , verilog text is converted into layout shown in figure 8. The dreg primitive used in counter is converted into a complex structure including the master and slave memories, each with two inverters and two pass transistors, as well as one pass transistor for the Reset function.

For testing the counter, the reset signal is activated twice, at the beginning and later, using a piece-wise-linear property.

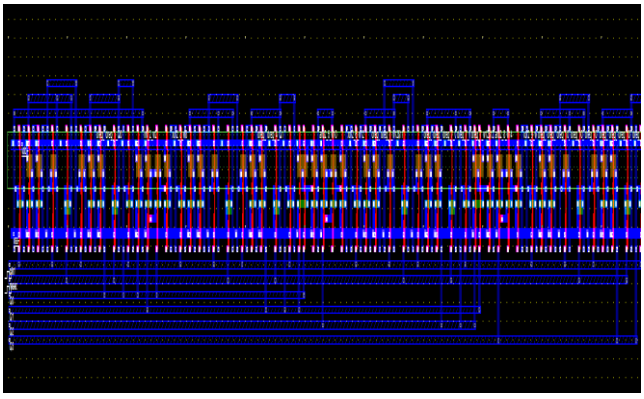

Figure 8. Layout of clock gated counter

Figure 9. Analog simulation of clock gated counter

Simulation is done using PWL(piece wise linear signal) for reset.

V. CONCLUSIONS

A clock gating scheme is embedded into the flip-flop has been proposed to eliminate redundant switching due to the clock and it minimized the power consumption.The experimental result using a 90nm CMOS process indicates the 15 percent power consumption. The power consumption of clock gated circuit is 0.143mW. This technique can further be used in complex parallel counters to reduce power consumption.

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