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A Novel Three-Phase Multilevel Inverter Using Less Number of Switches

Neelesh Kumar, Sanjeev Gupta, S.P.Phulambrikar

Abstract-*A novel three phase multilevel inverter with a small number of switching devices is proposed. Large electrical drives and utility application require advanced power electronics converter to meet the high power demands. As a result, multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power rating but also improves the performance of the whole system in terms of harmonics. In this paper the proposed inverter can output more numbers of voltage levels with reduced number of switches as compared to cascade H-bridge inverter, which results in reduction of installation cost and have simplicity of control system. Finally, the simulation and experimental results validate the concept of this new topology.*

***Keywords-PWM, SPWM, Cascade H-bridge(CHB), matlab simulation, multilevel inverter*.**

I. INTRODUCTION

Numerous industrial applications have begun to require high power apparatus in recent years. Power electronic inverter become popular for various industrial drives applications. Recently, multilevel power conversion technology has been developing the area of power electronics very rapidly with good potential for further developments. As a result the most attractive applications of this technology are in the medium to high voltage ranges. A multilevel converter not only achieves high power rating, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system for a high power application. proposed topology has less switches than that of [1] in symmetric topology.

II.CASCADE H-BRIDGE MULTILEVEL INVERTER

A cascade multilevel inverter made up of from series connected H-bridge inverter, each with their own isolated dc bus.

Each level can generate three different voltage outputs +Vdc, 0, -Vdc by connecting the dc sources to the ac output side by different combinations of the four switches. The output voltage of m level inverter is the sum of all the individual inverter outputs. Cascade multi-level inverter consists of a number of H-bridge inverter units with separate dc source for each unit and it is connected in cascade or series as shown in fig. 1

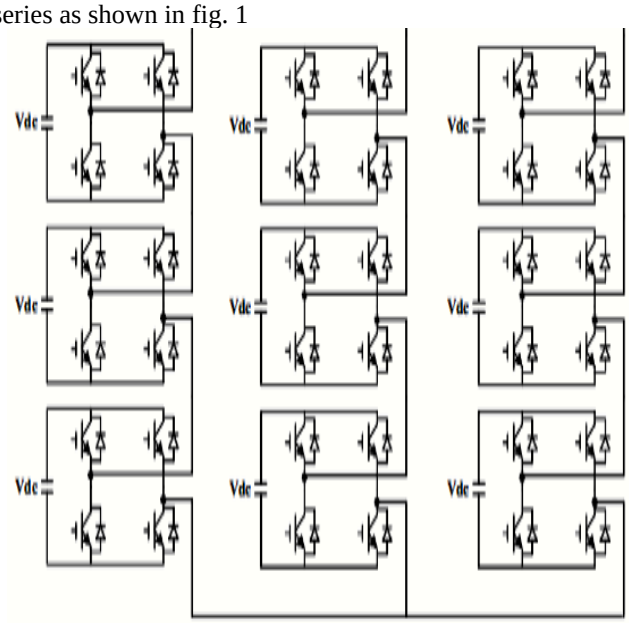

Figure 1 Three phase structure of Cascaded Multilevel Inverter

If all the dc source in Fig. 1 equal to Vdc, the inverter is known as symmetrical multilevel inverter and the number of output phase voltage levels N_{step} in a cascade inverter is defined by :

$$N_{step}=2n+1 \quad (1)$$

Where n is the number of separate dc sources or the number of full bridges and the maximum output voltage(V_{max}) of this n cascade multi level inverter is:

$$V_{max}=nV_{dc} \quad (2)$$

III.PROPOSED MULTILEVEL INVERTER

The general circuit diagram of phase A of the three phase proposed multilevel inverter is shown in fig.2. The proposed multilevel inverter requires only nine switches for single phase seven level inverter and total twenty seven switches for three phase seven level.. For the proposed topology, we just need to add only one switch for every increase in levels for single phase.

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Fig.3 showing the proposed three phase multilevel inverter, one phase of proposed inverter is shown in fig.4. fig.3 and fig.4 both are matlab simulated model of proposed multilevel inverter. In case of fig.4 it generate 7-level shaped output voltage wave. The switch S_8,S_9 connect in anti parallel across the load. In place of switch S_8,S_9 a bidirectional may be used. For increasing output voltage levels one power supply shall be added with one switch only. The table I showing the switching of device for different output voltage level.

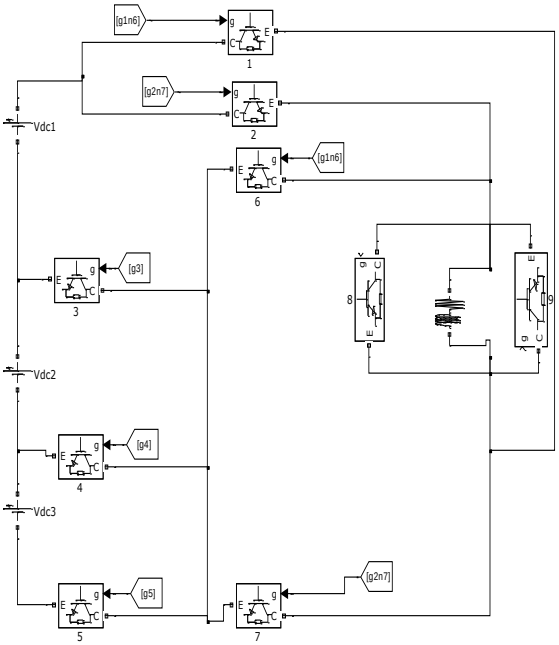


Figure 2 single phase basic structure of proposed multilevel inverter

Table I Switching conditions

	Conducting switches	Amplitude of the output voltage
1	S_2,S_7,S_3	$+V_{dc}$
2	S_2,S_7,S_4	$+2V_{dc}$
3	S_2,S_7,S_5	$+3V_{dc}$
4	S_8,S_9	0
5	S_1,S_6,S_3	$-V_{dc}$
6	S_1,S_6,S_4	$-1V_{dc}$
7	S_1,S_6,S_5	$-2V_{dc}$

Table II Comparison between cascade and proposed multilevel

Parameters	Cascade					Proposed				
Levels	3	5	7	9	11	3	5	7	9	11
Switches required	4	8	12	16	20	4	6	9	10	11

IV. THE MODULATION SCHEME

There are several modulation strategies possible for multilevel inverters. The firing method used in this paper is different from conventional pwm method. Firing pulses generated by comparing the sine wave with constant and then ANDed with pulse generator for pwm. This results smallest harmonics in output voltage and can be easily expanded to any level. This scheme is very simple and less complicated. The Fig. 4 showing the modulation scheme for switches 1to 7. The output pulse of fig 4 is shown in fig 5 for all the switches for single phase.

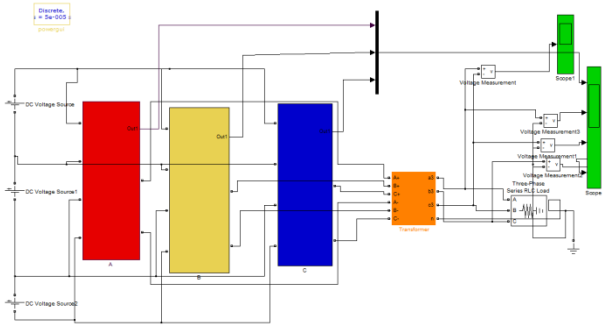


Figure 2 Three phase structure of proposed Multilevel Inverter

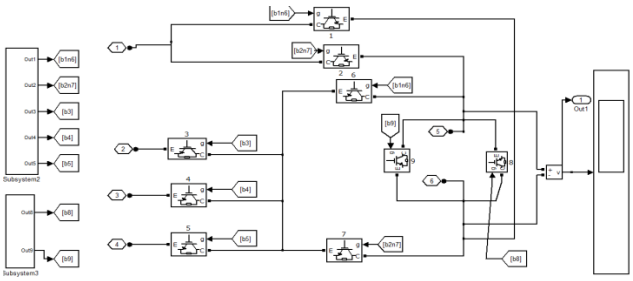


Figure 3 single phase structure of proposed multilevel inverter

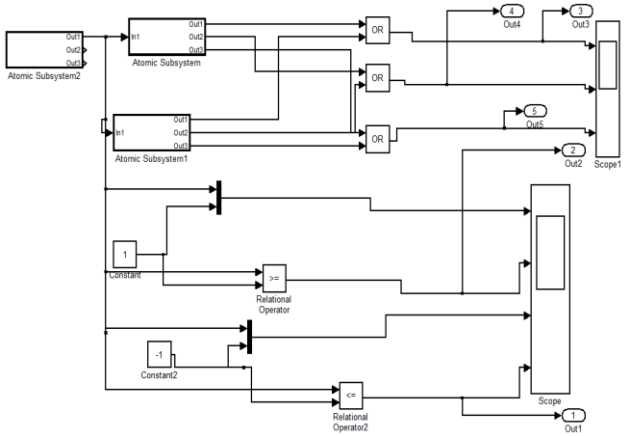
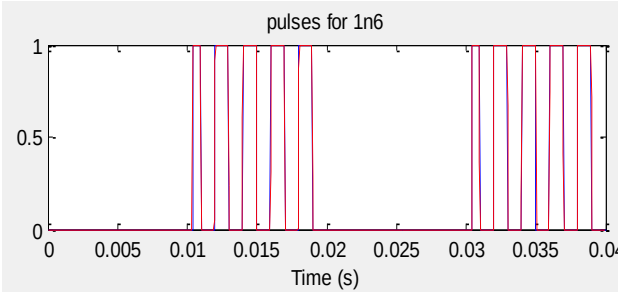


Figure 4 showing pulse generation circuit for switch 1 to 7



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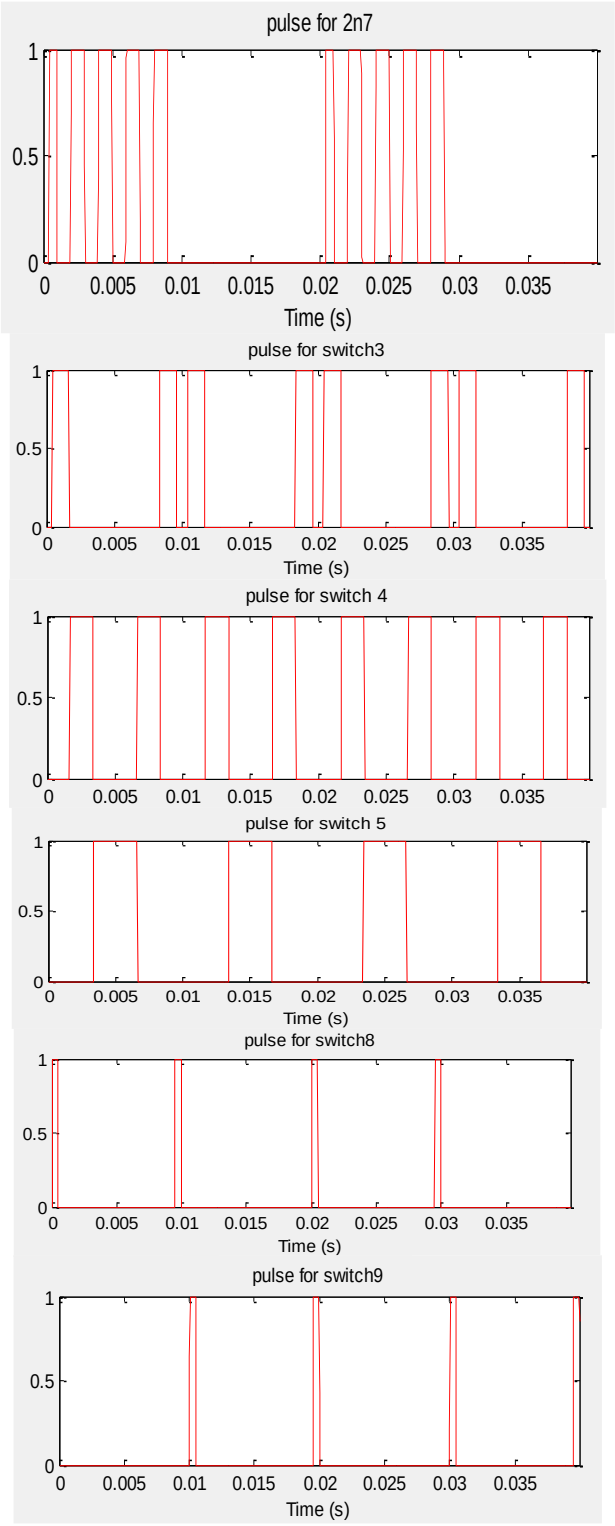

Figure 5. Firing pulses for switches using PWM Technique

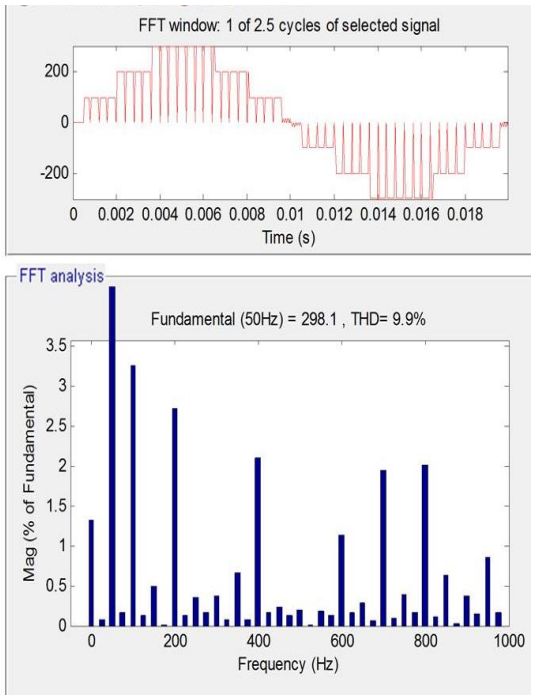

Figure 6 Showing FFT analysis of phase A voltage

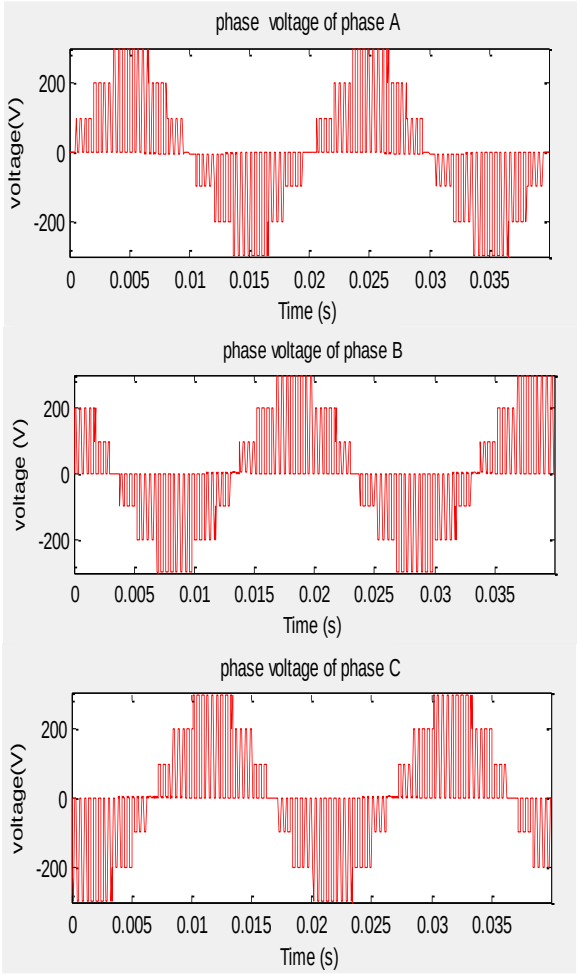

Figure 7 output phase voltage of proposed multilevel

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V. SIMULATION OF THE PROPOSED MULTILEVEL INVERTER

The matlab simulated circuit of 3-phase proposed inverter is shown in fig 2 and their one of the phase shown in fig 3. The IGBT used as a switch in proposed multilevel. The matlab circuit used for generating pulses using PWM is shown in the fig 4. The pulse generated by the circuit shown in the fig 5. The PWM technique is used to obtain a good harmonic spectrum. The gating pulse is generated from above mentioned technique and given separately to the respective IGBTs. The supply is given through three DC sources which are common for all three phases. All three voltage source have same value.

VI. SIMULATION RESULT

For verifying the validity of the proposed multilevel inverter in the generation of the desired output voltage waveform, prototype is simulated based on the proposed topology shown in fig 2 and fig 3. All the DC voltage source is same because the proposed multilevel is symmetrical type. The multilevel inverter is adjusted to produce a 50-Hz, 7-level staircase waveform. The parameter selected for testing are (a) L=50mH with R=100Ω (b) R=100Ω (c) V_{dc}=100 V.

The output waveform of a single phase is shown in fig 6 with their corresponding fourier spectrum. The total harmonic distortion(THD) is one of the measure harmonics in waveform. From fig 6 we have the THD in voltage waveform of phase A is 9.9% which is better.

The phase voltage of all the three phase is shown in fig 7. From fig 7 the output is staircase with 7-level and phase shifted with each other exactly by 120°.

VII. CONCLUSION

A novel three phase multilevel inverter topology has been proposed in this paper. The most important feature of the system is being convenient for expanding and increasing the number of output levels simply with less number of switches. This method results in the reduction of the number of switches, losses, cost and also place. With present switching algorithm, the multilevel inverter generates nearly sinusoidal output voltage with very low harmonic content.

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