

Design and Simulation of Two Stage OTA using 0.18 μm and 0.35 μm Technology

Hitesh Modi, Nilesh D. Patel

Abstract— The OTA is an amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source. Operational transconductance amplifier is one of the most significant building-blocks in integrated continuous-time filters. Here we design a two stage operational transconductance amplifier in TSMC 0.18 μm and 0.35 μm technology with all the transistor in the saturation region. The simulated output frequency response is shown for a supply voltage of 1.8V and 3.3V using IC studio in Mentor Graphics. DC gain is 47.86dB and 46.75dB, power consumption is 2mW and 3.2mW and slew rate is 37.58 V/ μs and 31.67 V/ μs for 1.8V and 3.3V respectively.

Index Terms— Two stage operational transconductance amplifier, CMOS analog integrated circuits, Gain and Phase Margin.

I. INTRODUCTION

The implementation of high performance signal processing and signal conditioning block is one of the most important task in real-time system designing. Operational amplifiers (Op-amps) are one such among various essential components of any kind of signal processing task ranging from simple amplification of weak signals to complex audio and video processing applications in mixed-signal domain.

The OTA is an amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source. There is usually an additional input for a current to control the amplifier's transconductance. An OTA is similar to a standard operational amplifier in that it has a high impedance differential input stage and that it may be used with negative feedback. Portable electronics with low-voltage operation finds big markets. However, the threshold voltage is not reduced proportionally with the supply voltage. Thus, the threshold voltage is becoming a restraint for many analog circuits. Some special techniques are used to overcome the size of the threshold voltage, e.g. floating gate transistors, bulk-driven transistors, continuous-time filters and low threshold transistors. They suffer from several drawbacks or need special fabrication steps, which increases the cost. It is preferred to implement low-voltage circuits using a standard CMOS technology.

OTA is the most important building block in analog circuits, the amplifier faces another difficulty in the low-voltage design, providing high gain and high output swing with lowpower consumption. The usual way to boost the gain, cascading of transistors, is not possible in

low-voltage design due to its output swing limitation. Alternatively, cascading transistor, i.e. the multi-stage amplifier, is adopted.

The objective of the design methodology in this paper is to propose a simple but accurate equation for the design of high gain two stage CMOS operational transconductance amplifier. To do this, a simple analysis with some significant parameters (gain, phase margin, gain margin, slew rate etc.) is performed. Process maintains a wide variety of specifications and constraints. In this paper, we formulate the CMOS operational transconductance amplifier design problem and their aspect ratios.

The simulation results have been obtained by TSMC 0.18 μm and 0.35 μm on CMOS technology.

II. BLOCK DIAGRAM OF TWO STAGE CMOS OTA

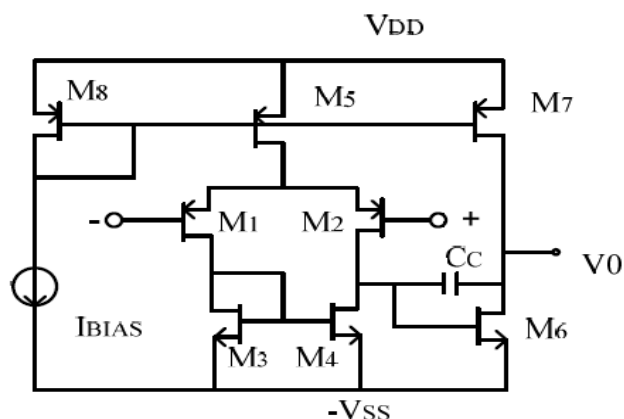


Fig.1 Two stage CMOS operational Amplifier[2]

A. Input Resistance, Output Resistance and Open-circuit Voltage Gain

The first stage in Figure 1 consists of a p-channel differential pair M1-M2 with an n-channel current mirror load M3-M4 and a p-channel tail current source M5. The second stage consists of an n-channel common-source amplifier M6 with a p-channel current-source load M7. Because the OP-AMP inputs are connected to the gates of MOS transistor, the input resistance is essentially infinite when the OP-AMP is used in internal applications. For the same reason, the input resistance of the second stage of the OP-AMP is also essentially infinite. The output resistance is the resistance looking back into the second stage with the OP-AMP inputs connected to small signal ground:

$$R_0 = r_{O6} \parallel r_{O7} \quad (1)$$

Manuscript received on February 13, 2013.

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Where R_0 =output resistance and r_{o6} and r_{o7} are the internal resistance of transistor M6 and M7 respectively. Although this output resistance is almost always much larger than in general purpose bipolar OP-AMP, low output resistance is usually not required when driving purely capacitive loads. Since the input resistance of the second stage is essentially infinite, the voltage gain of the amplifier in Figure 1 can be found by considering the two stages separately. The small signal voltage gain of first stage (basic diff amp) is given by

$$A_{v1} = \frac{v_{O1}}{v_i} = G_{m1}R_{O1} \quad (2)$$

Where V_{O1} , v_i , G_{m1} and R_{O1} are output voltage of first stage, input differential voltage, the transconductance and output resistance of the first stage respectively.

$$A_{v1} = g_{m1}(r_{O2} \parallel R_{O4}) \quad (3)$$

Where A_{v1} , g_{m1} , r_{O2} , R_{O4} are the voltage gain of first stage, transconductance of transistor M1, internal resistance of M2 and output resistance of M4 respectively.

Similarly, the second stage voltage gain is

$$A_{v2} = g_{m6}R_0 \quad (4)$$

Where R_0 is given in (2.1).As a result, the overall gain of the amplifier is

$$A_v = A_{v1}A_{v2} = g_{m1}(r_{O2} \parallel r_{O4})g_{m6}(r_{O6} \parallel r_{O7}) \quad (5)$$

This equation shows that the overall gain is related to the quantity $(g_{mR_0})^2$.

$$g_{mR_0} = \frac{2V_A}{V_{ov}} \quad (6)$$

Therefore, the overall voltage gain is a strong function of the early voltage and the overdrive. In which early voltage (V_A) is proportional to the effective channel length and V_{ov} is set by the bias conditions. The overall gain can be increased by either increasing the channel length of the devices to increase the early voltages or by reducing the bias current to reduce the overdrives.

B. Output Swing

The output swing is defined to be the range of output voltage $V_o = V_0 + v_0$ for which all transistors operate in the active region so that the gain calculation in (5) is approximately constant. From inspection of Figure 1, M6 operates in the triode region if the output voltage is less than $V_{ov6} - V_{ss}$. Similarly, M7 operates in the triode region if the output voltage is more than $VDD - |V_{ov7}|$. Therefore, and the output swing is

$$V_{ov6} - V_{ss} \leq V_o \leq VDD - |V_{ov7}| \quad (7)$$

Where V_{ov6} and V_{ov7} shows the overdrives voltage of M6 and M7 respectively. This inequality shows that the OP-AMP can provide high gain while its output voltage swings within one overdrive of each supply. Beyond these limits, one of the output transistors enters the triode region, where the overall gain of the amplifier would be greatly diminished. As a result, the output swing can be increased by reducing the overdrives of the output transistors.

C. Input Offset Voltage

The input offset voltage of a differential amplifier was defined as the differential input voltage for which the

differential output voltage is zero. Because of the OP-AMP in Figure 1 has a single-ended output, this definition must be modified here. The voltage between the output node and ground as the output voltage, the most straightforward modification is to define the input offset voltage of the OP-AMP as the differential input voltage for which the OP-AMP output voltage is zero. This definition is reasonable if $VDD = VSS$ because setting the output voltage to zero maximize the allowed variation in the output voltage before one transistor operates in the triode region provided that $|V_{ov6}| = |V_{ov7}|$. If $VDD \neq VSS$, however the output voltage should be set midway between the supply voltages to maximize the output swing. Therefore, we will define the input offset of OP-AMP with differential inputs and single ended output as the differential input voltage for which the dc output voltage is midway between the supplies.

III. TWO STAGE OTA SCHEMATIC DESIGN

A practical version of the two stage op-amp is shown in the fig. 2 the gain of the op-amp is mainly depends on input differential stage the DC gain is largely unaffected by choice of P-channel or N-channel input pair maximizes the slew rate.

Having a p-channel input first stage implies that the second stage has an n-channel input drive transistor of the second stage, which maximizes the transconductance of the drive transistor of the second stage which is critical when high frequency operation is important.

A. Gain

It is the ratio between output voltage and differential input voltage. Because the output signal is much larger than the input signal, so it is commonly called as large signal voltage gain.

B. Phase Margin

The absolute value of the open-loop phase shift between the output and the inverting input at the frequency at which the modulus of the open-loop amplification is unity.

C. Slew Rate

The average time rate of change of the closed-loop amplifier output voltage for a step-signal input.

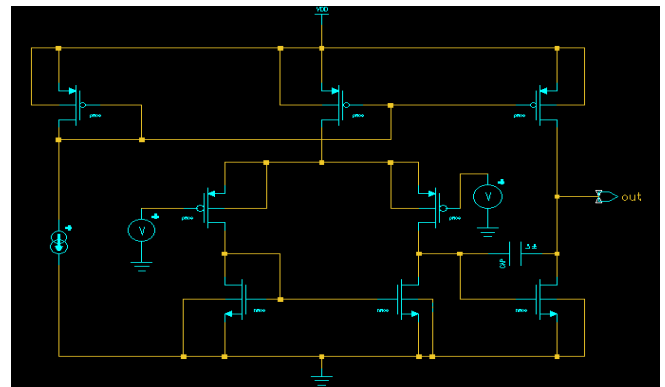


Fig. 2 Schematic design of two stage CMOS OTA

D. Gain Margin

The reciprocal of the open-loop voltage amplification at the lowest frequency at which the open-loop phase shift is such that the output is in phase with the inverting input.

IV. SIMULATION RESULT

The simulated output frequency response is shown in fig. 3, 4, 5 and 6 here 0.18 μ m TSMC IC studio is used for simulation. The DC Gain is found to be 47.86 dB, Gain Margin is 15.40 dB, Phase Margin is 217.53 $^{\circ}$ and Slew Rate is 37.58V/ μ s.

Gain:

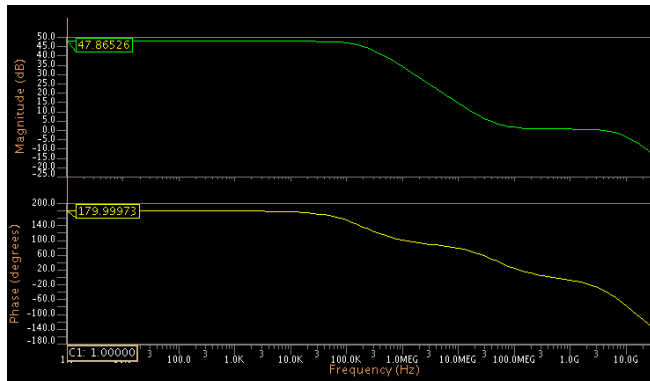


Fig. 3 Result of Gain at 1.8v

Gain Margin:

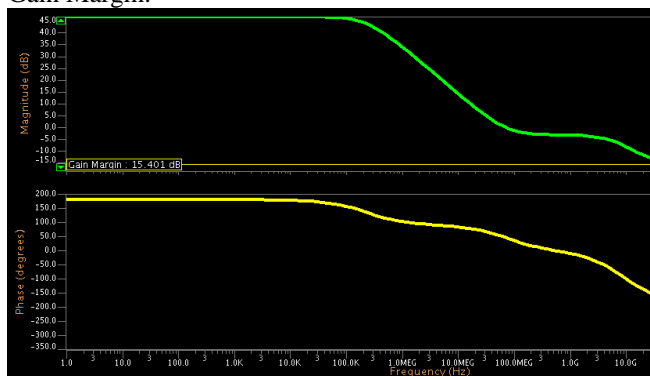


Fig. 4 Result of Gain Margin at 1.8v

Phase Margin:

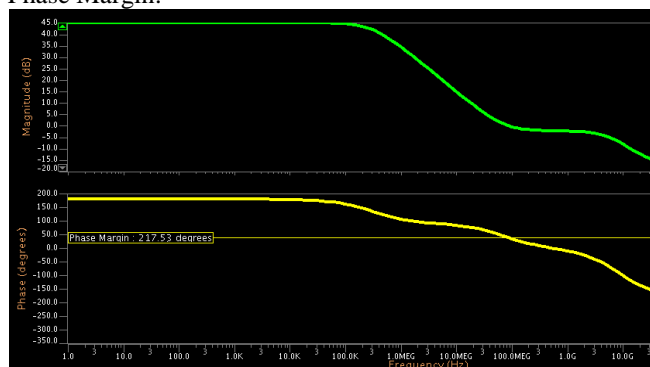


Fig. 5 Result of Phase Margin at 1.8v

Slew Rate:

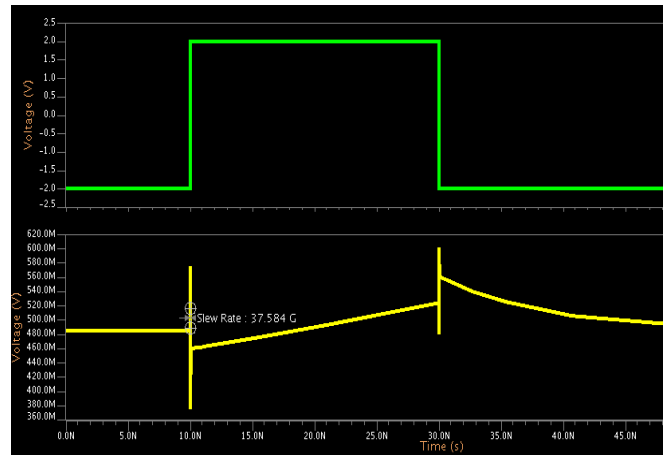


Fig. 6 Result of Slew Rate at 1.8v

The simulated output frequency response is shown in fig. 7, 8, 9 and 10 here 0.35 μ m TSMC IC studio is used for simulation. The DC Gain is found to be 46.75 dB, Gain Margin is 16.94 dB, Phase Margin is 225 $^{\circ}$ and Slew Rate is 31.67V/ μ s.

Gain:

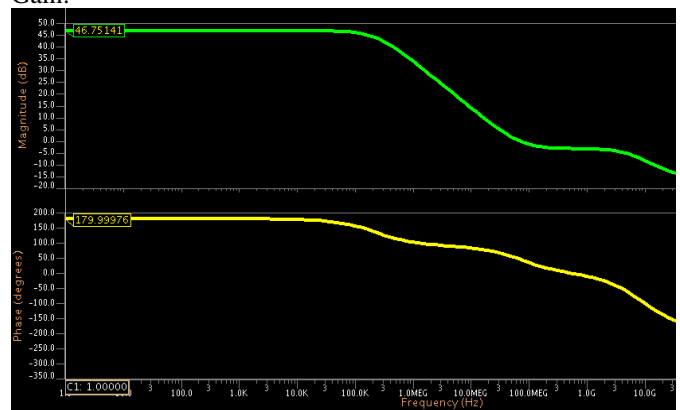


Fig. 7 Result of Gain at 3.3v

Gain Margin:

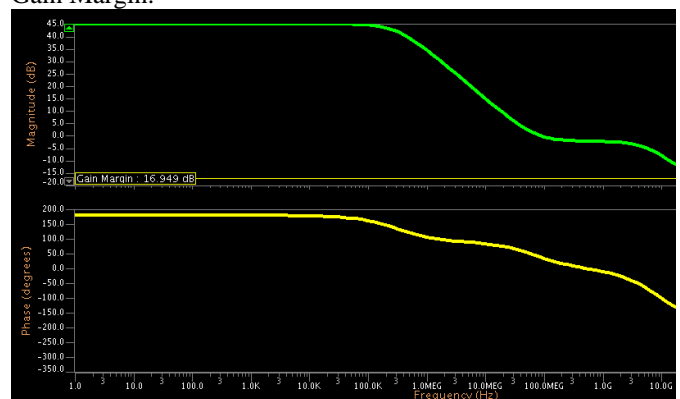


Fig. 8 Result of Gain Margin at 3.3v

Phase Margin:

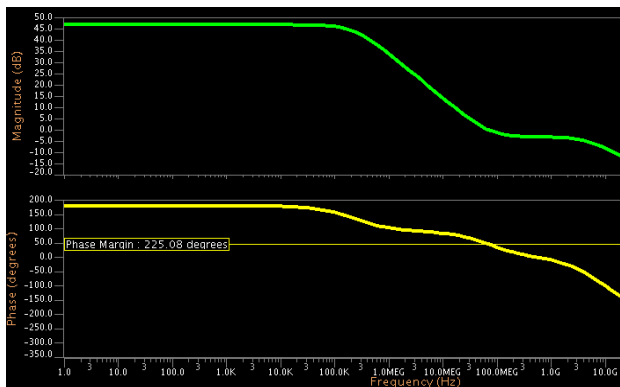


Fig. 9 Result of Phase Margin at 3.3v

Slew Rate:

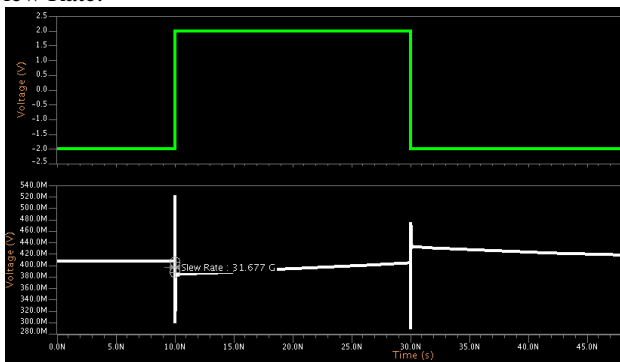


Fig. 10 Result of Slew Rate at 3.3v

Table I: The Design Parameter

Transistors	W/L Ratios	
	0.18 μm	0.35 μm
M1	25 μm	30 μm
M2	25 μm	30 μm
M3	10 μm	18 μm
M4	10 μm	18 μm
M5	20 μm	20 μm
M6	10 μm	20 μm
M7	10 μm	20 μm
M8	34 μm	40 μA
C_L	10pF	10 pF

Table II: Simulation Result

Parameters	Technology	
	0.18 μm	0.35 μm
Power Supply	1.8V	3.3V
Gain	47.86dB	46.75dB
Gain Margin	15.40dB	16.94dB
Phase Margin	217.53 $^\circ$	225 $^\circ$
Slew Rate	37.58 V/ μs	31.67 V/ μs
Power Dissipation	1.3mW	3.2mW

V. CONCLUSION

In this paper two stage OTA is optimized and simulated in 0.18 μm and 0.35 μm technology. Power supply of the architecture is 1.8V. Gain is 47.86 dB, gain margin is 15.40 dB and phase margin is 217.53 $^\circ$. Slew rate is 37.58 V/ μs and power dissipation is 1.3 mW and Power supply of the architecture is 3.3V. Gain is 46.75 dB, gain margin is 16.94 dB and phase margin is 225 $^\circ$. Slew rate is 31.67 V/ μs and power dissipation is 3.2 mW. In my simulation result gain margin, phase margin, slew rate and power dissipation is very excellent result.

ACKNOWLEDGMENT

Author thanks the team of Laljibhai Chaturbhai Institute of Technology College for the facilities provided and consistent encouragement.

REFERENCES

1. Majid Memarian Sorkhabi and Siroos Toofan, "Design And Simulation of High performance Operational Transconductance Amplifier", Canadian Journal on Electrical and Electronics Engineering Vol. 2, No. 7, July 2011.
2. Bhavesh H. Soni, Rasika N. Dhavse, "Design of Operational Trans-conductance Amplifier Using 0.35 μm Technology", International Journal of Wisdom Based Computing, Vol. 1(2), August 2011.
3. Reetesh V. Golhar and Mahendra A. Gaikwad and Vrushali G. Nasre, "Design and Analysis of High Performance Operational Transconductance Amplifier", International Journal of Scientific and Research Publications, Volume 2, Issue 8, August 2012.
4. Carsten Wulff and Trond Ytterdal, "High Speed, High Gain OTA in a Digital 90nm CMOS Technology".
5. M.Yousefi and A.Vatanjou and F.Nazeri, "High-Speed High-Gain CMOS OTA for Switched Capacitor Applications", World Academy of Science, Engineering and Technology 2012.
6. Zahra Haddad Derafshi and Mohammad Hossein Zarifi, "Low-Power High-Speed OTA in 0.35 μm CMOS Process", European Journal of Scientific Research ISSN 1450-216X Vol.37 No.3, 2009.
7. Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGRAW-Hill international edition, p.p. 291-335
8. R. Jacob Baker, Harry W. Li and David E. Boyce, CMOS Circuit Design, Layout, and Simulation, IEEE press, p.p 617-674

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