Low Voltage, High Gain CMOS Op Amp Using Nested Transconductance Compensation Capacitance

Hardik Patel, Rajnikant Soni

Abstract— An analytic design guide was formulated for the design of 3-stage CMOS OP amp with the nested Gm-C(NGCC) frequency compensation. The proposed design guide generates straight-forwardly the design parameters such as the W/L ratio and current of each transistor from the given design specifications, such as, gain-bandwidth, phase margin, the ratio of compensation capacitance to load capacitance. The applications of this design guide to the 10pF load capacitances, shows that the designed OP amp work with a reasonable performance in both cases, for the range of compensation capacitance from 10% to 100% of load capacitance.

Index Terms—Low voltage OP amp, design guide, frequency compensation, nested Gm-C

I. INTRODUCTION

As the minimum feature size of CMOS integrated circuits has been scaled down to nano-meter regime in recent years, the power supply voltage continues to scale down. However, the threshold voltage is not scaled down proportionally to the supply voltage due to the subthreshold leakage problem. Therefore, the design of analog circuits is becoming more difficult and challenging. The operational amplifier (OP amp), which is an important analog building block, is a good example to demonstrate the challenges in design of analog circuit with the nano-meter CMOS process . Since, the conventional cascode structure of the high-gain OP amp requires multiple stacks of transistors between power supply and ground; it is difficult to design in low-voltage environment. As the solution to the design limits of cascode structure in low-voltage environment, the multistage amplifiers (cascade structure), which achieve the high gain by cascading multiple gain stages, have been researched. The multistage amplifier is more suitable to low-voltage applications, because the required number of stacks is less than cascode structure. However, since the multistage amplifier consists of multiple gain stages, it requires a complex frequency compensation scheme to ensure stability.

There are two representative frequency compensation techniques: Nested Miller Compensation (NMC) and Nested Gm-C Compensation (NGCC). Most of the frequency compensation techniques are based on two major fundamental principles: pole-splitting and pole zero cancellation. In the case of NMC, due to the stability problem caused by the positive real zero, a series resistance to the miller capacitance is used in general for CMOS OP amps. The transfer function, stability, and phase margin conditions of multistage NMC amplifier are complicated to apply analytic design methodology. However, for multistage NGCC amplifier, a zero removal with feed-forward path is applied, which makes the transfer function, stability, and phase margin conditions relatively simple to apply analytic design methodology.

The design guide of multistage NGCC amplifier, proposed in previous paper , is not a completely systematic design guide. In this paper, a systematic design guide of 3-stage NGCC amplifier, which enables the systematic design of 3-stage NGCC amplifier with given design specifications, is proposed. The comparison between NMC with series resistance and NGCC will be presented in section II. The proposed systematic design guide of 3-stage NGCC amplifier will be described in section III. In section IV, the simulation results of 3-stage NGCC amplifier designed by the proposed design guide will be shown.

II. FREQUENCY COMPENSATION TECHNIQUES

In this section, two major frequency compensation techniques: NMC and NGCC will be briefly introduced, and also the comparison of characteristics for both techniques will be described. The frequency compensation for 2-stage amplifier is performed by using a Miller capacitance. The feed-forward current path through the Miller capacitance will generate the righthalf- plane (RHP) zero , which degrades the phase margin. The RHP zero is removed by using a series resistanceto the compensation capacitance, as shown in Fig. 1 and 2.

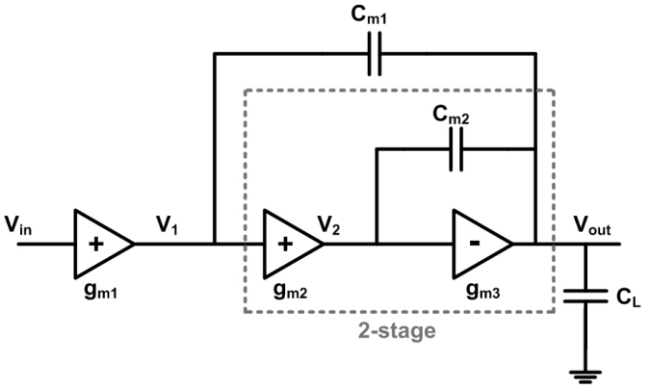

Fig. 1 Nested Miller Compensation

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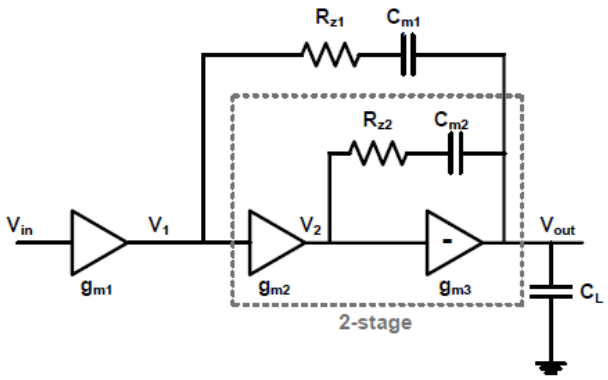

Fig. 2 NMC with series resistor

III. DESIGN GUIDE OF 3-STAGE NGCC AMPLIFIER

In this section, a systematic design guide is derived for the 3-stage OP amp using the NGCC frequency compensation technique. The design specifications include the gain-bandwidth product (GB), the high frequency pole (ω_3) to GB, the phase margin(PM), the output loading(C_L), and the input common-mode voltage range(ICMR).

A. Stability and Phase Margin

The stability condition of 3-stage NGCC OP amp indicates that the pole (ω_3) generated by the loading capacitance (C_L) and the 3rd gain stage, should be higher than ω_1 . The frequency relation based on the stability condition can be written as

$$\omega_3 > \omega_1 \qquad (1)$$

In general, the inequality of $\omega_1 < \omega_2 < \omega_3$ holds.

B. Current and W/L Ratio of Each Stage

In order to calculate the current and W/L ratio of each stage from the transconductance (g_{mi}) values acquired from previous subsection, the V_{DSAT} values of transistors are determined from the specification of the input common-mode voltage range (ICMR). The W/L ratios of input transistors in the 1st gain stage should be large enough to enhance the equivalent input noise voltage. Thus, V_{DSAT} values of the input transistors in the 1st gain stage were set to half of the V_{DSAT} values of the transistors, composing the active load of input differential pair and current sources. Besides, the V_{DSAT} values of all the gain-path transistors (g_{mi} i=1,2,3) are set to be the same as V_{DSAT} of the input transistor of 1st gain stage. Then, the ICMR of PMOS differential pair with NMOS active load is given by

$$\text{ICMR} = V_{DD} - 5V_{DSAT} - V_{TH} \qquad (2)$$

Where, V_{DSAT} is the value of the input transistor in the 1st gain stage. To guarantee that the ICMR is greater than 1/3 of supply voltage, the following condition should be satisfied.

$$V_{DSAT} \le \frac{1}{5}\left(\frac{2}{3}V_{DD} - V_{TH}\right) \qquad (3)$$

$$\left(\frac{W}{L}\right)_i = \frac{g_{mi}^2}{2\mu C_{ox} I_{Di}} \qquad (4)$$

Where i=1,2,3

Compensation Capacitor

$$C_{m1} = k\frac{g_{m1}}{g_{m3}}C_L \qquad (5)$$

$$C_{m2} = \frac{k^2}{1+2k}\frac{g_{m2}}{g_{m3}}C_L \qquad (6)$$

IV. SIMULATION RESULTS

The NGCC 3-stage amplifier shown in Fig. was designed using a 0.18µm CMOS process. Power supply voltage was set to 1.2V. and C_L=(1)10pF. The gate lengths of all MOSFETs were set to 0.5um, about 3 times the minimum feature size. Fig. shows the simulated frequency response when the value of C_L set to 10pF respectively.

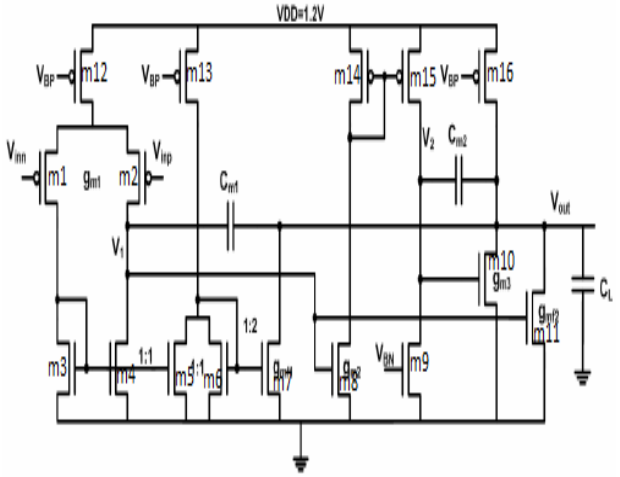

Fig. 3 Three stage NGCC

Design Parameters And Simulation Results

Table I- The Design Parameter

M1	W/l=24um/0.5um
M2	W/l=24um/0.5um
M3	W/l=24um/0.5um
M4	W/l=24um/0.5um
M5	W/l=24um/0.5um
M6	W/l=24um/0.5um
M7	W/l=24um/0.5um
M8	W/l=4um/0.5um
M9	W/l=4um/0.5um
M10	W/l=54um/0.5um
M11	W/l=54um/0.5um
M12	W/l=24um/0.5um
M13	W/l=24um/0.5um
M14	W/l=4um/0.5um
M15	W/l=4um/0.5um
M16	W/l=54um/0.5um

C_{m1}	3pf
C_{m2}	1.5pf
C_L	10PF

Transient Analysis In 180nm Technology

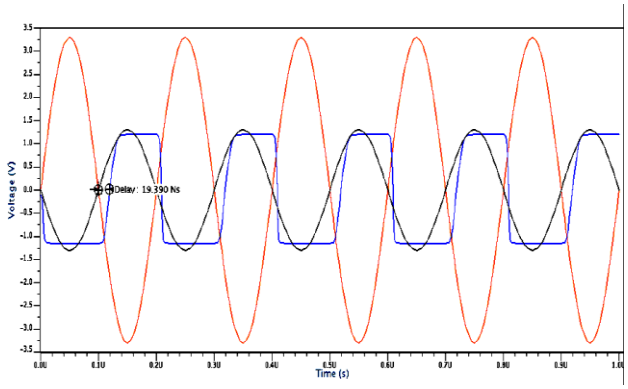

Fig 4. Transient analysis in 180nm technology

Transient Analysis In 250nm Technology

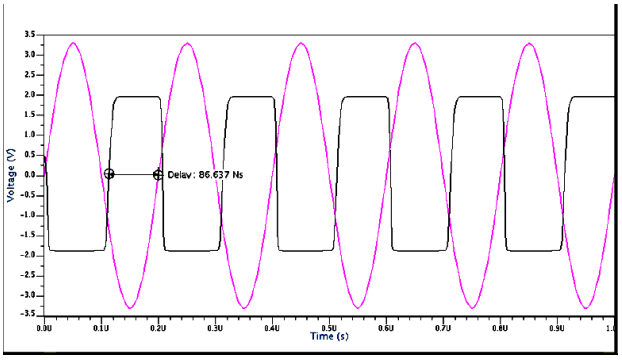

Fig 5. Transient analysis in 250nm technology

Ac Response In 180nm Technology

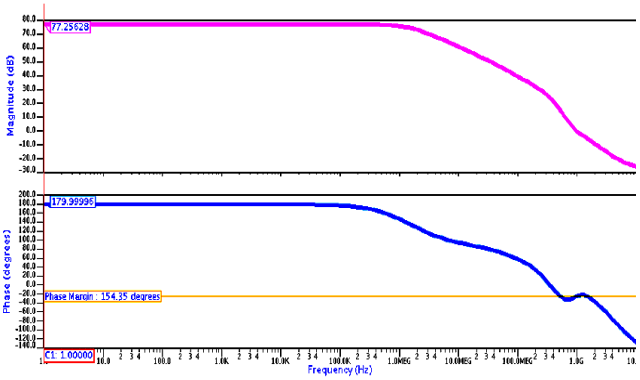

Fig 6.AC response in 180nm technology

Ac Response In 250nm Technology

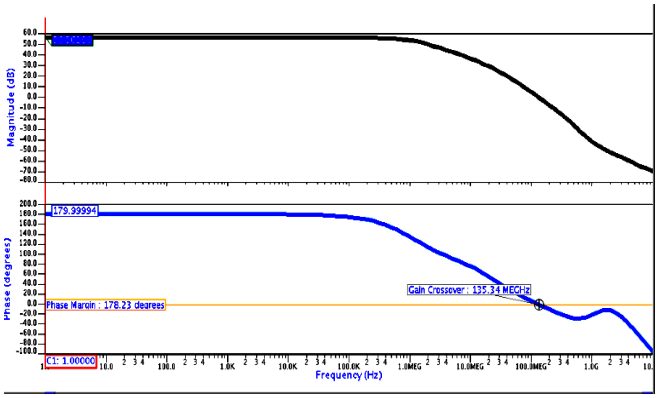

Fig 7.AC response in 250nm technology

Offset Analysis In 180nm Technology

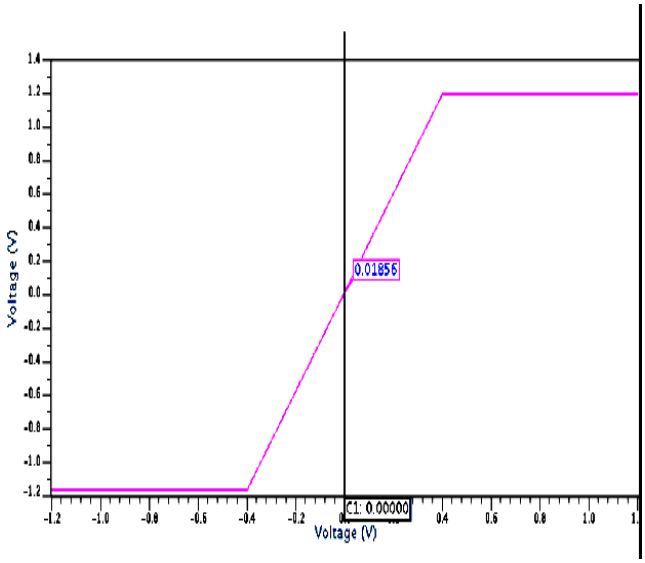

Fig 8.Offset analysis in 180nm technology

Offset Analysis In 250nm Technology

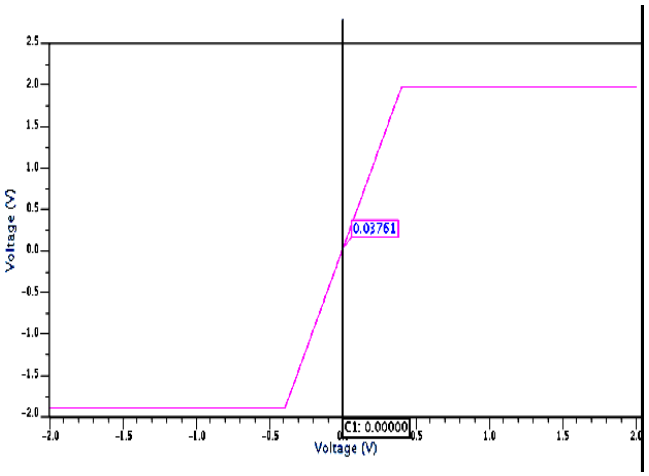

Fig 9.Offset analysis in 250nm technology

V. COMPARISON TABLE

Parameters	Technology	
	180nm	250nm
Supply voltage	1.2v	2v
Gain	77.25db	56.34db
Phase margin	154.35degree	178.23degree
Offset	0.018v	0.037v
Delay	19.13ns	86.68ns

VI. CONCLUSION

In this paper, an analytic design guide of 3-stage NGCCOP amp for low-voltage application was proposed. A 3-stage NGCC OP amp was designed by using the proposed design guide.

A 0.18µm CMOS process with 1.2V supply voltage and 0.25µm CMOS process with 2V supply voltage was used in the design. Here we get the 77.25db gain in 180nm technology and 56.34db gain in 250nm technology.

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