

A Novel Control Strategy for High Efficient SSPFC Topology

Sakkeer Hussain C.K, R. Muthukumar, A. Rathnam

Abstract— The conventional SSPFC (single-stage power factor correction) converters suffer from low efficiency because of high voltage and current stresses acting on switching devices and other circuit parameters. The introduction of resonant converters along with the conventional SSPFC provides a very sensible solution for the above mentioned problem. Since this resonant SSPFC converter operation carried out with variable frequency, it provides an efficient operation only at full load. Below full load, the operation results in efficiency drop due to the shift from resonant frequency. A load dependent strategy helps in maintaining the efficiency level as constant even below full load. Two variables are to be controlled in this circuit, which are resonant frequency and duty ratio. Normally two controllers are essential to perform the operation which cause increased cost and requires more processing time. This paper proposes a single PI controller to control the both variables to provide high converter efficiency and to reduce the cost and the processing time. The proposed system provides a constant efficiency in conversion process up to 50% of full load current. The MATLAB simulation is presented to verify the performance analysis.

Index Terms— AC/DC converters, power factor correction converters, PI controller, resonant converter.

I. INTRODUCTION

For any electronic equipment, the switch mode ac/dc converters provide the first functional block to supply the power from ac mains to rest of the circuit elements. So these switch mode converters must have some acceptability criterions suitable for both the ac mains and the output load. A good power quality, such that purely sinusoidal input current and input voltage waveforms is essential from the ac mains points of view. Similarly, well regulated output voltage and high conversion efficiency are also required from output and energy conversion point of view. But the normal ac/dc switch mode converters cause some problems on ac side such that input waveform distortion, voltage drop and electromagnetic interference due to high frequency switching. The power factor correction circuitry is proposed to meet the above mentioned problems. There are mainly two methods are mentioned in literatures for the input power factor correction; passive and active power factor correction.

Passive power factor correction can be achieved with the help of passive reactive elements. Even though it is simple and direct method, its size, weight and cost at low frequencies limits its applications [1]. In active method, power electronic switches are used to attain the input power factor correction. The conduction time of these switching devices are controlled to make the voltage and current waveforms in phase and distortion less. High power factor, low harmonics, low weight and high reliability are the major advantages of active PFC [2]. The active PFC can be implemented in two different ways; two-stage and single-stage power factor correction. The two-stage PFC circuit consists of a power factor pre-regulator and a dc-dc converter. This method has the advantages such as high power factor, low input harmonics but the cost, size and efficiency are more superior [3]. The single-stage power factor correction circuit provide all the features of two-stage PFC in addition to small component size, low switching loss and cost effective due to less number of switches [4].

In both two-stage and single-stage PFC, dc-dc converters are used as the input current shaper. All basic types of dc-dc converters have the “self power factor correction” capability while they are operating in discontinuous conduction mode. Boost converter is the most suited dc-dc converter for the power factor correction purpose [5]. Most of SSPFC converters cascade a boost converter with a forward dc-dc converter and an energy storage capacitor in between, provides input power factor correction, isolation and also output voltage regulation in a single stage [6]. The switching operation is controlled by the appropriate SPWM technique [7]. When a small capacitor is used for the energy storage purpose, the SSPFC leads large ripples in the output voltage. If a large capacitor is used, it causes floating of dc-bus voltage that will results in high voltage stress across the switches which leads to more switching losses. As in [8], a resonant circuit can solve these problems by controlling stress and switching loss. These SSPFC resonant converters have the flexibility to operate with variable frequency asymmetrical pulse width modulation [9] or with variable frequency phase shift modulation [10]. In both of the cases the operation is carried out with variable frequency. Because of this reason, when the circuit is operating below full load current, the switching frequency may shift from resonant value. This will leads to drop in their conversion efficiency. For maintaining high efficiency even below full load, a load adaptive energy storage technique is introduced in [11]. Here, two variables have to be controlled at a time, namely; the switching frequency to control output voltage and duty ratio to control dc bus voltage level. Two separate controllers increase the cost and the processing time.

Manuscript published on 28 February 2013.

* Correspondence Author (s)

Sakkeer Hussain C.K., Department of Electrical and Electronics Engineering, Paavai Engineering College, Paachal, Namakkal, India.

R. Muthukumar, Asst.Professor, Department of Electrical and Electronics Engineering, Paavai Engineering College, Paachal, Namakkal, India.

A. Rathnam, Asst.Professor, Department of Electrical and Electronics Engineering, Paavai Engineering College, Paachal, Namakkal, India.

© The Authors. Published by Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP). This is an [open access](http://creativecommons.org/licenses/by-nc-nd/4.0/) article under the CC-BY-NC-ND license <http://creativecommons.org/licenses/by-nc-nd/4.0/>.

In this paper a single PI controller is proposed to attain the load adaptive control of single stage SSPFC resonant AC/DC converter. This will help in providing ripple free output voltage and a well regulated dc-bus voltage with reduced cost and reduced processing time.

II. POWER CIRCUIT

The variable frequency asymmetrical pulse width modulation (VFAPWM) converter topology and its switching sequence are shown in figures 1 and 2.

Figure 1 show a three-level series-parallel LCC (L_s, C_s , and C_p) resonant converter circuit with an input boost inductor (L_{in}) directly connected to the lower pair of the switches. The boost inductor can operate in either DCM or CCM. The dc-bus consists of the two capacitors (C_{b1}) and (C_{b2}). These dc-bus capacitors provide the required hold up time and it will reduce the effect of low frequency ripples in the output voltage. If the capacitors are designed to have equal values and operate symmetrically, each should have half the dc-bus voltage in the normal condition. The two diodes (D_{c1}) and (D_{c2}) acts as clamping diodes which clamp the switch voltages to half that of the dc-bus. The series-parallel resonant converter is used because of the reason that it can operate in a buck-boost mode according to the applied switching frequency. This property is required in order to adjust the output voltage throughout the power cycle. Other peculiar properties of the LCC resonant circuit are fast output regulation and low output voltage ripple as well as: input/output isolation; zero voltage switching; the use of an LC output filter, which results in an almost ripple free output voltage; and high conversion efficiency. Therefore, by designing the converter to operate close to its resonant frequency, high efficiency can be obtained for a wide range of input voltage and output load current. The input filter is used to reduce the high frequency components of the input current, which is especially important in the case of discontinuous input inductor current operation. The output stage is consists of a diode rectifier followed by an LC filter (L_o and C_o) to smooth the output voltage waveform.

OPERATING PRINCIPLE

During the interval ($t_0 < t < t_1$), switches S_3 and S_4 are ON and current through the boost inductor (L_{in}) increases linearly. The current flowing through the switches is the sum of the resonant and boost inductor currents. The voltage across the terminals of the resonant circuit is $-\frac{V_{bus}}{2}$, with capacitor C_{b2} delivering energy to the output through the resonant circuit. This stage of operation ends at $t_1 = DT_s$, where D is the duty ratio of the boost stage and T_s is the switching period.

At the beginning of the next interval ($t_1 < t < t_2$), switch S_4 is turned OFF. The drain-source capacitor of switch S_4 starts charging. When the switch voltage (V_{ds4}) reaches $\frac{V_{bus}}{2}$ (the voltage across C_{b2}), the clamping diode D_{c2} turns on and clamps the switch voltage to half the dc-bus voltage. The voltage across the resonant circuit decreases to zero and the resonant current circulates through switch S_3 and clamping diode D_{c2} . at the end of this period the current in the boost inductor is also diverted to the upper switches, discharging their drain-source capacitors. At $t = t_2$, switch S_3 is turned OFF and its drain-source capacitor gradually charges to $\frac{V_{bus}}{2}$. The inductor current continues to charge the dc-bus

capacitors. The resonant current contributes to the discharge of the switch capacitances and when they are fully discharged, both currents flow through the body diodes of switches S_1 and S_2 as the voltage across the resonant circuit rises to $\frac{V_{bus}}{2}$.

At the beginning of the next stage ($t_2 < t < t_4$), switches S_1 and S_2 are turned ON with zero voltage switching. The voltage across the resonant circuit remains at $\frac{V_{bus}}{2}$, with capacitor C_{b1} delivering energy to the output through the resonant circuit. The current flowing through the switches in this case is the difference between the resonant current and the boost inductor current. At $t = t_4$, switch S_1 is turned OFF. The drain-source capacitor of switch S_1 starts to charge. When the switch voltage (V_{ds1}) reaches $\frac{V_{bus}}{2}$ (the voltage across C_{b1}), the clamping diode D_{c1} turns on and clamps the switch voltage to half the dc-bus voltage. The resonant circuit voltage again drops to zero, with the resonant current circulating through S_2 and D_{c1} .

During the final stage, switch S_2 is turned OFF and its drain-source capacitor gradually charges to $\frac{V_{bus}}{2}$. The resonant current is diverted to discharge the drain-source capacitors of switches S_3 and S_4 . When these capacitors are fully discharged, the body diodes of the switches start conducting. The cycle is repeated with switches S_3 and S_4 being turned ON with zero voltage switching and the boost inductor starts charging in the new switching cycle.

III. CONTROL STRATEGY

As mentioned earlier two control variables are available at a time to control the output voltage and the dc-bus voltage. They are: a) the switching frequency of the resonant converter to control the output voltage and b) the duty ratio, D of the boost converter to regulate the dc-bus voltage to the desired level. A single PI controller is introduced to control the both variables. The schematics of control strategy are shown in figure 3.

The output current feedback is necessary in this circuit to enhance the load adaptive energy storage technique. The actual reference value for the dc bus voltage under full load condition based on the input ac voltage is given as

$$V_{bus(ref)} = 1.285V_m + 200 \quad (1)$$

Where $V_{bus(ref)}$ represents the reference dc-bus voltage and V_m represents the peak value of the input ac voltage. In order to incorporate the load adaptive technique the output current also takes into account for calculating the dc bus reference voltage. Therefore the equation (1) can be re written as

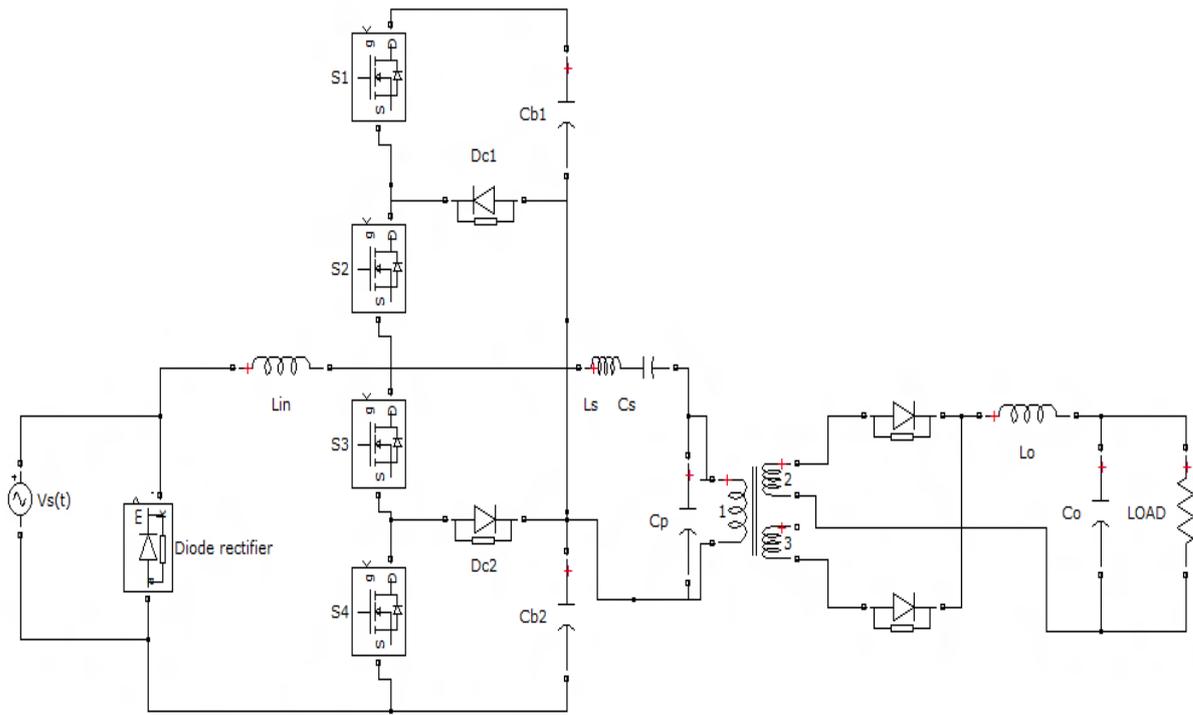


Figure 1:

re 1: SSPFC with VFAPWM topology

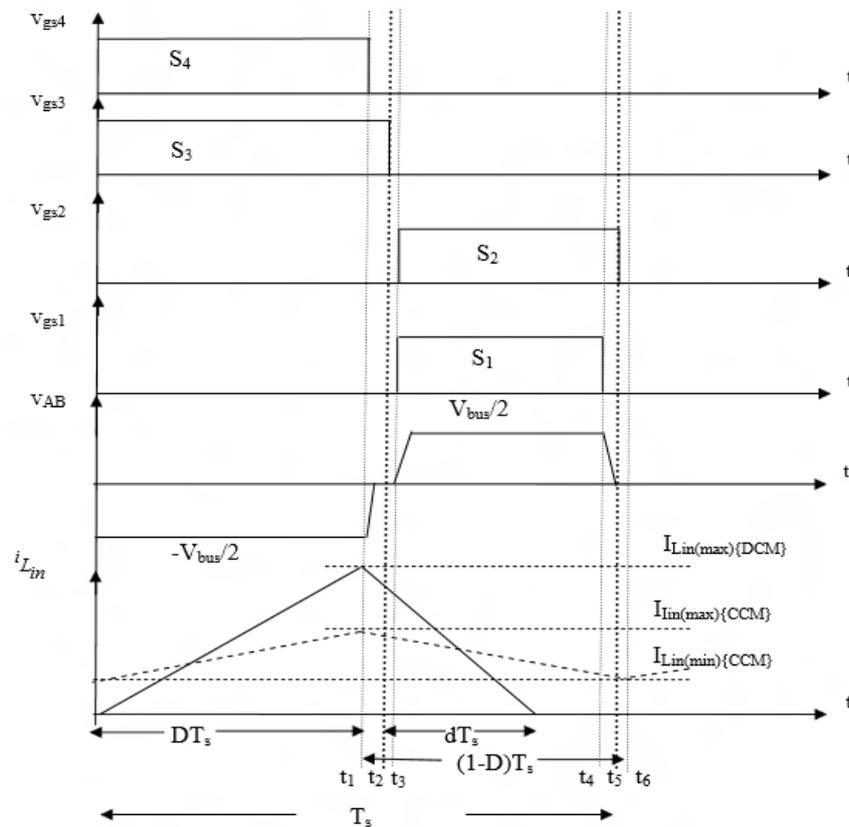


Figure 2: Switching sequence for VFAPWM topology

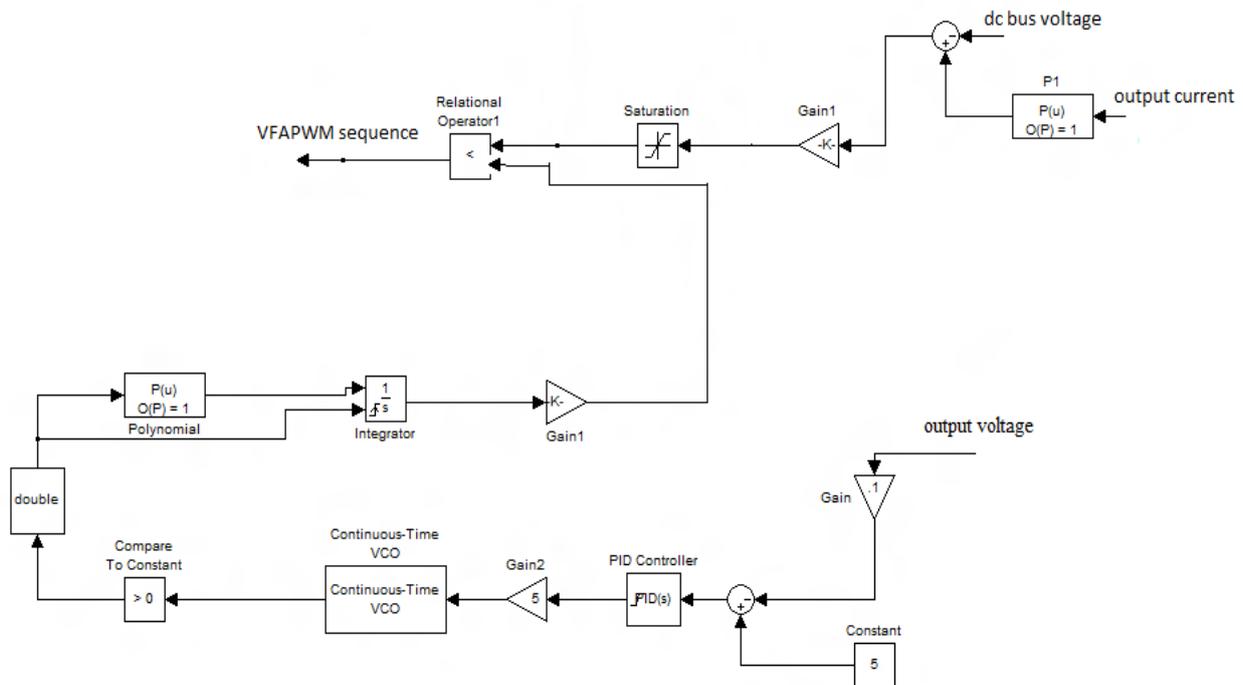


Figure 3: Schematic of control strategy

The output of the PI controller is given to the voltage controlled oscilloscope which generate a continuous-time output signal whose frequency changes in response to amplitude variation of the input signal. The pulse output of the VCO is integrated to get a corresponding triangular wave with the help of a polynomial evaluation block. This triangular wave is compared with the output from the saturation block to form the variable frequency asymmetrical pulse width modulated pulse. This pulse controls the switching operation of various switches present in the boost converter.

$$V_{bus(ref)} = 1.285 V_m + 200 - K \tag{2}$$

Where

$$K = f\left(\frac{I_o}{I_{o(FL)}}\right) \tag{3}$$

In the above equation, the value of f can be selected based on the desired performance and the easiness of implementation. I_o Represents the output current and $I_{o(FL)}$ represents the full load current.

The above reference bus voltage can be realized with the help of a polynomial evaluation block in the MATLAB software. This reference value is compared with the dc bus voltage and the output is given to saturation block to limit the signal to the upper and lower saturation values. Now the output voltage is compared with a constant value and the error signal is fed to the PI controller. The proportional responds quickly to changes in error deviation whereas the integral action is slower but removes offsets between the plant's output and the reference. The basic block of PI controller is shown in figure (4).

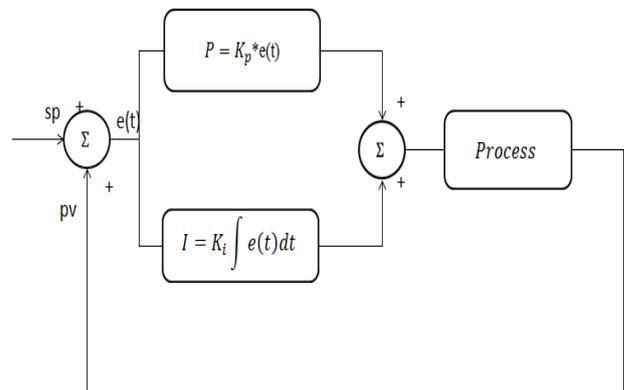


Figure 4: Basic block of PI controller

The controller output is given by

$$K_p * e(t) + K_i \int e(t) dt \tag{4}$$

Where $e(t)$ is the error or deviation of actual measured value (PV) from the reference value (SP).

IV. TEST SYSTEM SPECIFICATIONS

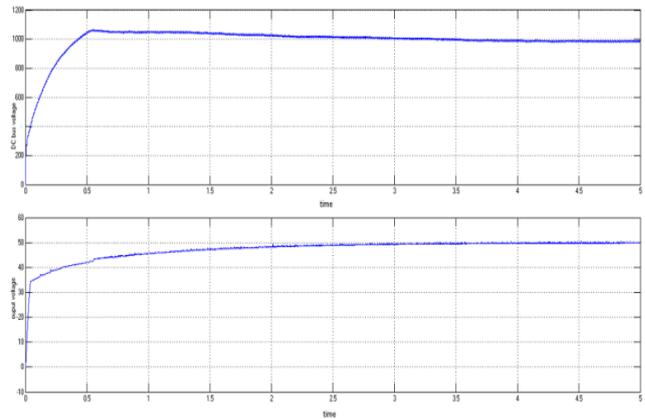
PARAMETERS	VALUES
Input voltage, Vs.	100 V

Input filter	$L=2 \mu\text{H}, C=4.4 \mu\text{H}$
Boost inductor, L_{in}	7 μH
DC bus capacitors, C_{b1}, C_{b2}	560 μF
Series resonant inductor, L_s	22 μH
Series resonant capacitor, C_s	47 nF
Parallel resonant capacitor, C_p	47 nF
Transformer turns ratio, $N_1:N_2$	2:1
Output inductor, L_o	20 μH
Output capacitor, C_o	330 μF

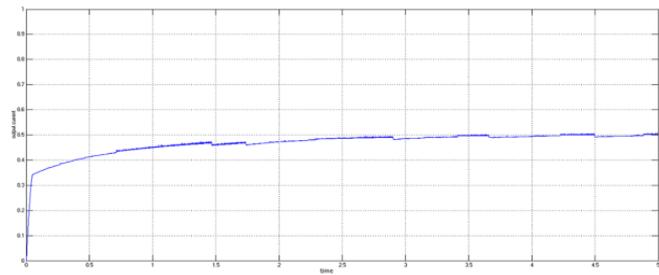
V. EXPERIMENTAL RESULTS

The performance of the proposed system is experimentally analyzed using MATLAB/SIMULINK software. The circuit is designed to get a well regulated constant dc 50V as output. The experimental result shows the proposed system has the capability to meet the requirements of power factor correction and the output. The proposed system provides almost constant conversion efficiency for wide range of loading. The simulation waveforms of output voltage, dc bus voltage, output current, power factor correction and output of resonant converter for the different load currents are shown in figures (5-7).

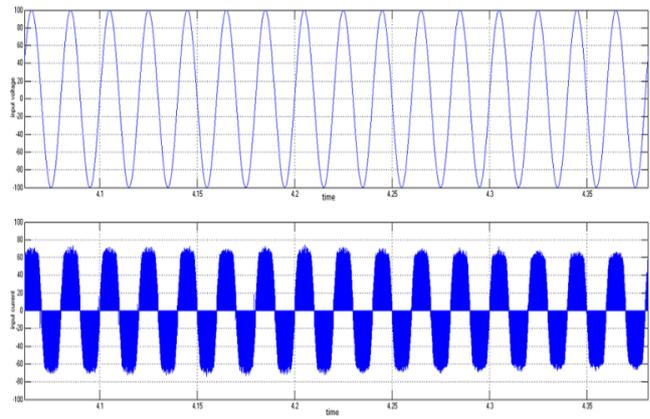
The pulse formation corresponding to the error signal is the basic of the DC output voltage regulation and DC bus voltage regulation. The output DC voltage is compared with the reference signal. The error signal is processed through a PI controller whose control parameters are $K_p = 0.4$ and $K_i = 0.4$ which are selected manually by trial and error process. The PI controller output is given to the voltage controlled oscilloscope which generates a continuous time output signal of amplitude 1V whose frequency varies corresponding to the error signal. This continuous time output signal integrated to get the triangular wave with the help of a polynomial evaluation block. The polynomial co-efficient are given as [1 -0.5]. Now the DC bus voltage is compared with a reference value. This reference value is calculated using the equations (2) and (3) and whose polynomial co-efficient are given as [-2 328.5]. The error signal is saturated to upper and lower values with the help of a saturation block. Now, this output is compared with the triangular wave using a relational operator. If the triangular wave is above saturation reference value, that generates the pulses. The pulse formation is shown in figure 8.



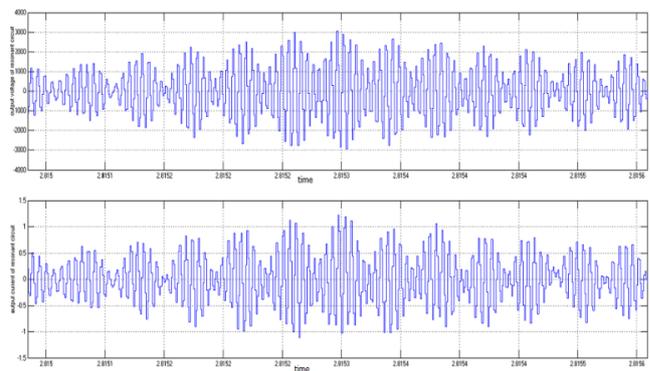
(a)



(b)



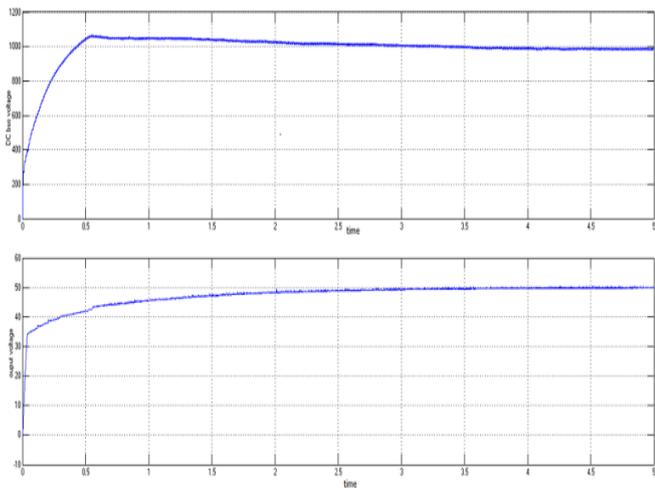
(c)



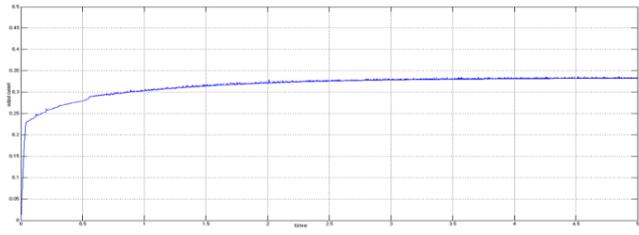
(d)

Figure 5: Experimental waveforms for full load current (a) DC bus voltage and output voltage (b) output current (c) input voltage and current (d) output of resonant circuit

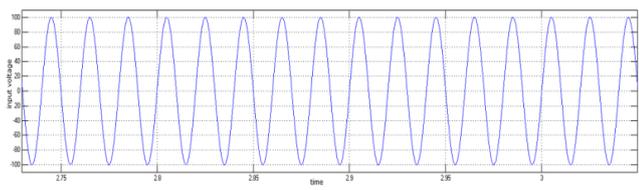




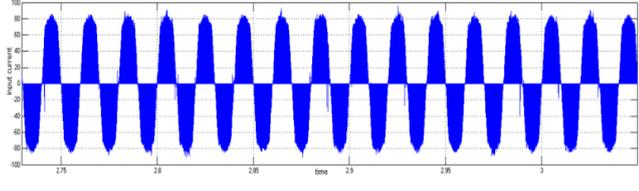
(a)



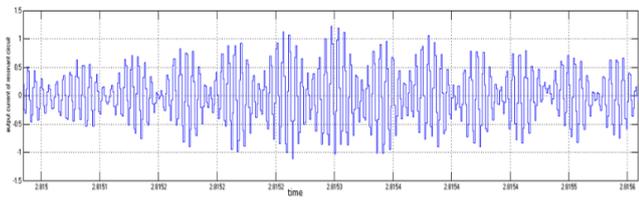
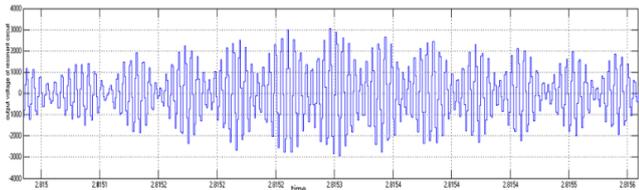
(b)



(c)

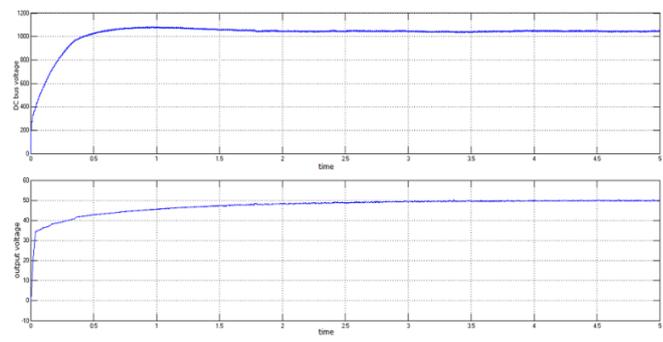


(d)

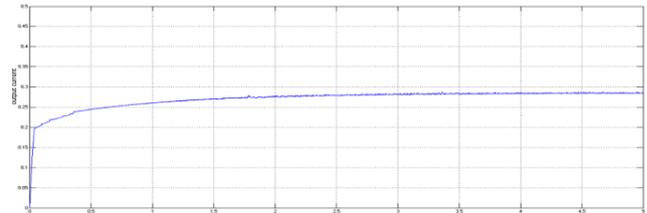


(d)

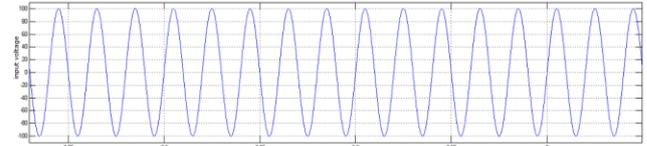
Figure 6: Experimental waveforms for 60% of full load current (a) DC bus voltage and output voltage (b) output current (c) input voltage and current (d) output of resonant circuit



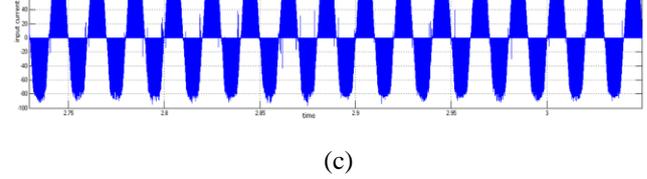
(a)



(b)



(c)



(d)

Figure 7: Experimental waveforms for 40% of full load current (a) DC bus voltage and output voltage (b) output current (c) input voltage and current (d) output of resonant circuit

Figure.5 shows the experimental waveforms for full load current. The figure 5(a) shows the output voltage and DC bus voltage provides constant value. Similarly 5(c) shows the current waveform follows the voltage waveform which gives almost unity power factor. Figure 6, the waveforms for 60% of full load current, as comparing with previous one gives almost the same waveform except for output current.



The figure 7 shows the waveforms for 40% of full load current. In this, 7(c) shows the output of resonant circuit is considerably reduced from the same for full load current and realizes that the efficiency is considerably decreased. All the waveforms shows one thing is that, for any load current, the DC bus voltage, output voltage and input power factor are regular and constant. This highlights the acceptability of the control circuit.

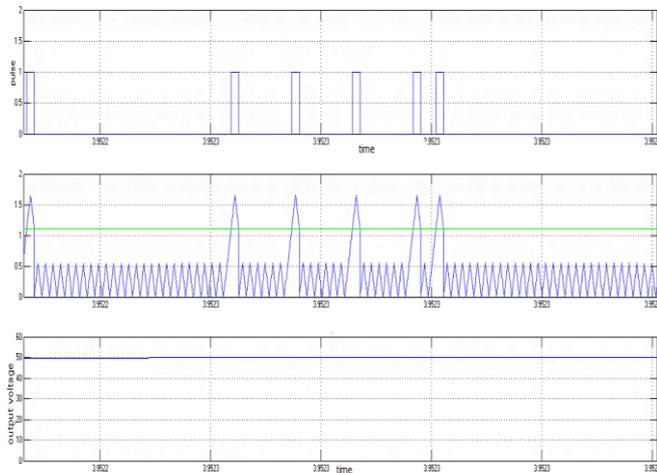


Figure 8: Asymmetrical pulse formation

VI. CONCLUSION

In this paper, a single PI controller is used to regulate output voltage and the dc bus voltage. The proposed control strategy meets the output, dc bus voltage and power factor correction requirements. It provides almost constant conversion efficiency for wide range of loading. The proposed system can handle higher power levels and it reduces the cost and processing time. Manual tuning is used for tuning the PI controller

REFERENCES

- [1] M. Jovanovic & D. Crow, "Merits and Limitations of Full Bridge Rectifier with LC Filter in Meeting IEC 100-3-2 Harmonic Limit Specification," IEEE Transactions on Industry Applications, Vol. 33, No. 2, March 1997, pp. 551-557.
- [2] Z. Yang & P. Sen, "Recent Developments in High Power Factor Switch-Mode Converters," Proceedings of the Canadian Conference on Electrical and Computer Engineering (CCECE) 1998, pp. 477-480.
- [3] G. Spiazzi & S. Buso, "Power Factor Pre-Regulator Based on Combined Buck- Fly back Topologies," IEEE Transactions on Power Electronics, Vol. 15, No. 2, March 2000, pp. 197-204.
- [4] M. Daniele, P. Jain & G. Joos, "Single Stage Power Factor Corrected AC/DC Converter," IEEE Transactions on Power Electronics, Vol. 14, No. 6, Nov. 1999, pp. 1046-1055.
- [5] Huai Wei & Issa Batarseh, "Comparison of Basic converter Topologies for Power Factor Correction" IEEE 1998 pp. 348-353.
- [6] Changming Qiao & Keyue M. Smedly, "A Topology Survey of Single-Stage Power Factor Corrector" IEEE 2000 pp.460-467.
- [7] O. Garcia, J. Cobos, R. Preito, P.Alou & J. Uceda, "Single Phase Power Factor Correction: A Survey" IEEE Transactions on Power Electronics vol.18, No.3, May 2003 pp. 749-755.
- [8] Yu-Lung Ke & Ying-Chun Chuang, "A Novel Single-Stage Power-Factor-Correction Circuit with High Frequency Resonant Energy tank for DC-link Inverter" IEEE Transaction on circuits & systems-II, vol.53, No.2 Feb 2006.
- [9] M.S. Agamy & P.K. Jain, "A new single stage power factor corrected three level resonant AC/DC converter with and without active current control", IEEE Oct. 2005 pp. 1992-1999.
- [10] M.S. Agamy & P.K. Jain, "A single stage PFC three level resonant AC/DC converter using combined phase shift and frequency control" IEEE Nov.2005 pp. 1166-1171.
- [11] M.S. Agamy & P.K. Jain, "An adaptive energy storage technique for efficiency improvement of single-stage three-level resonant AC/DC converters" IEEE Transactions on industry applications Vol.47, No.1 Feb.2011.