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A Comparative Study: Multiplier Design using Reversible Logic Gates

G Padmanabha Sivakumar, S.Rameshwari Devi

Abstract— Low power consumption and smaller area are some of the most important criteria for the high performance systems. Optimizing the speed and area of the multiplier is a major design issue. However, area and speed are usually conflicting constraints so that improving speed results mostly in larger areas..Hence in this paper we try to determine the best solution to this problem by using reversible logic gates. reversible logic has emerged as a promising technology having its applications in low power CMOS, Reversible logic circuits have theoretically zero internal power dissipation because they do not lose information, the classical set of gates such as AND, OR, and EXOR are not reversible. The most significant aspect of the reversible gates used in this paper , are that it can work singly as a reversible full adder, that is reversible full adder can now be implemented with a single gate only.General multiplier is based on two concepts. The partial products can be generated in parallel and thereafter the addition can be reduced by using reversible parallel adder.The entire power analysis can be done using HSPICE tool,and hence by the comparions done we can conclude that the proposed system can reduce the power consumption . Furthermore, it has been demonstrated that the proposed design of reversible multiplier circuit using modified full adder,needs fewer garbage outputs and constant inputs. The multipliers can be generalized for NxN bit multiplication. Thus, this job will be of significant value as the technologies mature.

Keywords: Reversible logic gates, Reversible logic circuit, Adders, multipliers, power analysis, simulation outpus

I. INTRODUCTION

One of the major goals in VLSI circuit design is reduction of power dissipation and to improve system performance. Multiplication algorithms have considerable effect on processors performance. As demonstrated by R.Landauer in the early 1960s, irreversible hardware computation, regardless of its realization technique, results in energy dissipation due to the information loss [1]. It is proved that the loss of each one bit of information dissipates at least KTln2 joules of energy (heat), where K=1.3806505x10-23m2kg-2K-1 (joules Kelvin-1) is the Boltzmann's constant and T is the absolute temperature at which operation is performed.Reversible logic circuits have theoretically zero internal power dissipation because they do not lose information. Hence,. In 1973, Bennett showed that in order to avoid KTln2 joules of energy dissipation in a circuit, it must be built using reversible logic gates [2]. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector

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Such gates or circuits allow there production of the inputs from observed outputs and we can determine the inputs from the outputs [3-5]. A reversible logic circuit should have the following features [5]:

- Use minimum number of reversible gates.
- Use minimum number of garbage outputs.
- Use minimum constant inputs.

The output that is not used for further computations is called garbage output [6]. The input that is added to an nxk function to make it reversible is called constant input [7].
Multiplication is a heavily used arithmetic operation in many computational units. It is necessary for the processors to have high speed multipliers. Multipliers are key components of many high performance systems such as FIR filters, microprocessors, digital signal processors, etc. A system's performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest clement in the system. Furthermore, it is generally the most area consuming.Hence, optimizing the speed and area of the multiplier is a major design issue. However,area and speed are usually conflicting constraints so that improving speed results mostly in larger areas. As a result,a whole spectrum of multipliers with different area-speed constraints have been designed with fully parallel. Here we introduce modified full adder,which is used for instead of reversible parallel adder in 4x4 multiplier to reduce the no. of calculations, no. swithching activities to reduce the power dissipation and hence We show that the proposed reversible multiplier circuit is better than the existing designs in term of number of gates, number of garbage outputs, number of constant inputs and hardware complexity.

II. REVERSIBLE LOGIC

Computers now on the market are faster, smaller and more complex than their predecessors. However, the price paid for this speed and complexity is increased power consumption. The primary reasons for the rise in power consumption are the increase in clock frequency and the increased number of transistors packed onto a chip. In any digital computer, an array of0s and 1s represents a number. Every operation in a computer corresponds to the manipulation of the bits, e.g., flip-ping of 0 to 1 or 1 to 0. Internally, computers consist of millions of gate that perform logic operations. In most cases, these logic operations are so called irreversible. That is, some information about the inputs is erased every time a logic operation (function) is per-formed. Thus, we cannot deduce the inputs from just knowing the outputs alone.
If we assume that every transistor out of the 40 million transistors in a processor

(e.g., Pentium IV) dissipates heat at a rate equal to its processor frequency (e.g., 1 GHz), then its power consumption will be approximately4×1016×KT ln2 = 0.05 Watt. (Note: This assumes that the processor works at the temperature of 300 K.) This rate at which heat is generated is still small. However, according to Moore's law, the speed, the complexity and, hence, the heat dissipation—due to the information loss—will increase exponentially. If this current trend continues, there will be an intolerable amount of heat generated by computer systems not so far down the road. Definitely, we should be looking for revolutionary technologies that permit extremely low power consumption and heat dissipation in computing.

Combining reversible logic gates, we can construct reversible circuits that can perform complex logical and arithmetic operations. For a gate to be reversible, the logic function it realizes has to be bijective. That is, there must be a one-to-one mapping between inputs and outputs. By definition, any reversible gate has an "inverse" (also called a "dual"). One can run the logical operations backwards by cascading a reversible logic gate with its dual.

Reversible circuits are also called lossless circuits, as there is neither energy loss nor information loss. These circuits are very attractive for applications where extremely low power consumption, or heat dissipation, is desirable in areas ranging from communications, low power VLSI (Very Large-Scale Integration) technology, optical computing to nanotechnology. Reversible logic has been found to be very useful in quantum computing where the quantum evolution is inherently reversible.

2.1 Reversible Gates

An nxn reversible gate can be represented as:
$I_V = (I1,I2,I3,\ldots,In)$
$O_V = (O1,O2,O3,\ldots,On)$
Where I_V and O_V are input and output vectors respectively. Several reversible logic gates have been proposed in the past years. Between them are: Feynman gate, FG [19], Toffoli gate, TG [20], Fredkin gate, FRG [21], Peres gate, PG [22], New Gate, NG [23], TSG gate, TSG [24].In this section we review these reversible logic gates. Some of them are presented to allow for comparison with existing studies. Feynman gate (FG), is a 2x2 reversible gate that can be described by the equations: P=B and Q=A⊕B, where 'A' is control bit and 'B' is the data bit. It is shown in Fig. 1.

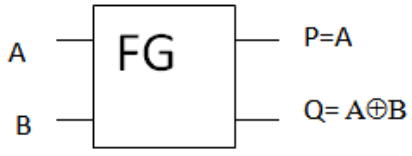

Fig.1 Feynman gate

Toffoli Gate (TG) is a 3*3 two-through reversible gate as shown in Fig.2. The Toffoli gate can be represented as:Iv = (A, B, C) Ov = (P = A, Q = B, R = AB⊕C)Where Iv and Ov are input and output vectors, respectively

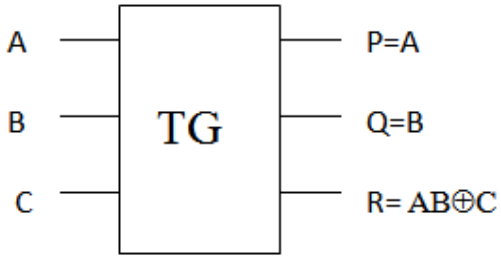

Fig.2 TG gate

Fredkin gate is a (3*3) conservative reversible gate. It can be represented as:
$I_V = (A, B, C)$
$O_V = (P = A, Q = A'B⊕AC, R = A'C⊕AB)$
Where I_V and O_V are input and output vectors. It is shown in Fig. 3. Fredkin Gate is a conservative gate, that is, the Hamming weight of its input vector is the same as the Hamming weight of its output vector.

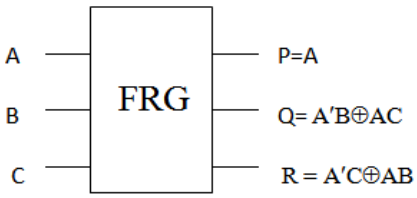

Fig.3 FRG gate

Peres gate is a 3 inputs 3 outputs (3*3) reversible gate , it is also known as New Toffoli Gate (NTG), combining Toffoli Gate and Feynman Gate is a 3x3 reversible logic gate.

It can be represented as:
$I_V = (A, B, C)$
$O_V = (P = A, Q = A⊕B, R = AB⊕C)$
Where Iv and Ov are the input and output vectors.
The Peres gate is shown in Fig. 4. Peres gate is equal with the transformation produced by a Toffoli Gate followed by a Feynman Gate.

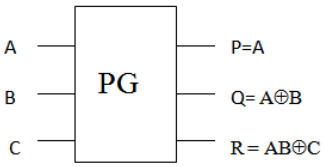

Fig.4 PG gate

TSG gate is a 4x4 reversible logic gate. The gate is shown in Fig. 5,, where each output is annotated with the corresponding logic expression.

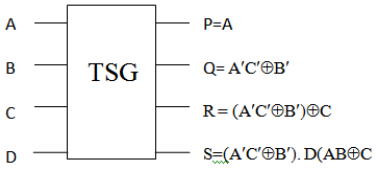

Fig.5 TSG gate

TSG gate is capable of implementing all Boolean functions and can also work singly as a reversible Full adder. Figure 6 shows the implementation of the proposed gate as a reversible Full adder.

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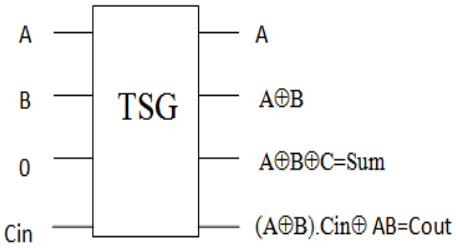

Fig.6 TSG gate as a Full Adder

III. REVERSIBLE MULTIPLIER

In this section we will discuss about the existing reversible multiplier and then we will propose the new one. After that, we will prove some properties of the proposed multiplier and then make a comparative study between the existing and the proposed one.

3.1 Existing Reversible Multiplier

It is based on two concepts. The partial products can be generated in parallel with a delay of d using Fredkin gates and thereafter the addition can be reduced to log2N steps by using reversible parallel adder designed from TSG gates. Each two adjacent partial products will be added together with an N-bit reversible parallel adder. A number of interesting and optimized parallel adders are proposed in [11]. The addition of adjacent partial products will generate the first level of computation with N/2 partial sums. These partial sums are added again in the aforesaid fashion to create a second level of
computation with N/4 partial sums. The final product will be obtained at the log2N level. The working of the multiplier can be deeply understand by considering a binary tree having N leaf nodes (equivalent to N partial sums) which are merged to form their N/2 parents (equivalent to N/2 Partial Sums). These N/2 parents are again added in the aforesaid fashion and finally this process will be successively repeated to the get at the root of the tree(final product). Thus, the required number of levels to compute the multiplication result will be log2N.

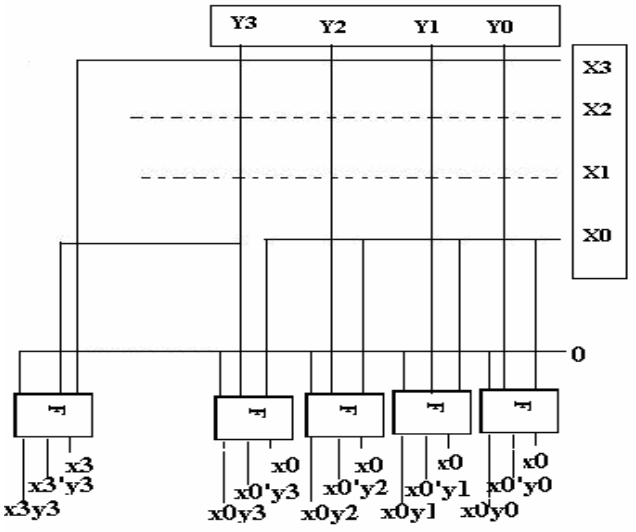

Fig.7 Parallel generation of Partial Product using FRG gates

Since this architecture requires (N-1) of N-bit reversible adders, it needs a total of N *(N-1) reversible full adder cells. So, the worst propagation delay of the proposed multiplier architecture can be computed as: - d+N*d'[log2N] where d and d' are the propagation delays of a Fredkin gate and reversible TSG gate (adder) respectively. By changing the type of adder such as reversible CLA (Carry Look Ahead Adder) to reversible CPA (Carry Propagate Adder) will make a substantial change in the propagation delay. the partial products are generated in parallel using Fredkin gates as shown in Figure 7. Thus, we have 4 partial products generated as shown in Figure 8. Each 2 partial products are added using 4-bit reversible parallel adder creating the first level of computation which has 2 partial sums. These two partial sums are fed to the second level of 4-bit reversible parallel adder,
resulting in the formation of the final product. The proposed reversible multiplier efficiency significantly depends on the type of reversible parallel adders used in addition operation.The existing reversible multiplier is shown in Figure9 for 4x4 bit. The multiplier uses the proposed TSG gates as reversible full adder units.

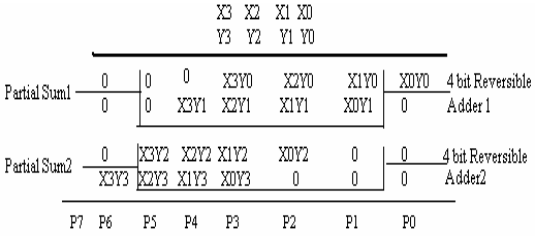

Fig.8 Methodology of 4x4 Reversible Multiplier

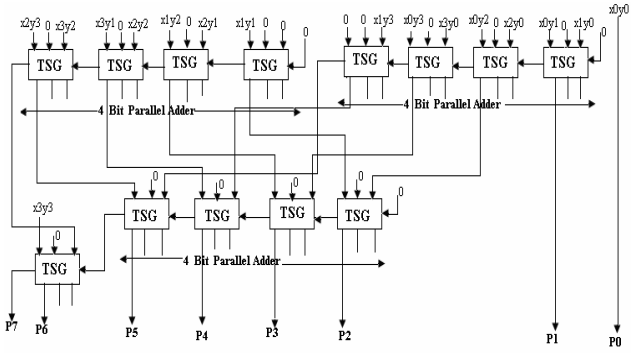

Fig.9 Existing 4x4 Novel Reversible Multiplier

IV. PROPOSED REVERSIBLE MULTIPLIER

The operation of the partial products can be generated in parallel using 16 Peres gates as shown in Fig.8. because of its lower hardware complexity, we use Peres gate instead of other reversible gates. This structure is proposed in [12].

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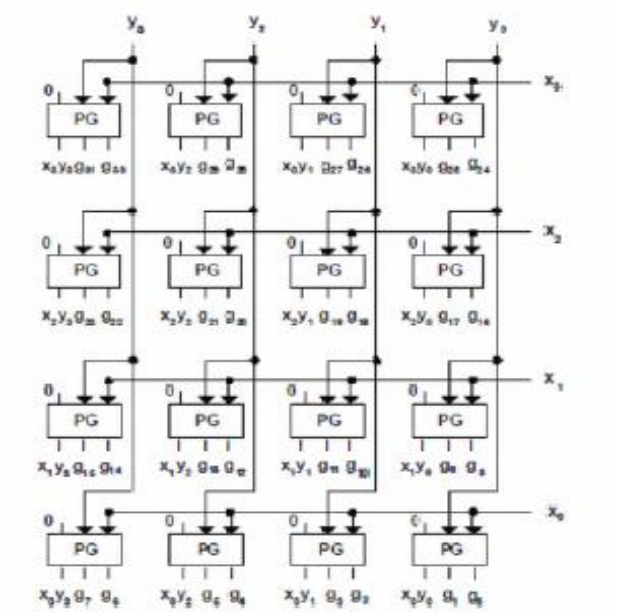

Fig. 8 Reversible partial products generation circuit using Peres gates

The RPA circuit as shown in Fig. 9 needs reversible full adder (FA) and half adder (HA). Many reversible full adders have been proposed in the past. For example, the Maslov circuit, TSG, MKG and HNG gates can singly perform the full adder operation if Iv=(A,B,Cin, 0).

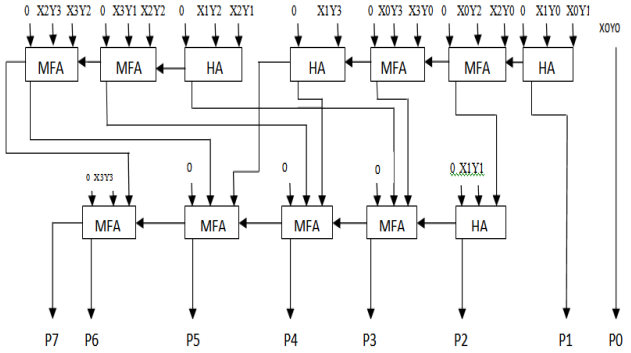

Fig.9 Reversible circuit in which output of PPGC are input of RPA

V. EVALUATION OF PROPOSED MULTIPLIER

The purpose of this paper is the design of reversible multiplier circuits with the aim of optimizing its hardware complexity to make it more economical in terms of number of garbage outputs and constant inputs without losing its efficiency. The garbage outputs identified as the outputs which are not used in further computations and constant inputs need to realize only balanced functions. This is the driving force that makes the proposal of new reversible multiplier circuit uses the modified full adder (MFA) [17] as shown in Fig. 10.

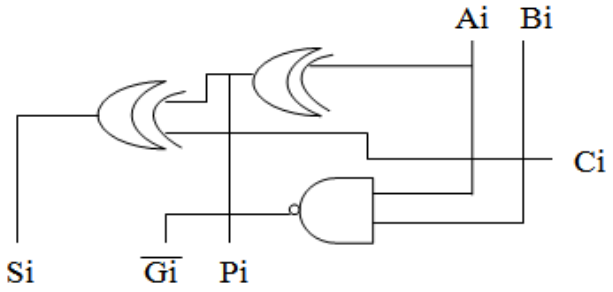

Fig.10 MFA (Modified Full Adder)

We propose the replacement of MFA by conventional reversible parallel adders of reversible multiplier circuit, were proposed in [13-15]. Further, the proposed full adder will be of great help in reducing the garbage outputs and constant inputs parameters. The reason for the fact that proposed reversible multiplier circuits use eight modified full adders (MFA) that they produce zero garbage outputs and zero constant inputs. In addition, it needs four reversible half adders .We use Peres gate as reversible half adder, because it has less hardware complexity [12]. The carry of the next stage in MFA can be expressed as:

$$C_{i+1}=\overline{G_i}\ \overline{P_i\, C_i}$$

NAND gates are used for the faster carry propagation in MFA and help us to keep speed efficiency. Carry genera ion in MFA is depicted in Fig. 11

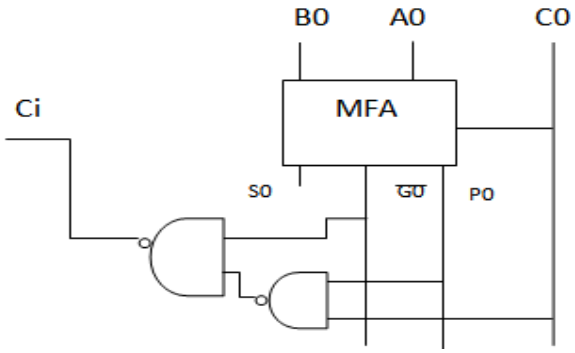

Fig. 11 Carry generation in MFA

It can be clearly realized that the proposed architecture is being tried to design optimal hardware complexity in the reversible 4-bit multiplier. This design generates 36 garbage outputs and 20 constant inputs in reversible multipliers.

Reversible Multiplier	No. of Reversible Gates	No. of Garbage Outputs	No. of Constant inputs	No. of Logical calculations	Power Consumption(nW)
Existing circuit with TSG gates[24]	16FRG+13TSG=29	58	31	110a+103b+71d	5610
Proposed Circuit Using MFA Gates[25]	16PG+12MFA=28	36	20	64a+44b+32d	37.71

Table 6 Comparative Experimental Results of Reversible Multiplier Circuits

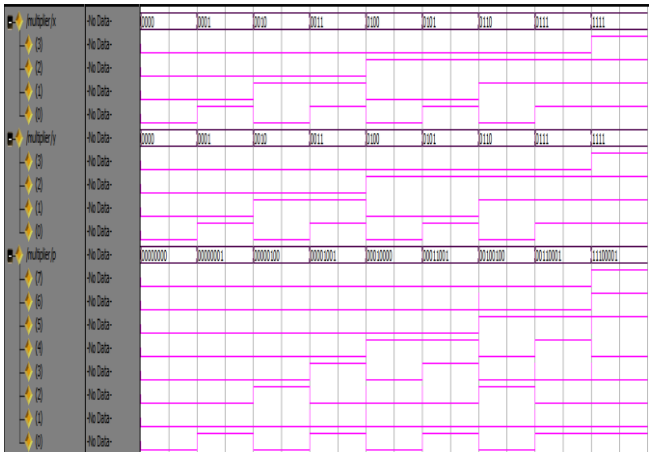

Table 7 Simulation outputs of Multiplier

In order to present a fair comparison, in Table 6, we have shown results of reversible multiplier circuits and our proposed circuit in terms of number of garbage outputs and constant inputs and hardware complexity. In this table,
we define:
a = A two input EXOR gate calculation
b = A two input AND gate calculation
d = A NOT gate calculation
One of the other major constraints in designing a reversible logic circuit is the number of reversible gates. As shown in Table 6, our proposed design approach requires 28 reversible logic gates and it is to be noted that the previous design in [15] also requires 28 reversible gates. In table 7 the simulation outputs can be observed.

VI. CONCLUSION

Multiplier is a basic arithmetic cell in computer arithmetic units. Furthermore, reversible implementation of this unit is necessary for quantum computers. Targeting this purpose, various designs can be found in the literature.
The comparison between the proposed multiplier and those of the previous works showed that the garbage outputs of the MFA design were about 28% and constant inputs were about 30% less than previous works with respect to other counterparts' efficiency.
The prospect for further research includes the reversible implementation of more complex arithmetic circuits such as function evaluation and multiplicative division circuits using the proposed multiplier.

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