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Design Low Power 32-Bit Barrel shifter using Efficient Charge Recovery Logic

Shweta Chawla, Ramanand Harijan, Harpal singh

Abstract— Today power dissipation has become the main concern as the circuit size become larger and larger. Especially in this paper we presented the reduction of the power dissipation which shows an increasing growth as the technology is scaled down. Various theories have been formulated regarding this problem. Out of which Adiabatic Logic is gaining much attention because of its exemplary results. By adiabatic technique, power dissipation in transistors can be minimized as well as energy stored in load capacitance can be reused instead of dissipation as heat. In these circuits we can reduce the energy dissipation during switching process as well as reuse the energy from the load capacitance by making a feedback path from load capacitance to the supply.In this paper we first study of various adiabatic techniques and will lay emphasis on one of its widely used technique called the Efficient Charge Recovery Logic (ECRL). We will study how ECRL technique is better than the rest and how circuits are implemented using it.Using this technology we will design a 32 bit barrel shifter and perform various tests on the circuit. We will also compare the results of this adiabatic technology with the normal CMOS technology and show the drastic reduction in power dissipation. All the design structures based on Adiabatic Switching Logic are designed and simulated using standard TSMC 0.18 µm CMOS technology and 5 V voltage supply at an operating temperature of 27° C. Mentor Graphics Corporation based tool known as IC Design Architect have been used for all the design and analysis.

Keywords- Low power, Adiabatic, ECRL, Fully Adiabatic., Partially Adiabatic Circuit (Quasi),Barrel shifter, Multiplexor

I. INTRODUCTION

Now days the portable electronics has made low power circuit design extremely desirable. All efforts eventually converge on decreasing the power consumption entailed by ever shrinking size of the circuits enabling the portable gadgets. Reducing power supply voltage is a straightforward method to achieve low power consumption. The low power and low voltage CMOS techniques were applied extensively in analog and mixed mode circuits for the compatibility with the present IC technologies. Designing high – performance analog circuits is becoming increasingly challenging with the persistent trend towards reduced supply voltages The desire for portability of electronic equipment generated a need for low power systems in battery operated products like hearing aids, implantable cardiac pacemakers, cell phones, and hand held multimedia terminals. Low power dissipation is attractive, and perhaps even essential in these applications to have reasonable battery life and weight. The ultimate goal in design is close to having battery- less systems, because the battery contributes greatly to volume and weight. [1],[3], [4],[9]. The low-power requirements of present electronic systems have challenged the scientific research towards the study of technological, architectural and circuital solutions that allow a reduction of the energy dissipated by an electronic circuit. One of the main causes of energy dissipation in CMOS circuits is due to the charging and discharging of the node capacitances of the circuits, present both as a load and as parasitic. Such part of the total power dissipated by a circuit is called dynamic power. In order to reduce the dynamic power, an alternative approach to the traditional techniques of power consumption reduction, named adiabatic switching [1][2], has been proposed. In such approach, the process of charging and discharging the node capacitances is carried out in a way so that a small amount of energy is wasted and a recovery of the energy stored on the capacitors is achieved.

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II. ADIABATIC

The term “adiabatic” describes a thermodynamic process in which there is no energy exchange with the environment, and therefore no dissipation of energy or power occurs. But in VLSI, as the transfer of the electric charge takes place between the nodes of a circuit, various techniques can be applied to minimize this energy loss during this charge transfer process. [2]Adiabatic technology is basically used to reduce the energy or power dissipation during the switching process and further reuse some of the energy by recycling it from the load capacitance. For recycling, the adiabatic circuits use the constant current source power supply and for reduce dissipation it uses the trapezoidal or sinusoidal power supply voltage. Adiabatic logic works on the principal of reversible logics. Reversible logic means when a system erases a bit of information, it dissipates heat and today’s computers erase a bit of information every time they perform a logic operation. These are called irreversible logics. And in contrast to it, the logic operations that do not erase information these are called reversible logics. Today most research has focused on building adiabatic logic out of CMOS. However, current CMOS technology, though fairly energy efficient compared to similar technologies, dissipate energy as heat, mostly when switching. To reduce this there are two fundamental rules:-

1. Never turn on a transistor when there is voltage difference between drain and source.
2. Never turn off a transistor that has current flowing through it [2].

logic and the energy flows through the transistor in a controlled manner. As the second rule states that the transistor must not be turned off when there is current flowing through it, reason behind this is that the transistors are not perfect switches.

The change from one state to another is directly proportional to the speed at which the gate voltage changes.[2]

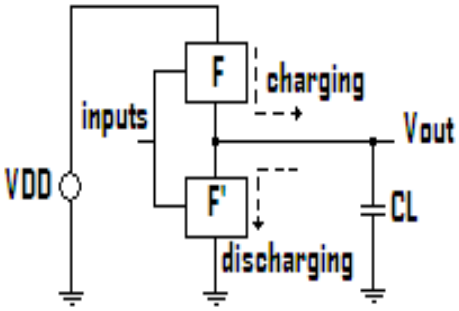

Figure 1 Charging and Discharging in CMOS System

Figure 1 shows the Charging and Discharging in CMOS System. In a CMOS inverter circuit during the negative half of the supply voltage the load capacitance gets charged through the functional block F (PMOS), in the above figure1. There is some energy required to store this energy. Now 50% of this energy is dissipated as heat in the PMOS, hence the capacitance is charged by only 50% of the power supplied. Now during the positive half of the supply voltage the PMOS is switched off and the functional block FBAR(NMOS) is switched on because of which the energy stored in the load capacitance is moved to the ground, and hence it represents the worst case of energy wastefulness[3].

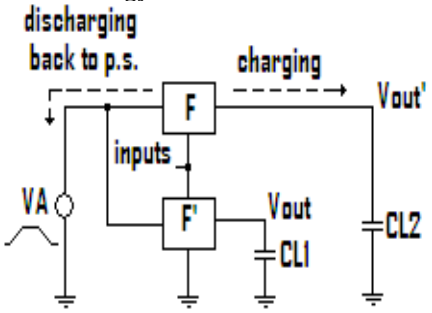

Figure 2 Charging and Discharging in Adiabatic system

Figure 2 shows the Charging and Discharging in Adiabatic System. In figure F functional block use PMOS transistor and FBar use NMOS transistor. Ease of Use

A. Types of Adiabatic Technique

In literature, today various kinds of adiabatic circuits proposed [1] all of them can be grouped into two fundamental classes:

1. Fully Adiabatic Circuit
2. Partially energy recovery Adiabatic Circuit (Quasi)

There are various techniques in both the types of adiabatic technologies. We will study about each technology and find out the boons and banes of each one.

Table I. Comparison between Fully adiabatic and partially adiabatic

Fully Adiabatic	Partially energy adiabatic
All charge on the load capacitance is recovered by the power supply.	Some charge is allowed to be transferred to the ground
More complex architecture	Simpler architecture.
Lose energy due to leakage current through non ideal switches	Energy loss is directly proportional to the capacitance driven and square of threshold voltage
Related techniques:- 1. Pass transistor adiabatic 2. logic(PAL) 3. split rail charge recovery 4. logic(SCRL) 5. Two level Adiabatic Logic (2LAL)	Related techniques:- 1. Efficient Charge Recovery Logic(ECRL) 2. 2N2N2P Adiabatic Logic 3. Positive feedback Adiabatic logic 4. NMOS Energy Recovery Logic(NERL) 5. Clocked Adiabatic Logic(CAL) 6. Time Single phase Adiabatic Logic (TSEL) Source Coupled Adiabatic Logic (SCAL

III. EFFICIENT CHARGE RECOVERY LOGIC

Figure 3 shows the Efficient Charge Recovery Logic (ECRL) and was proposed by Moon and Jeong. It uses two cross-coupled PMOS transistors and two NMOS transistors in the N- functional blocks for the ECRL adiabatic logic block.

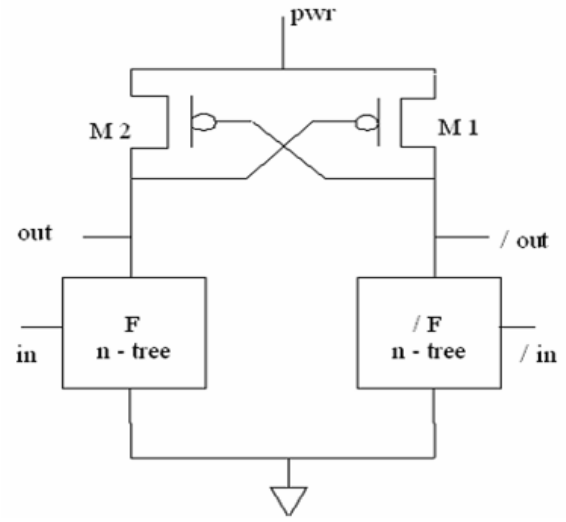

Figure 3. ECRL Logic Circuit

In above figure pwr is the AC power supply is used for ECRL gates, so as to recover and reuse the supplied energy. Both out and /out are generated so that the power clock generator can always drive a constant load capacitance independent of the input signal. Full output swing is obtained because of the cross-coupled PMOS transistors in both precharge and recover phases. But due to the threshold voltage of the PMOS transistors, the circuits suffer from the non-adiabatic loss both in the precharge and recover phases. That is, to say, ECRL always pumps charge on the output with a full swing. However, as the voltage on the supply clock approaches to |Vtp|, the PMOS transistor gets turned off.[6]The ECRL circuits are operated in a pipelining style with the four-phase supply clocks. When the output is directly connected to the input of the next stage (which is a combinational logic), only one phase is enough for a logic value to propagate. However, when the output of a gate is fed back to the input, the supply clocks should be in phase. A latch is one of the simplest cases which have a feedback path. The input signals propagate to the next stage in a single phase, and the input values are stored in four phases (1-clock) safely.

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A. Working

Let us assume in is at high and inb is at low. At the beginning of a cycle, when the supply clock 'pwr' rises from zero to VDD , out remains at a ground level, because in turns on F- tree (NMOS logic tree). /out follows pwr through M1. When pwr reaches VDD, the outputs hold valid logic levels. These values are maintained during the hold phase and used as inputs for the evaluation of the next stage. After the hold phase, pwr falls down to a ground level, /out node returns its energy to pwr so that the delivered charge is recovered. Thus, the clock pwr acts as both a clock and power supply. For instance if we consider a circuit of a two input(x, y) AND gate with output(y).

output , $y = x.y$ (1)

And, $\bar{y} = \overline{x.y} = \bar{x} + \bar{y}$ (2)

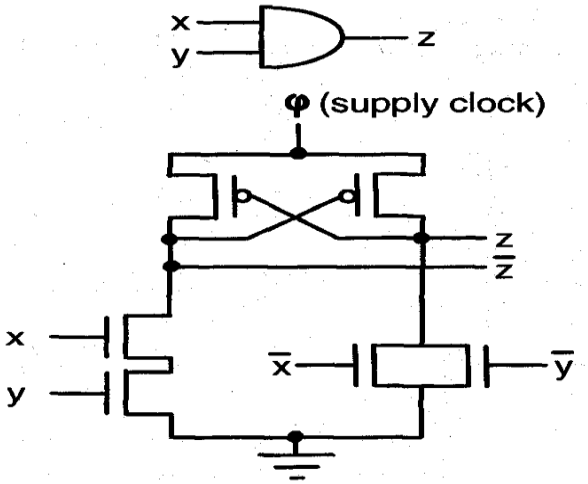

Figure 4. ECRL and gate circuit

So by substituting the value of y and $\bar{y}$ at the positions of F and F/ n tree positions in the Fig. 1 respectively we get the AND circuit implementation using ECRL technology. [5]Similarly in the 4*1 Multiplexer having inputs(D0,D1,D2 and D3) along with select lines(S1 and S2), we get the output Y, Where

$$y = D_0\bar{S_1}\bar{S_2} + D_1\bar{S_1}S_2 + D_3S_1\bar{S_2} + D_3S_1S_2 \quad (3)$$

$$\bar{y} = \overline{D_0\bar{S_1}\bar{S_2} + D_1\bar{S_1}S_2 + D_3S_1\bar{S_2} + D_3S_1S_2} \quad (4)$$

$$\bar{y} = (\overline{D_0} + S_1 + S_2)(\overline{D_1} + S_1 + \bar{S_2})(\overline{D_2} + \bar{S_1} + S_2)(\overline{D_3} + \bar{S_1} + \bar{S_2}) \quad (5)$$

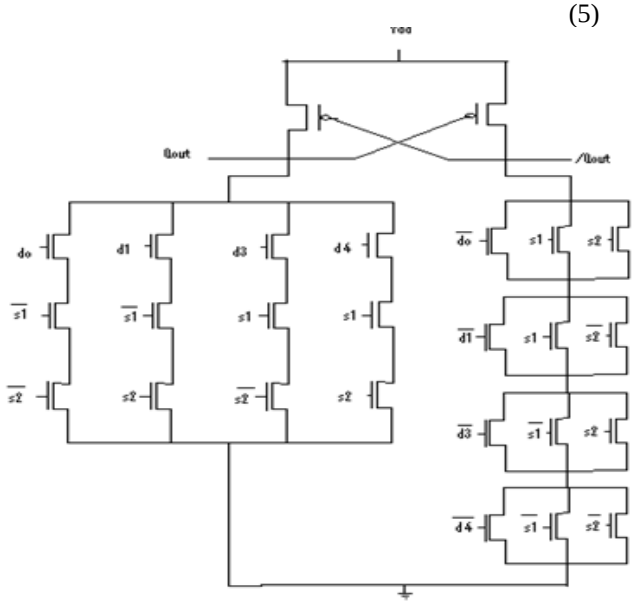

Figure5. ECRL multiplexer circuit

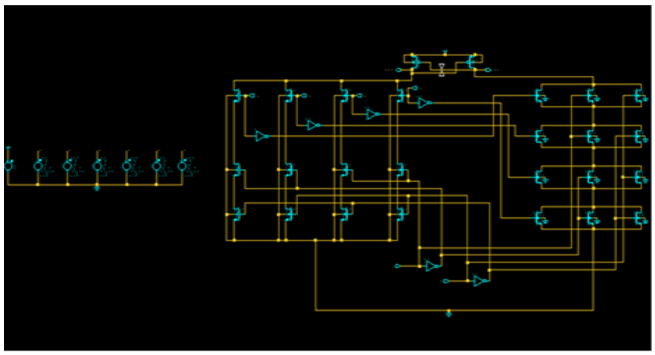

Figure 6. Implementation Schematic 4.1 multiplexer using ECRL technology

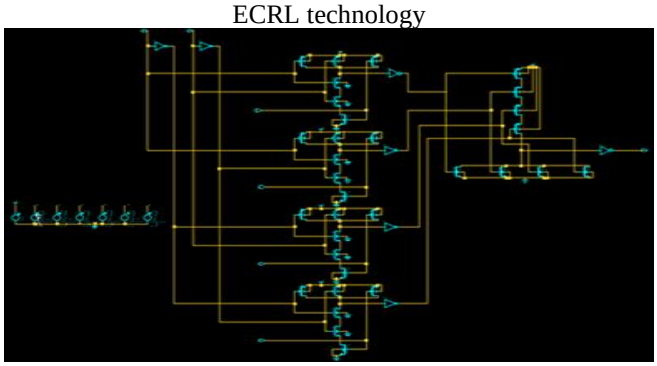

Figure 7. Implementation schematic 4.1 multiplexer using CMOS technology

IV. 32 BIT BARREL SHIFTER

A barrel shifter may be defined as a digital circuit that shifts a data word by a specified number of bits in one clock cycle. It is a bit-rotating shift register. The bits shifted out the MSB end of the register are shifted back into the LSB end of the register. In a barrel shifter, the bits are shifted the desired number of bit positions in a single clock cycle. For example, an eight-bit barrel shifter could shift the data by three positions in a single clock cycle. If the original data was 11110000, one clock cycle later the result will be 10000111.Functionally, since any bit can end up in any bit position, multiplexers are used to place the bits correctly for proper storage. Thus, a barrel shifter is implemented by feeding an N-bit data word into N, N-bit-wide multiplexers. An eight-bit barrel shifter is built out of eight flip-flops and eight 8-to-1 multiplexers; a 32-bit barrel shifter requires 32 registers and thirty-two, 32-to-1 multiplexers, and so on. Working of a barrel shifter can be explained with the help of a 4 bit barrel shifter. A four bit barrel shifter may require four, input multiplexer shown in figure 8 below.

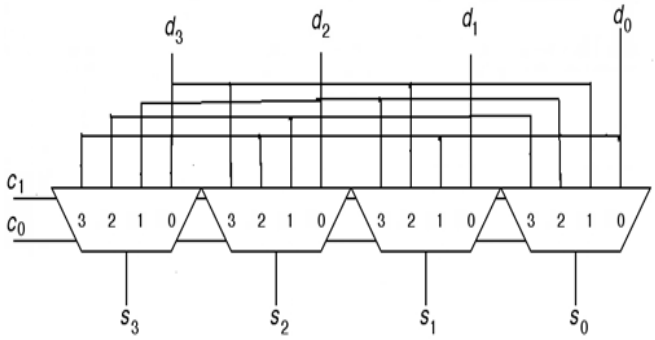

Figure 8. 4-bit barrel shifter circuit

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The above figure shows the block diagram of a shift rotate barrel shifter. The bits enter the barrel shifter through the four inputs(d0,d1,d2,d3) , and the rotated output is received at (s0,s1,s2,s3). The amount of rotation depends upon the select lines of the multiplexer (c0, c1).The inputs are received only on the least significant bit of the multiplexer and rest of the pins are all interconnected. Which can be further explained with the help of a truth Table II the rotation always takes place with respect to the input pattern, i.e W3,W2,W1,W0, and the amount of rotation depends upon the binary equivalent of the inputs at the select lines.

Table II. Truth table of Barrel shifter

C0	C1	S3	S2	S1	S0
0	0	W3	W2	W1	W0
0	1	W0	W3	W2	W1
1	0	W1	W0	W3	W2
1	1	W2	W1	W0	W3

As discussed above, for the design of a 32 bit barrel shifter, we require 32 input multiplexers and all the design structures based on Adiabatic Switching Logic are designed. So now I will demonstrate step by step procedure followed for the design of 32 bit barrel shifter. First we design two input multiplexor shown in figure below.

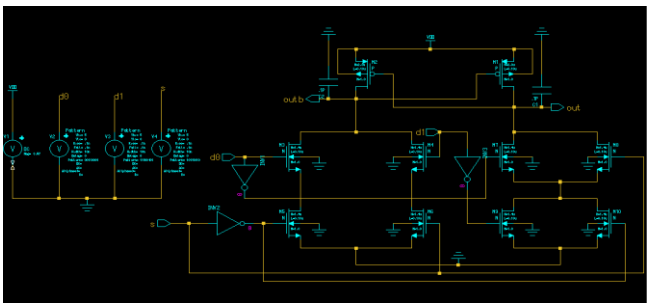

Figure 9 input multiplexor schematic

Figure 10. Input multiplexor symbol

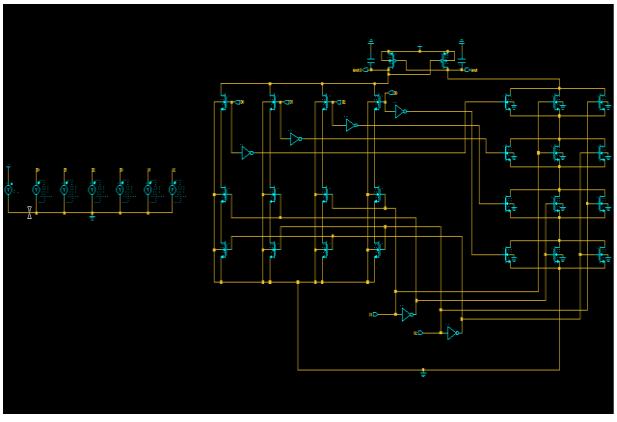

Figure 11. 4 input multiplexor schematic

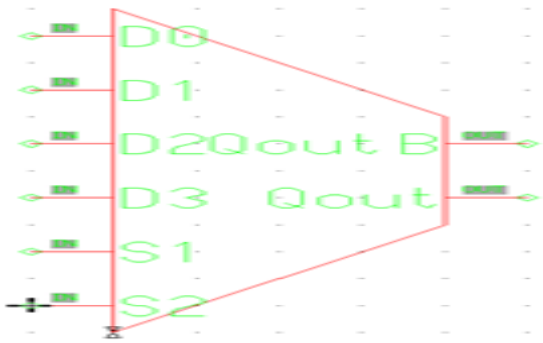

Figure12. Input multiplexor symbol

And second we design the 4-input multiplexer using adiabatic switching shown above figure and then combined both the design 32- input multiplexor and finally we design 32-bit barrel shifter shown figure.

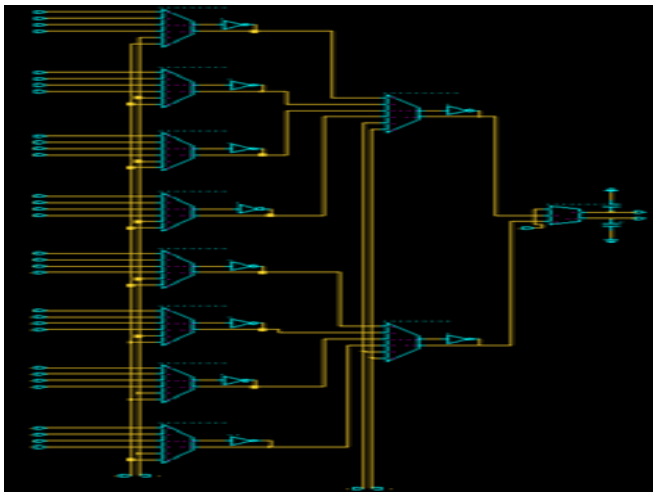

Figure13. 32 input multiplexer Schematic

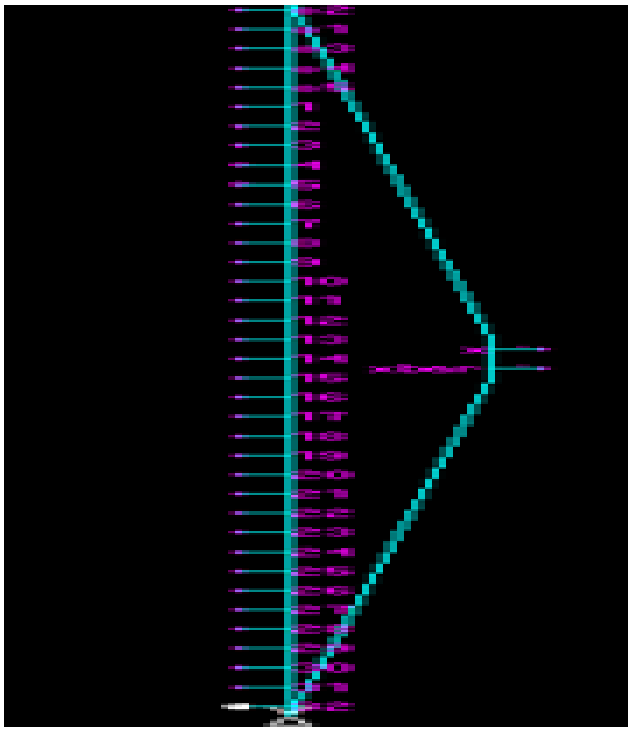

Figure14.32 input multiplexer Symbol

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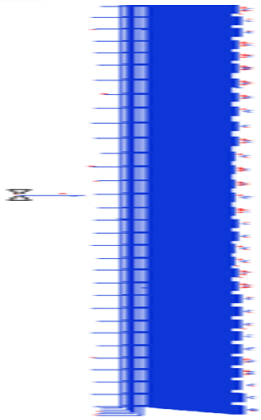

Figure15. 32 Input Barrel shifter using ECRL technology Schematic

V. SIMULATION RESULT

First we design 4:1 multiplexor using ECRL technology and CMOS technology. all the design structures based on Adiabatic Switching Logic are designed and simulated using standard TSMC 0.18 μm CMOS technology and 5 V voltage supply at an operating temperature of 27º C. Mentor Graphics Corporation based tool known as IC Design Architect have been used for all the design and analysis and figure 8 shows the 4:1 multiplexor output wave form and Table II shows the comparison result of ECRL technology and CMOS technology. From the below Table III it is clear that the Power Dissipation is reduced in ECRL technology when compared with the CMOS technology. Number of elements, nodes and input signals are all reduced in this technology. In ECRL there is only two PMOS used, no matter how large the circuit is. But in CMOS technology it uses equal number of PMOS and NMOS. And as we know that PMOS is a greater source of power dissipation hence it is reduced in this technology.

A. Comparison Result of ECRL and CMOS Technology

Table III is clear that the Power Dissipation is reduced in ECRL technology when compared with the CMOS technology. Number of elements, nodes and input signals are all reduced in this technology. In ECRL there is only two pmos used, no matter how large the circuit is. But in CMOS technology it uses equal number of pmos and nmos. And as we know that pmos is a greater source of power dissipation hence it is reduced in this technology.

Table III. Compression result ECRL and CMOS multiplexer

Basis	ECRL multiplexer	CMOS multiplexer
Memory space allocated (Bytes)	56631296	56635392
Elements	39	46
Nodes	26	30
Input Signals	13	14
Temperature (ºC)	26	27
Total Power Dissipation (Watts)	4.4242N	6.2611N

B. Comparison ECRL and CMOS Technology Barrel Shifter

From the above results it could be formulated that the power dissipation in 32 bit barrel shifter made from ECRL technology has been reduced when compared with the CMOS technology. The results show a drastic reduction in number of nodes and number of elements used. Hence ECRL technology can always be used when power dissipation is the concerning matter.

Table IV. Compression result ECRL and CMOS multiplexer

Basis	ECRL BARREL SHIFTER	CMOS BARREL SHIFTER
Memory space allocated (Bytes)	95240192	96174080
Elements	11014	12998
Nodes	6374	7686
Input Signals	2374	2374
Temperature (ºC)	27	27
Total Power Dissipation(Watts)	379N	1.5169U

C. ECRL Barrel shifter Variation of power dissipation with temperature for 10 test vectors

Table V. Variation of power Dissipation with Temperature

TEMPERATURE	DELAY (Ns)	FREQUENCY (Meg Hz)	POWER DISSIPATION (Watts)
-50	404.68	49.860	49.4188N
-40	402.40	49.888	54.8285N
-20	411.59	49.911	80.4732N
-5	412.92	49.931	124.6314N
0	423.54	49.898	147.0092N
5	421.08	49.937	174.4488N
20	428.10	49.903	296.4472N
40	435.89	49.917	595.8815N
60	438.09	49.896	1.1561U
75	447.18	49.917	1.9104U

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REFERENCES

[1] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low Power CMOS Digital Design," IEEE Journal of Solid-state Circuits, Vol. 27, No. 04, pp. 473-484, April 1999.

[2] J. S. Denker, "A Review of Adiabatic Computing", 1994 IEEE Symposium on Low Power Electronics, pp 94-97, 1994.

[3] T. Indermauer and M. Horowitz, "Evaluation of Charge Recovery Circuits and Adiabatic Switching for Low Power Design," Technical Digest IEEE Symposium Low Power Electronics, San Diego, pp. 102-103, October 2002.

[4] W. C. AthaS, J. G. Koller, L. Svensson, "An Energy- Efficient CMOS Line Driver using Adiabatic Switching" Fourth Great Lakes symposium on VLSI, California, March 2005.

[5] A. Kamer, J. S. Denker, B. Flower, et al., "2N2D-order Adiabatic Computation with 2N-2P and 2N-2N2P Logic Circuits," In Proc. of the International Symposium on Low Power design, Dana Point, pp. 191-196, 1995.

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[6] A. Blotti And R. Saletti, "Ultralow- Power Adiabatic Circuit Semi-Custom Design", IEEE Transaction on VLSI system, vol. 12, no. 11, pp. 1248-1253, November 2004.

[7] Dragan Maksimovic´, G. Vojin, Oklobdžija, and et all, "Clocked CMOS Adiabatic Logic with Integrated Single-Phase Power-Clock Supply," IEEE Transactions on VLSI Systems, Vol. 08, No. 04, pp. 460-463, August 2000.

[8] Y. Moon and D. K. Jeong, "An Efficient Charge Recovery Logic Circuit," IEEE JSSC ,Vol.31, No. 04, pp. 514-522, April 1996.

[9] S.S. Rajput and S.S. Jammuar, "*Low Voltage Analog Circuit Design Techniques*", IEEE Transactions on Circuits and System Magazine, Vol no.-2, pp. 24 -42, 2002.

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