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High Definition Surveillance System Using Motion Detection Method based on FPGA DE-II 70 Board

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Abstract- The low cost High Definition (HD) Surveillance system using Field-programmable Gate Array (FPGA) DE-II 70 Development Education Board is proposed in this paper. The proposed solution can be applied not only to various security systems, but also to environmental surveillance. Firstly, the basic principles of HD CMOS Camera Module & motion detection algorithm are given. The HD CMOS Camera Module is used to capture the surveillance video and send the video data i.e. RAW format data to FPGA DE-II 70 board. The motion detection algorithm is used to minimize the recorded data storing capacity. The Automatic motion detection system which can effectively attract operator attention and trigger recording is therefore the key to successful HD surveillance in dynamic scenes. The proposed methods can be well-suited for HD surveillance architectures, where limited computing power is available near the camera for communication. In the proposed system, HD camera is linked with Altera FPGA platform (DE-II 70 Board) where a motion detection algorithm is implemented and recorded video is stored on SD card. FPGA on an Altera DE-II 70 board was used to develop the custom hardware required to perform the motion detection algorithm. The Altera NIOS II embedded processor system was used to perform all hardware interaction tasks necessary on the DE-II 70 board and the custom hardware was constructed as modules inside the NIOS II system.

Keywords-HD CMOS Camera Module, Motion Detection Algorithm, Surveillance System.

I. INTRODUCTION

Now days, there are different types of surveillance systems used depending on applications. First, Health Surveillance Systems, second Security Surveillance Systems and third Weather Surveillance Systems. Proposed system is the types of security surveillance system which is used for the security purpose at ATM's centres, Shopping malls, Jewellery shops, authenticated regions, Bank Lockers room, traffic surveillance etc [4]. The Surveillance video applications have wide scope in many security setups [19]. Many techniques were developed in this area and currently many concepts are under research.

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HD surveillance video requires a huge amount of storage space. Recording everything with surveillance camera is a waste of storage space and also it will be time-consuming for a human to review the stored video. All these disadvantages limit the effectiveness of HD video surveillance [16]. So these problems can be resolved by having the camera which will record only the important part of the captured video, i.e. when the motion is detected in the video scene [16], [17], [11]. A low-cost intelligent security and monitoring solution using motion detection algorithm is presented in this paper for HD surveillance system. If HD surveillance system is designed using FPGA then it has several advantages over other systems without FPGA's (i.e. low cost, less complexity, easing the impact, low power consumptions etc.).

This system is deals with the real-time monitoring of persistent and transient objects within a specific environment. Therefore in this paper, we analyze the feasibility of optimizing HD video surveillance system with an FPGA. The Surveillance video is capture by the HD camera sensor which is interfaced with FPGA DE-II 70 board. Then the captured video is displayed on a VGA Display. But the video is recorded only when motions are detected & stored on a SD-Card [16], [21].

The main categories of event detection algorithms are motion detection, face recognition and shape recognition. A motion detection algorithm was chosen because it seems to cost less in development time, its complexity is rather simple and more accurate for this project than shape or face recognition algorithms. Moreover, the implementation of this algorithm is just to verify the feasibility of the proposal solution. Also, the algorithm is used to detect any kind of event occurring in the monitored room. Therefore, face recognition and shape recognition are too specific to be used. The main method for motion detection is to make a background subtraction methodology [9], [12].

There are many motion detection and tracking algorithms rely on the process of background subtraction, a technique which detects changes from a model of background scene [1], [17], [10], [12]–[13]. Here we present an algorithm in which motion in video frames can be estimated by calculating the difference in consecutive frames [5]. The algorithm takes as input video sequence in which moving objects are present and outputs a statistical background model describing the static parts of the scene which will vary in accordance with the current captured frame [7]–[9].

Once the background frame is selected after that we can take a difference of current frame with past frame for detecting motion. Our system will start recording of surveillance video by setting some threshold value [5].

A. Design Features

1) CMOS Camera

High-definition video is video of higher resolution than standard. While there is no specific meaning for high-definition, generally any video image with more than 480 horizontal lines (North America) or 570 lines (Europe) is considered as high-definition.

HD CMOS Camera for proposed system must compatible with the FPGA DE-II 70 board. So "TRDB_D5M" HD CMOS Camera we are using for the proposed system. The TRDB_D5M is a 5-Mega Pixel Digital Camera module having following Key Performance Parameters.

TABLE I
KEY PERFORMANCE PARAMETERS [14]

Parameter		Value
Active pixels		2,592H x 1,944V
Pixel size		2.2µm x 2.2µm
Color filter array		RGB Bayer pattern
ADC resolution		12-bit
Maximum data rate/master clock		96 Mp/s at 96 MHz
Frame rate	Full resolution	Programmable up to 15 fps
	VGA (640 x 480)	Programmable up to 70 fps
Supply Voltage	Power	3.3V
	I/O	1.7V～3.1V

The TRDB-D5M requires one clock (XCLKIN), which is nominally 96 MHz by default, this result in pixels being output on the D11:D0 pins at a maximum data rate of 96 Mp/s. The TRDB-D5M pixel array consists of a 2,752-column by 2,004-row matrix of pixels addressed by column and row. The address (column 0, row 0) represents the upper-right corner of the entire array. The array consists of a 2,592-column by 1,944-row active region in the centre representing the default output image, surrounded by a boundary region (also active), surrounded by a border of dark pixels. The boundary region can be used to avoid edge effects when doing color processing to achieve a 2,592 x 1,944 result image, while the optically black column and rows can be used to monitor the black level [14].

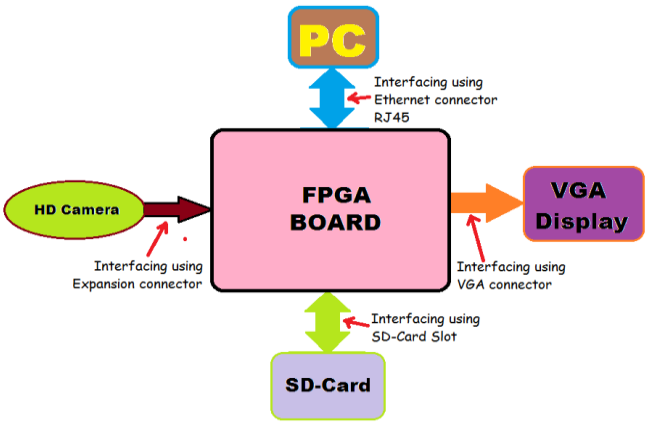
Pixels are output in a Bayer pattern format consisting of four "colors" Green1, Green2, Red, and Blue (G1, G2, R, B) representing three filter colors. When no mirror modes are enabled, the first row output alternates between G1 and R pixels, and the second row output alternates between B and G2 pixels. The Green1 and Green2 pixels have the same color filter, but they are treated as separate colors by the data path and analog signal chain.

To convert a video from a Bayer representation to an RGB format, the two missing color values in each pixel need to be interpolated. Several standard interpolation methods (nearest neighbor, linear, cubic, cubic spline etc.) have been proposed for this purpose. The best performance is achieved by a correlation-adjusted version of the linear interpolation. The linear interpolation has better interpolation accuracy and speed of method.

2) FPGA DE-II 70 Board

This paper deals with an HD camera surveillance system. Figure 1 shows the HD camera is linked with an Altera Field Programmable Gate Array (FPGA) platform on DE-II 70 Board [15] where a motion detection algorithm is implemented.

FIGURE 1
SURVEILLANCE SYSTEM USING FPGA DE-II 70 BOARD



This paper is analyzing the feasibility of optimizing video surveillance with an FPGA. A room is monitored and the video captured by the HD camera is displayed on a VGA screen. The captured video is recorded only when motions are detected & then, the video is stored on a SD-Card. Hardware and software co-design is studied to implement the motion detection algorithm on a NIOS II softcore processor, with hardware acceleration. The main goal of the system to get the full implementation on FPGA is to build a prototype system to monitor a room, to process data captured & to record the useful part of the video.

3) Time Constraint

The time constraint follows two different axes. On the one hand, the image processing part must be fast enough to start the recording as soon as a motion is detected. On the other hand, the storage process must be fast enough to store a picture after another picture without freezing. These two aspects are depends on the platform used and the efficiency of the algorithm. This time constraint is related to the data constraint because the quickness of execution of the image processing depends on the temporary storage of pictures.

4) Data Constraints

For motion to be detected, pictures need to be processed and analyzed. It already underlines two kinds of constraints. The first one is that the system needs a memory with fast access for the process to be in real time. The other constraint is about the type of the data: is it possible to perform the algorithm on the raw data? Or this raw data need to be transformed into a known picture type. After the detection of a movement, when the system starts to record, the video must be stored. It means that the pictures has to be stored quickly enough as they are arriving (less than 0.1s).

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As a consequence: the system must have a memory sized big enough to store a decent amount of video recorded. When a video is recorded, it needs to be available in the FPGA memories (internal or external) for the external users of the system. The success of the motion detection and the storage of the video are dependent on the flow of pictures and their dimensions.

II. HD CMOS CAMERA MODULE

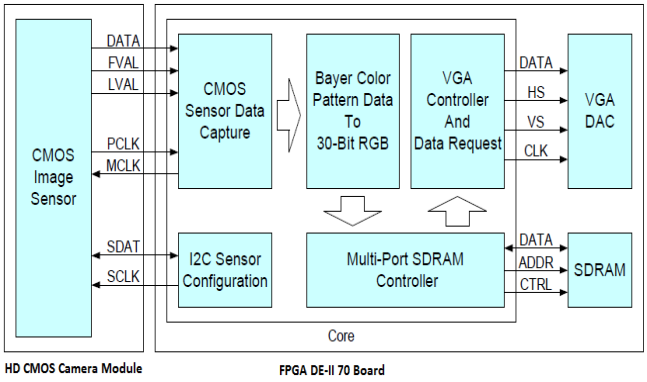
Camera sensor Module is connected to the DE-II 70 Board through General Purpose Input / Output (GPIO) pins [15], which requires a low level access and because, there were already some existing IP-block to use the camera sensor in Verilog.

The Figure 2 shows the Block diagram of interconnection of HD CMOS camera Module and FPGA board. The aim of CMOS sensor data capture block is to get RAW data from the camera sensor and transfer them to the Bayer data (RAW) to RGB block. The aim of Bayer data block is to translate raw data to three colors data Red, Green and Blue (RGB). The second functionality of this block is to calculate the grey value of each pixel, using following equation (2.1).

$$\text{Grey} = \frac{(299 * \text{Red} + 587 * \text{Blue} + 114 * \text{Green})}{1000} \quad (2.1)$$

It is used with integer numbers because it is very expensive to use float numbers in hardware, as it requires more logic elements and therefore bigger area.

FIGURE 2
HD CMOS CAMERA MODULE WITH FPGA BOARD [14]



The purpose of Inter Integrated Circuit Bus (I2C) sensor configuration block is to control and configure the exposure time of the camera sensor. It allows the user, through the switches, to change this time and therefore, to enlighten the image in case it is too dark. This block uses the I2C protocol to communicate the new exposure time of the sensor. I2C is a multi-master serial computer bus that is used to attach low-speed peripherals to a motherboard, embedded system or cell phone.

The main purpose of Multi-port SDRAM controller block is to prepare and format information to be stored on the SDRAM. Therefore, it gets data from the RAW to RGB block and sends them to VGA controller block and SDRAM. The number of the pixel is stored separately, while the color values are stored by splitting the green value in two and sharing the memory space for two colors (Red and the five Green least significant bits & Blue and the five Green most significant bits). It is because the SDRAM block has two storage stacks of 16 bits.

III. MOTION DETECTION ALGORITHM

The three major classes of methods for motion detection are background subtraction, temporal differencing, and optical flow [3]. Background subtraction is the most popular motion detection method and consists of the differentiation of moving objects from a maintained and updated background model [1], [7]-[9], [17], [19]. The method of background subtraction is flexible & fast, but the background scene & camera are required to be stationary [20].

A simple motion detection algorithm for fixed camera compares the current image with a reference image and simply counts the number of different pixels [20]. After reference image has shot, the algorithm runs until the detection of the motion. The algorithm requires two images to understand whether there is considerable change that can be considered as a motion in the projected vision or not. To get the frame difference, first subtract the current frame from the reference frame, often called the background image or background model, pixel by pixel [1], [5]–[7]. Then, we sum up the absolute values of the pixel difference to get the Sum Average Difference (SAD) [8]–[9], [13]. As a basic, the background image must be a representation of the scene with no moving objects and must be kept regularly updated so as to adapt to the varying luminance conditions and geometry settings. Therefore the foundation of the algorithm can be summarized by the following equation (3.1):

$$| \text{Frame}_i - \text{Background}_i | > \text{Threshold} \quad (3.1)$$

Where Frame_i is the current frame captured by the video camera, Background_i is the actual background and Threshold is the threshold level differentiating motion pixels from background pixels. Due to camera noise, the SAD between two consecutive frames may be nonzero even if there is no motion. Therefore, we need to set a threshold to filter out camera noise [17]. The threshold therefore also determines the sensitivity of motion detection. Here we will set the threshold to be slightly above the camera noise level [1], [6], [16]. However, the SAD method as described above is not robust to lighting changes. Lighting changes alter the pixel values of the image and thus can result in a very high value of SAD which may be mistaken as motion. We can avoid this problem by using Block-based mean-Reduced SAD (Block-based MR-SAD) [16].

In Block-based MR-SAD, we decompose the image in to small blocks, which hopefully will separate the objects with different reflectivity into different blocks. For each block of frame difference, mean is calculated and then it subtract from the frame difference. We then sum up the absolute values of all pixels to get the SAD. The choice of an appropriate block size is important. For close-up scenes, where a few objects take up a large portion of the whole frame, each having simple reflectivity, a larger block size can provide very good performance. If the scene has objects that are far away, each having different reflectivity, then a smaller block size is desirable. Note, however, if one chooses a block size that is too small, then one may miss some motion that should be detected. In our implementation, we make the block size an adjustable parameter for the user to choose. Future research will involve automatic adaptation of the block size [16].

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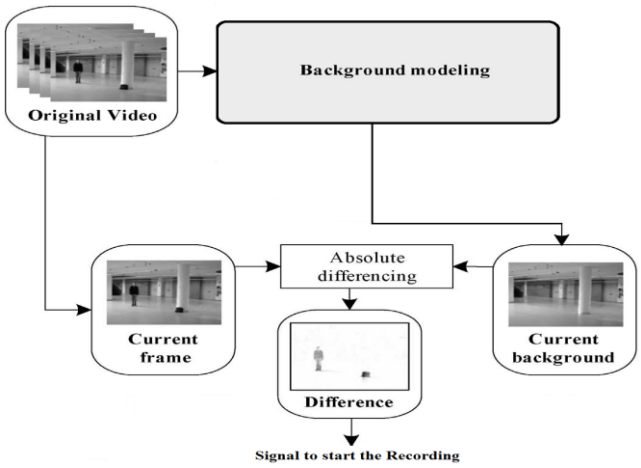
FIGURE 3
MOTION DETECTION ALGORITHM [1]



The algorithm was in c-code for being studied. From this working draft, a NIOS II version of the code was written. Although the aim of studying the algorithm by calculating metrics and profiling it to get an idea of the hardware and software co-design, the algorithm is fully implemented in software. The first reason is that the tool C2H, provided in Altera development software, is very hard to use. The second reason is that, if the code to be accelerated does not fulfill some requirements, there can be no acceleration. The final reason is that the main bottlenecks of the algorithm are memory accesses and this cannot be accelerated, except by adding other memory chips.

IV. SURVEILLANCE SYSTEM

Surveillance is the monitoring of behavior; a surveillance system is a system designed to process and monitors the behavior of people, objects or processes within a given system for conformity to expected or desired norms in trusted systems for security or social control. It can be either secrete or evident. From the beginning of human civilization, there has always been a need for surveillance systems.

The reasons are numerous: borders guarding, raiders, spies and thieves protections. Figure-4 shows the entire system block diagram. The captured video from camera sensor is stored in SDRAM through multi-port SDRAM controller. The aim of multi-port SD-RAM controller is to get an access to the SDRAM of the board. In this, all information for a picture is stored temporarily. It consists of four First in First out (FIFO) stacks to optimize the writing and the reading of data. The aim of VGA Controller & Data request is to display data on a VGA-Screen. Therefore it gets data from the SD-RAM and encodes them for VGA standard. If one wants to display grey scaled picture, the VGA display only needs to get the same value of grey on the three colors. The Switch allows the user to select the color to be displayed: RGB image or Grey-scaled image. The Request signal is sent by the screen to get the information to display. Firstly, synchronization data is sent to prepare the screen. Then, Red, Green and Blue values are sent to the VGA-screen.

The second goal of the project is to record and store a video captured by the camera sensor on SD-Card. In order to access the memory of the board, a convenient solution is to use a softcore processor.

As an Altera DE-II 70 Board is used, a NIOS II processor is used as a softcore processor. So to record captured video, memory is very important, as it storing temporarily a lot of frame captured by the camera. The first problem that appeared is that one frame is around 8 MB:

$$\frac{2592*1944*12}{8} = 7558272\,\text{Bytes} = 7381\,\text{KB} = 7.2\,\text{MB} \quad (4.1)$$

The available temporary memory on the board is 32 MB for the SDRAM, which means no more than 4 images simultaneously. It is quite a problem to capture a video, running 15 frames per second while processing 3 images simultaneously with the processor (the background image, the actual image and the temporary grey-scaled image). It means that the processor needs to access the SD-Card around 3 times per second. The SD-Card controller module of the custom of the NIOS II used in this project has a 3-bits output: one bit for the clock, one bit for the command and one bit for the data. The aim of this project was to implement an intelligent surveillance video camera, using the SD-Card as a tool to store data, not to develop a custom SD-Card driver.

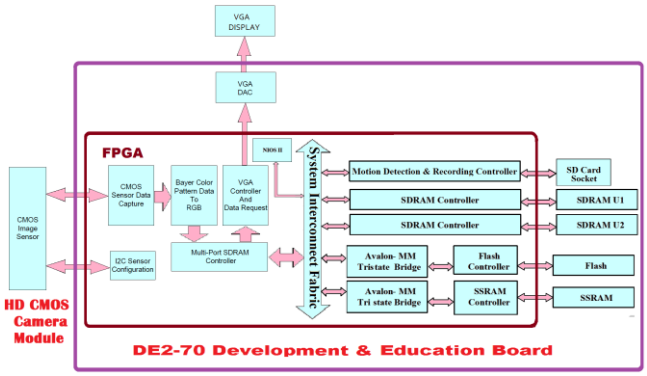


FIGURE 4
HD SURVEILLANCE SYSTEM USING FPGA DE-II 70 BOARD

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As a project was progressing, the need for a softcore processor has become clearer. But this decision to use software is not only due to the disadvantages of programming without softcore processor. As said before using a softcore processor allows to use C/C++ and other object-oriented languages and to work at a higher level of abstraction. On the other hand, it needs another way to think the architecture of the system. Using a softcore processor means using hardware/software co-design methodology.

V. EXPECTED RESULTS

The proposed system can be implemented by using any FPGA board, which has the VGA out, SD card and 40-pin expansion connectors. When the motion is detected then only camera captures or records the video. The recorded video is stored on the SD card. Also the recorded video is sent to the VGA display and video will be display on the VGA screen.

VI. FUTURE WORK

Implement the web-server to allow a user to access data faster than through the JTAG connection. It also enhances the implementation of the SD-Card controller.

Reduce the power consumption of the global system. It can be done either by reducing or optimized the area used by the system on the FPGA , but also by studying the possibility of an ASICs implementation with a fully working prototype on FPGA development platform(including all chips in one ASIC: memories, FPGA etc.).

The storing of video with its audio can be done as a future development.

VII. CONCLUSION

In this paper, we proposed the motion detection algorithm technique for High definition surveillance system using FPGA DE-II 70 development & Educational Board. These techniques reduce the data storage capacity for recorded video. By using Block-Based MR-SAD motion detection technique, we are detecting video motion which will reduce unwanted recording of the surveillance video.

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