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Control of Three-Phase PWM Rectifiers Using a Single DC Current Sensor

M.Prakash, M.S. Jayakumar, S.Ajayan

Abstract-This paper presents a new current control method for three-phase pulse width modulation rectifiers with active power factor correction. Conventional three-phase PFC control requires sensing of at least two input phase currents. Since the input line should be isolated from the control circuitry, current transformer or Hall effects current sensors can be used for sensing the phase currents, these are bulkier and more expensive than resistive current sensors. That type of electromagnetic current sensors are also difficult to integrate with the rest of the control circuitry, it is a major barrier for low-cost integrated PFC control development. The new current control method solves these problems by using only the dc-rail current as the feedback signal .The dc-rail current can be easily sensed by a shunt resistor, and the output signal can be directly used by the control circuitry without isolation .The control method is developed based on a nonlinear average current control principle and avoids the steady-state phase error of conventional linear PI control.

Key words- Current sensing, nonlinear current control, power factor correction, PWM rectifiers.

I. INTRODUCTION

Active power factor correction (PFC) is an effective means for dealing with user equipment harmonic distortion problems. Various current control methods for three-phase PFC converters have been reported. One of the methods is Nonlinear current control methods, such as one-cycle control, can help to overcome the control bandwidth limitation of linear feedback control and have been generalized to three-phase PFC converters using dual-phase control feedback control and have been generalized to three-phase PFC converters using dual-phase control of dual-phase current control is the harmonic distortion around the sector transition points of the input voltages where the inputs to the current combensator become discontinuous. This is fortunately not a problem for one-cycle control because of its small integration time constant and the periodic reset of the integrator.

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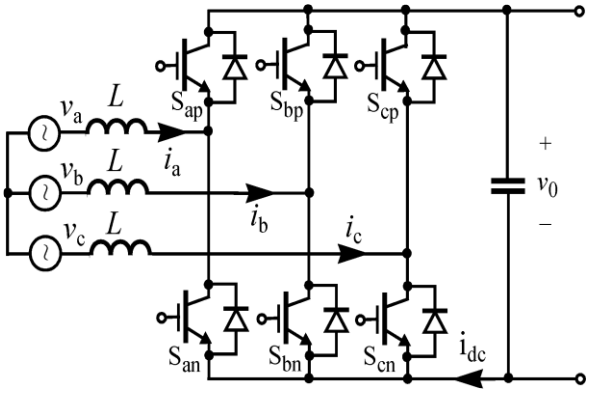

Fig.1.Three phase rectifier with dc-rail current sensor

On the other hand, one-cycle control as reported in the literature regulates the peak of the input current, hence it may suffer from high-input current harmonic distortion under light load conditions, or in general when the current ripple is large.

Almost all existing three-phase PFC control methods require sensing of the input currents, which typically requires three current sensing transformers. Such sensing transformers not only increase the size but also complicate the design of the control circuits. This paper presents a new current control method for three phase PFC converters that directly uses the dc-rail current measurement as feedback for input current control. It provides an effective PFC control method for low-cost applications by avoiding the use of bulky phase current sensors. In The circuit diagram with three phase rectifier with dc-rail current sensor shown in the fig.1

This paper presents a new current control method for three phase PFC converters that directly uses the dc-rail current measurement as feedback for input current control. It provides an effective PFC control method for low-cost applications by avoiding the use of bulky phase current sensors or complicated current estimation algorithms. The remaining of the paper is organized as follows: Section I present detail about the nonlinear averaged current control method for single-phase PFC from which the proposed new control method is developed. Section II presents details of the new phase dual phase current control method. Section III presents details of the overall control design. Section IV presents details of the implementation using an FPGA Section Vpresents details of the PWM signal distribution and how the PWM signal convert in to gate signal how this switch the three phase rectifier section VI followed by the summary.

II. NONLINEAR AVERAGE CURRENT CONTROL OF SINGLE-PHASE PFC

A nonlinear average current control method for boost single phase PFC converters was introduced in Unlike other nonlinear current control methods, the method controls the true average of the input current The control method combines input current feed forward with partial feedback based on the switch current to achieve sinusoidal input current and unity input power factor. It overcomes the limitations of the conventional linear average current control in terms of control bandwidth and sensitivity to noise.For the boost single-phase PFC converter, the principle of nonlinear average current control method can be described by the following equation, where ge is a constant generated by output voltage controller and ge|vin| and is defined as represents the reference for the PFC converter input current iref: The variable dffis the so-called feedforward duty ratio signal

$$dff = 1 - \frac{vin}{v0}$$

The control method can be implemented by using the circuit depicted where is is the sensed switch current while α ge|vin| and (1+α) ge[vin] dff are reference signals generated by another control circuit. Stability and control performance ofthe method are affected by the selection of the parameter α, anduse of the following α is recommended

$$\alpha = \frac{dff}{1 - dff}$$

the switch current is used as feedback in this method (while the true average of the inputcurrent is controlled.) dual-boost single-phase PFC converters by reformulating the control algorithm to work with the diode instead ofthe switch current, that avoids the complexity associated with sensing two switch currents in the dual-boost topology. Because the current of the conducting diode in a dual-boost converter isequal to the dc-rail current, it can be easily sensed by a seriesor shunt resistor placed on the dc return rail, greatly simplifyingthe current sensing circuit design. This method is generalized inthe following sections to three-phase boost PFC converters by combining by dual phase control method

III. DUAL-PHASE CURRENT CONTROL TECHNIQUES.

Dual-phase control of three-phase converters operates the switches in only two phases at a time, while the third phase is not switched. The effect is similar to "flat-top" modulation in which the switching loss of the converter is reduced by 1/3. The method works by dividing a line cycle into six sectors each spanning over a 60◦ interval, as defined in Fig. 2. In each sector, the two phases that have the smallest voltages (hence smallest currents under the assumption of unity power factor operation) are controlled; the third phase current is uncontrolled and flows to or from the dc link through the high- or the lower side diode depending on the sector of operation. For easy reference, the six sectors are referred to as Sectors I through VI Fig. 3 shows the equivalent circuit of a three-phase PFC converter working in Sector I, in which phase a and c are controlled.Only the lower side switches San and Scn are shown because, due to the direction of ia and ic, the high-side switches in these two phases do not conduct current even when they are turned on; instead, the currents flow through their antiparallel diodes, which are shown on the top in Fig. 3. Phase b is uncontrolled in this sector. The lower side switch Sbn can be left on, but because of its polarity, the current ib flows through the

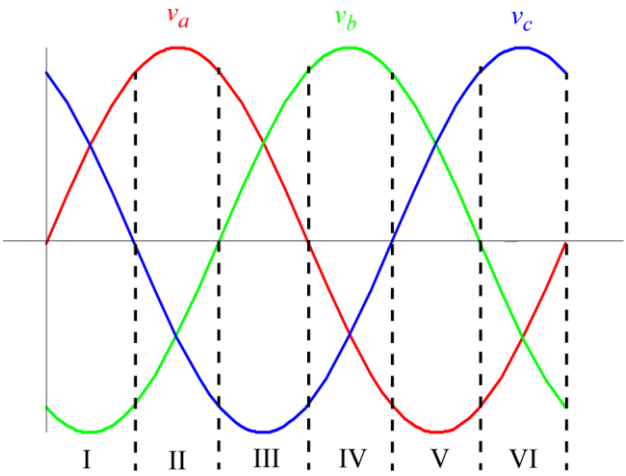

Fig.2.Division of a line cycle into six sectors.

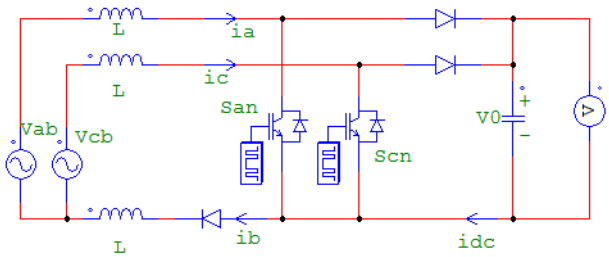

Fig.3. Operation of I sector

Shown for phase b. One-cycle control of three-phase PFC converters is also based on this dual-phase control technique Note that each of the controlled phase currents (ia and ic) is part of the dc rail current idc, whenever the corresponding lower side switch (San and Scn) is off. With different combinations of the switch conduction states, the relationship between idc and the phase currents in Sector I can be summarized by Table I,where "0" indicates OFF state of a switch and "1" indicates the switch is on.

TABLE I Dc-Rail Current Relationship To The Input Currents

S_{an}	S_{cn}	i_{dc}
0	0	i_a+i_c
1	0	i_c
0	1	i_a
1	1	0

Note that the two switches of each phase are usually controlled by complementary gate signals such that the high-side switch is off when the lower side switch is on, and vice versa.Similar relationship can also be identified for other sectors. The phase currents that are to be controlled, which provides the foundation for the proposed control method.

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a. Phase Current Control Based on DC-Rail Current

Consider again the operation in Sector I. Unity power factor operation requires that the average of each input current follows a reference that is proportional to the corresponding phase voltage Denoting the duty ratio of the three upper switches (Sap, Sbp, and Scp) by da, db , and dc respectively, and assuming that da < dc, we have assume that a switching cycle starts with the high-side switches Sap and Scp of phase a and c being turned on depicts the responses of currents ia, ic and idc over a switching cycle in Sector I and when da < dc , which usually is the case when the converter operates in the first half of Sector I where phase c voltage (hence also current) is higher than that of phase a, as shown in the figure. Because idc = ia+ icin interval [0, daTS] and idc = icin interval dcTS, that can be rearranged Similar to (1), the earlier two equations define duty ratios da and dc that satisfy current control requirements expressed in other words, they define the necessary conditions for unity power factor operation of the converter in Sector I. An nonlinear current control method can be devised based by replacing the duty ratios on the right-hand sides bythe following feed forward duty ratio signals calculated based on ideal PFC operation of the converter, similar to the way in which is determined for single-phase boost PFC converters requires only the sensing of idc and would work as follows:

1) Turn on the high-side switch of both phase a and c at thebeginning of each switching cycle, and start to integrateidc as indicated
2) When the integrator output becomes equal to the right hand side turn off the high-side switch (and turn onthe lower side switch) of phase a while a second integrator starts to integrate idc
3) Phase c will be switched when the second integrator output becomes equal to the right-hand side Both integrators are reset before the next switching cycle starts. The second integrator can be avoided by reforming as will be discussed later in the paper.

TABLE II Designation Of Phase Voltages In Different Sectors

Sector	I	II	III	IV	V	VI
v_x	v_a	$-v_b$	v_b	$-v_c$	v_c	$-v_a$
v_y	v_c	$-v_c$	v_a	$-v_a$	v_b	$-v_b$

Note that phase b is not switched in Sector I. Unfortunately the control as outline earlier is inherently unstable because of the existence of a positive-feedback mechanism in the resulting phase current response, that can be explained as follows: if for some reason idc is smaller than desired, it will take longer time for the integrator output to reach the reference represented by the right hand side Because idc decreases when any of the high-side switches is turned on it will be even smaller at the end of the current switching cycle. That leads to instability of the current control loop. The problem can be resolved by changing the sign of the dc-link current feedback and adding an offset i0 to both sides of the equations With a properly selected i0 , the control based would be stable and would work in the same way as outline earlier, with the integrator input changed from idc to i0 − idc. Similar stabilization technique was used for dual-boost single-phase PFC converters. The resulting control method and its design considerations will be discussed in the next section.

IV. OVERALL CONTROL DESIGN

The basic control principle outlined earlier applies only to Sector I of a line cycle and when the high-side switch of phase c conducts longer than that of phase a. Two integrators that are reset at the beginning of each switching cycle are also needed.Generalization of the control to other sectors and elimination of one integrator to simplify the implementation are discussed in this section along with some general design considerations.First, to eliminate the need for a second integrator, note that the first integrator can continue to operate after its output reaches the right-hand side and the high-side switch of phase a has been turned off. Instead of controlling phase c based on by using a second integrator, can be combined with to give an equivalent condition, which satisfies the control objective represented controller are the triangular signal amplitude and the hysteresis bandwidth.

A. Generalization to Other Sectors

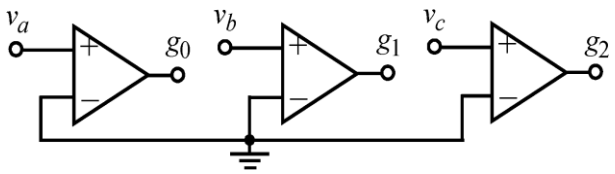

Fig. 3. Generation of three logic signals $g0$,$g1$, and $g2$ used for sector determination.

$$dxff = \frac{1}{v0}[2vx + vy - geL\frac{d(2vx+vy)}{dt}]\text{……..1}$$

$$dyff = \frac{1}{v0}[vx + vy - geL\frac{d(vx+2vy)}{dt}]\text{……2}$$

To generalize the control to the second half of each sector where $dx > dy$, one simply needs to exchange the subscript x and y in (18) and (19). More specifically, the control equations for the second half of each sector can be written as follows:

$$\frac{1}{Ts}\int_0^{dxTs}(i0 - idc)dt = d_xff(i_0 - g_{ev_{x-}}\, g_{ev_y}) + (d_{xff-}d_{yff})\, g_{ev_y}\text{……3}$$

$$\frac{1}{Ts}\int_0^{dyTs}(i0 - idc)dt = d_yff(i_0 - g_{ev_{x-}}\, g_{ev_y})\text{……..4}$$

Defining dM= max{dx , dy}, dm= min{dx , dy}, dMff = max{dxff, dyff}, dmff = min{dxff, dyff}, and

$$\frac{1}{Ts}\int_0^{dMTs}(i0 - idc)dt = d_Mff(i_0 - g_{ev_{x-}}\, g_{ev_y}) + |d_{xff-}d_{yff}|im\text{……..5}$$

$$\frac{1}{Ts}\int_0^{dmTs}(i0 - idc)dt = d_mff(i_0 - g_{ev_{x-}}\, g_{ev_y})\text{ ….6}$$

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The sector in which the converter operates and the corresponding voltages vx and vy can be determined based on three logic signals g0 ,g1 , and g2 defined in Fig. 3.

B. Offset Signal

The offset *i*0 in (3) and (4) is necessary for stability of the current loop under the proposed control. In general, a positive*i*0 larger than the dc-rail current *i*dc will ensure the positiveness of the integral and stability of the current loop. This offset also affects control performance of the input currents, and a constant *i*0 , although simple to implement, does not yield the best performance because of the changing operation condition over a line cycle. For dual-boost single-phase PFC converter, that an offset proportional to the input voltage can remove variation in the current loop pole and result in significantly improved control performance over a constant *i*0 . The same concept is applied here by selecting

$$i0 = a(vx + vy) \ldots\ldots\ldots\ldots 7$$

To guarantee stability, α must be larger than *ge*. Since *ge* is the output from the voltage loop, which changes with the load,α should be selected based on full load. Although an α close to *ge* improves control speed, it results in diminishing input signal level of the integrator, making the control more sensitive to noise. A proper selection of α needs to consider these effects.

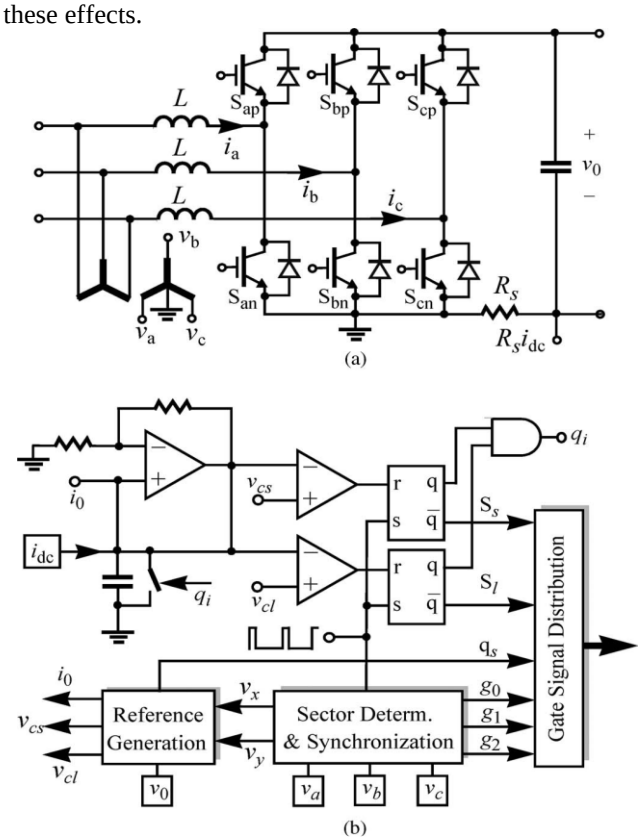


Fig. 4. (a) Power stage and (b) functional blocks of the proposed control fora three-phase boost PFC converter.

V. IMPLEMENTATION USING AN FPGA

Implementation of the control method discussed in Section II and III requires both analog and digital functions. Considering that an FPGA is used to implement the control method. The converter power stage is shown in Fig. 4 along with a block diagram of the control function, which consists of the following major blocks:

1) Sensing circuits (and analog–digital converters) for the three-phase input voltages, the output voltage, and the dc-rail current;
2) logic circuits that determine the sector of operation based on the sensed phase voltages and synchronize the sector transition to the PWM switching clock to minimize current distortion caused by sector transition;
3) digital circuit to generate the offset current i0 for the integrator and non inverting inputs of the two comparators:

$v_{cl} \propto d_M ff(i_0 - g_{ev_x} - g_{ev_y}) + |d_{xff} - d_{yff}| i_m \ldots\ldots..8$

$v_{cs} \propto d_{mff(}(i_0 - g_{ev_x} - g_{ev_y}) \ldots\ldots\ldots\ldots\ldots\ldots\ldots 9$

4) an integrator with reset switch, two comparators, and two R–S latches to generate two PWM signals Ss and Sl; and
5) logic circuits that distribute the PWM signals Ss and Sl to the particular switches in the three-phase switch network based on the sector of operation.

Two additional logic signals are used in the diagram: qi is the combination of the non inverting output of the latches and is used to reset the integrator after both comparator output states have changed; qs indicates which of the two controlled phases (x and y) has a shorter duty ratio and will be switched first. It is defined based on the calculated feedforward duty ratios as follows:

$$q_s = \begin{cases} 0 \ if \ d_{xff} > d_{yff} \\ 1 \ if \ d_{xff} \le d_{yff} \end{cases} \ldots\ldots\ldots\ldots\ldots\ldots 10$$

VI. PWM SIGNAL DISTRIBUTION

The S–R latches in Fig. 4 produce two PWM signals Ss and Sl. The first step to determine gate control signals for the actual switches is to convert these PWM signals into gate control signals for the phases (x and y) that are physically controlled in the sector in which the converter operates. This is accomplished by using the logic signal qs defined earlier;

$$s_x = q_s s_s + \bar{q}_s s_l \ldots\ldots\ldots\ldots\ldots\ldots\ldots 11$$

$$s_y = q_s s_l + \bar{q}_s s_s \ldots\ldots\ldots\ldots\ldots\ldots\ldots 12$$

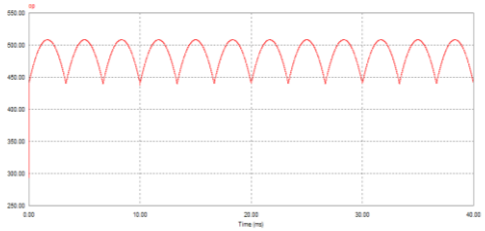
The next step is to direct the resulting gate signals to the appropriate phases (such as phase *a* and *c* in Sector I.) This is accomplished as follows by using the logic signal *g*0 ,*g*1 , and *g*2

$$s_{an} = g1g2 + \bar{g}1g2s_x + g1\bar{g}2s_y \ldots\ldots\ldots 13$$

$$s_{bn} = g0g2 + \bar{g}0g2s_x + g0\bar{g}2s_y \ldots\ldots\ldots\ldots 14$$

$$s_{cn} = g0g1 + \bar{g}0g1s_x + g0\bar{g}1 \ldots\ldots\ldots\ldots 15$$

a.Simulation and result



VII. SUMMARY

The relationship between the three phase currents and the dc-rail current was first identified to show the composition of the dc-rail current in each conduction state of the three-phase switch network. By dividing a line cycle into six sectors and operating two phases in each sector, a simple control circuit consisting of a single integrator and two comparators can be used to develop PWM control signals which drive the phase currents to follow their respective references. Additional logic circuits are used to determine the sector of operation and the switches to which the PWM gate signals are applied.

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