International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-2 Issue-2, December 2012

Design of a 1.5-V, 4-bit Flash ADC using 90nm Technology

Arunkumar. P. Chavan, Rekha. G, P. Narashimaraja

Abstract - In this paper, a 4bit analog to digital converter is designed for low power CMOS. It requires 2^N-1 comparators, an encoder to convert thermometer code to binary code. The design is simulated in cadence environment using spectre simulator under 90nm technology. The pre simulation results for the design shows a low power dissipation of 1.984mW for the designed ADC. The circuit operates with an input frequency of 25MHz and 1.5V supply with a conversion time of 6.182ns.

Keywords – CMOS comparator, Thermometer encoder, Flash ADC, Low-power.

I. INTRODUCTION

An **analog-to-digital converter** (ADC) is a device that converts the input continuous physical quantity to a digital number that represents the quantity's amplitude. The result is a sequence of digital values that have converted a continuous-time and continuous-amplitude analog signal to a discrete-time and discrete-amplitude digital signal. A direct-conversion ADC or flash ADC has a bank of comparators sampling the input signal in parallel, each firing for their decoded voltage range. The comparator bank feeds an encoder logic circuit that generates a code for each voltage range.

II. FLASH CONVERTER

Flash ADCs (sometimes called parallel ADCs) are the fastest type of ADC and use large numbers of comparators. The input signal is applied to all the comparators at once, so the thermometer output is delayed by only one comparator delay from the input, and the encoder N-bit output by only a few gate delays on top of that, so the process is very fast. An N-bit flash ADC consists of 2^N resistors and 2^N–1 comparators arranged as in Figure Fig 1. Each comparator has a reference voltage which is 1 LSB higher than that of the one below it in the chain. For a given input voltage, all the comparators below a certain point will have their input voltage larger than their reference voltage and a “1” logic output, and all the comparators above that point will have a reference voltage larger than the input voltage and a “0” logic output.

Manuscript published on 30 December 2012.
***** Correspondence Author (s)
Arunkumar P Chavan Department of Electronics and Communication, R V College of Engineering, Bangalore 560059, India.
Rekha G, Department of Electronics and Communication, R V College of Engineering, Bangalore 560059, India.
P Narashimaraja, Department of Electronics and Communication, R V College of Engineering, Bangalore 560059, India.

The 2^N–1 comparator outputs therefore behave in a way analogous to a mercury thermometer, and the output code at this point is sometimes called a thermometer code. Since 2^N–1 data outputs are not really practical, they are processed by a decoder to generate an N-bit binary output.

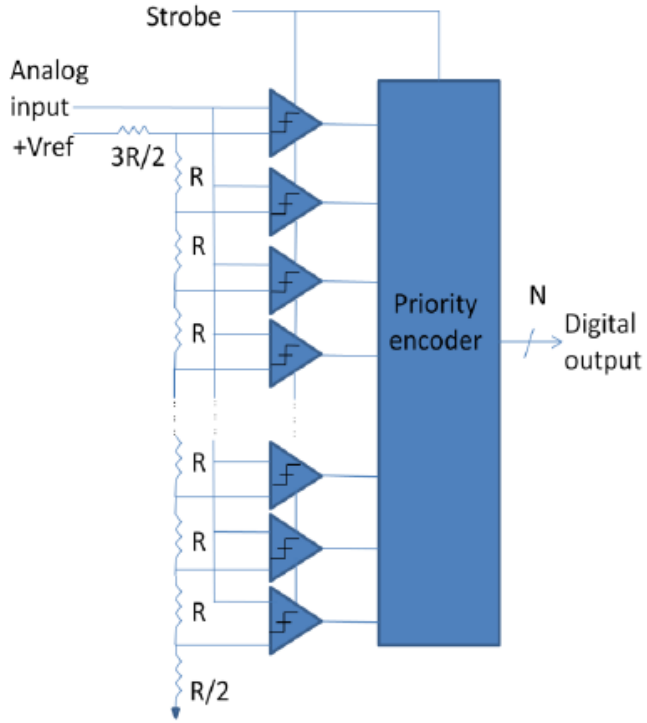

Figure 1: N-Bit Flash ADC

The architecture uses large numbers of resistors and comparators and is limited to low resolutions, and if it is to be fast, each comparator must run at relatively high power levels. Hence, the problems of flash ADCs include limited resolution, high power dissipation because of the large number of high speed comparators and relatively large (and therefore expensive) chip sizes. In addition, the resistance of the reference resistor chain must be kept low to supply adequate bias current to the fast comparators.

A. Comparator

The low power comparator circuit used in the design of Flash ADC is shown in fig 2 which is proposed in [1]. This circuit uses a preamplifier and a latch stage. In the preamplifier stage to achieve an acceptable gain the input differential pair uses NMOS transistors and the load uses PMOS transistors. The latch stage consists of two inverters which are connected in a back to back fashion forming a differential comparator and an NMOS transistor is connected between the two differential nodes of the latch.

The design was implemented in cadence using 180nm technology [1]. In our proposed work simulation results are shown using 90nm technology.

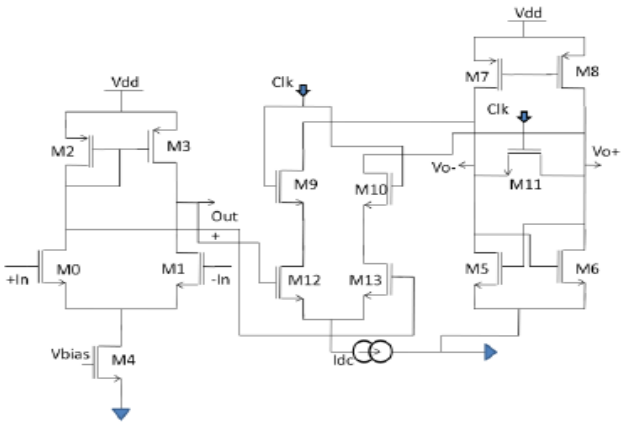

Fig 2: Preamplifier-Latch comparator

The preamplifier stage improves the sensitivity of the comparator and isolates the comparator input from switching noise of the positive feedback stage [3]. The latch stage gives the information about which of the input signals is larger and amplifies the difference between the signals [4].

B. Thermometer to Binary Code Converter

The logic encoder used for 4bit ADC is as shown in fig 3. This is a multiplexer based encoder which converts thermometer codes to binary codes. Table 1 show the truth table for the 4bit encoder. The multiplexers used are designed using transmission gates for better accuracy.

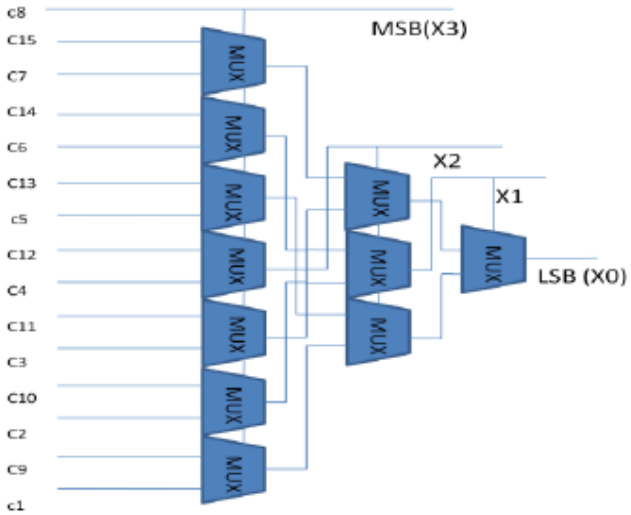

Fig 3: Logic Encoder for 4bit ADC

Table 1: Truth table for 4bit encoder

C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	X3	X2	X1	X0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	1
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	1	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	1
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	0	0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0

III. PRE SIMULATION RESULTS

A. Comparator Output

The schematic of comparator using 90nm technology is shown in fig 4. The input signal applied to the non-inverting terminal is a sine wave and a dc reference voltage is applied to the inverting terminal of the comparator. The resulting waveform at the output of the comparator is as shown in fig 5.

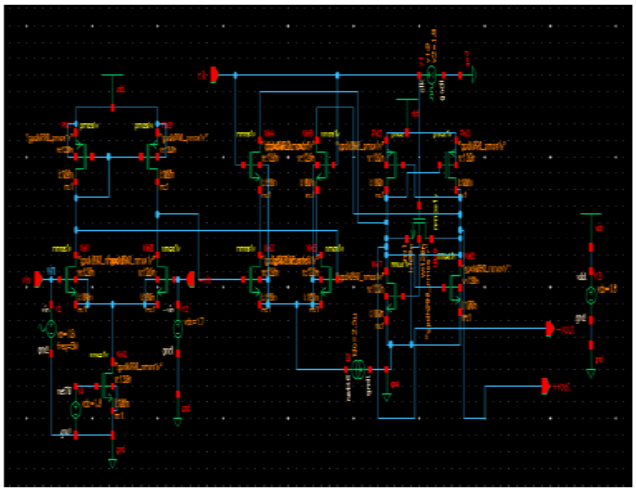

Fig 4: Schematic of comparator

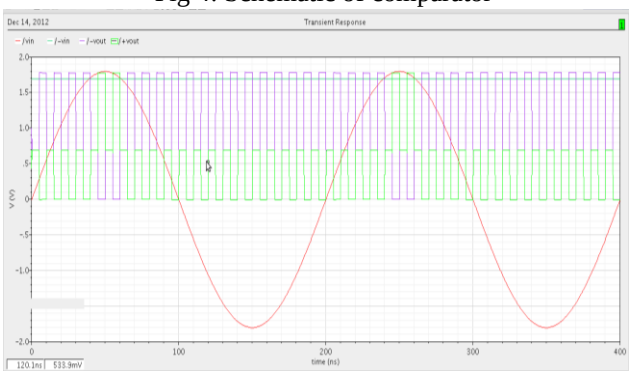

Fig 5: Comparator output waveform

B. Flash ADC Output

The above obtained 2^N-1 comparator outputs are encoded into 4bit output using an encoder and the resulting waveform of the ADC is as shown in fig 7. The schematic view of ADC ia as shown in fig6.

Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)

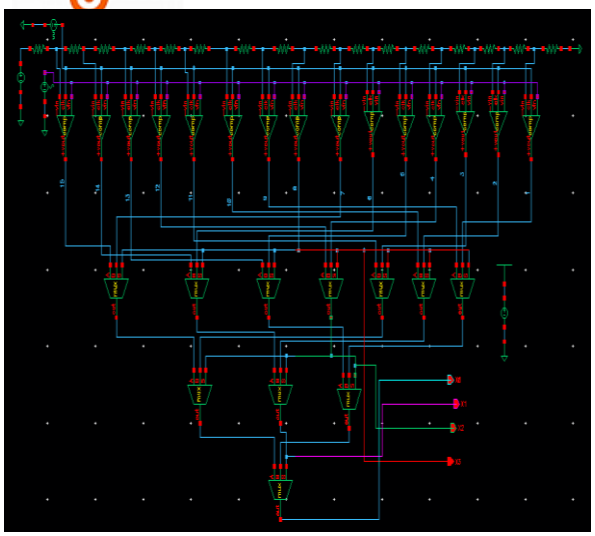

Fig 6: Schematic view of 4bit ADC

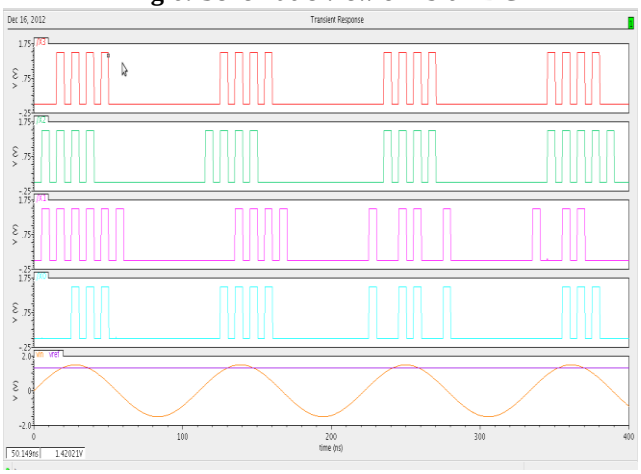

Fig 7: Output waveform of 4bit ADC

Table 2 shows the parameter values obtained for the 4bit ADC circuit under 90nm technology with supply voltage equal to 1.5V.

Table 2: Parameter Values for 90nm

Resolution	Frequency	Power dissipation	Conversion Time
4-bit	25MHz	1.943mW	6.182ns

IV. CONCLUSIONS

The problem of flash ADCs lies with limited resolution, high power dissipation because of the large number of high speed comparator. In this regard we have made an attempt to design a low-power 4bit ADC. The design and Pre simulation are carried out in cadence environment using spectre simulator under 90nm technology. The ADC design can be used for low power and high speed applications.

REFERENCES

1) Shubhara Yewale, Radheshyam Gamad "Design of Low Power and High SpeedMOS Comparator for A/D Converter application", Wireless Engineering and Technology, 2012, 3, 90-95.
2) B. Razavi, "Deign of Analog CMOS Integrated Circuits," Tata McGraw-Hill, Delhi, 2002.
3) R. Wang, K. Li, J. Zhang and B. Nie, "A High Speed High Resolution Latch Comparator For-Pipeline ADC," IEEE International Workshop on Anti-counterfeiting, Se- curity, Identification, Xiamen, 16-18 April 2007, pp. 28- 31.
4) W. Rong, W. Xiaobo and Y. Xiaolang, "A Dynamic CMOS Comparator with High Precision and Resolution," IEEE Proceedings of 7th International Conference on So- lid-State and Integrated Circuits Technology, 18-21 Oc- tober 2004, pp. 1567-1570.
5) ShaileshRadhakrishnan, Mingzhen Wang, Chien-In Henry Chen,"Low-Power 4-b 2.5GSPS Pipelined Flash Analog-to-Digital Converters in 3um CMOS", IEEE Instrumentation and Measurement Technology
6) Conference, vol. 1, pp. 287 – 292, May. 2005.
7) Chia-Nan Yeh and Yen-Tai Lai, "A Novel Flash Analog-to-Digital Converter", IEEE J, 2008.
8) G. M. Yin, F. Op'tEynde, and W. Sansen, "A high-speed CMOS comparator with 8-bit resolution", IEEE J. Solid -State Circuits, vol. 27, 1992.
9) Y. Sun, Y. S. Wang and F. C. Lai, "Low Power High Speed Switched Current Comparator," IEEE 14th Inter- national Conference, Ciechocinek, 21-23 June 2007, pp. 305-308.

Arunkumar. P Chavan born on July, 4th, 1987 in Karnataka, India, obtained his B.E degree in Electronics and Communication Engineering from Visvesvaraya Technological University (VTU), Belgaum, India. Currently pursuing M.Tech in VLSI Design and Embedded Systems. His areas of interest are VLSI design, Analog circuit design and digital electronics.

Rekha. G born on March, 15th, 1990 in Karnataka, India, obtained her B.E degree in Electronics and Communication Engineering from Visvesvaraya Technological University (VTU), Belgaum, India. Currently pursuing M.Tech in VLSI Design and Embedded Systems. Her areas of interest are VLSI design, Image Processing, and Digital electronics.

Narashimaraja. P born on January, 31st, 1982 in Tamilnadu, India, obtained his BE degree in Electronics from Madurai Kamaraj university, in 2004 and ME degree in VLSI Design from Bharath institute of higher education & research, in 2006. Currently, Is an Assistant professor at RV College of Engineering. His research interest are in the field of VLSI architectures, Memory design and Analog design.