Test Escape Study IN IC Manufacturing

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Abstract- The invention of IC technology has paved way for modern application and has miniaturized devices with low power consumption and high operational capabilities. India though is a developing country it has very few industries in the field of integrated circuits. SPEL semiconductor is the only organization in India with facilities of IC assembly and testing. The steps involved in the organization make sure that high yield is produced. The raw material passes through a series of steps like assembly and testing before being dispatched to the customer. There are many other supporting facilities which help the main operations of SPEL. Quality of the material is maintained high with "RIGHT THE FIRST TIME" as the motive. SPEL aims to become a natural destination for assembly processes. The hierarchy in SPEL is arranged so as the processes happens in a time effective manner. OJET, which is the main motive of this program aims at making a student highly salable finished product equivalent to that of an IC assembled in SPEL.

Improving efficiency of existing material can be obtained only if the existing workforce spends their time on value added services. For this the concept of motion study is utilized by whichwe can determine the operator efficiency and can use the data to produce rational and reasonable results. The status of machines are obtained to find out the amount of production and the wastage in resources.TR in pocket fail check has also been done to verify the procedure employed by operators in case of TR in pocket fail error. LOT PROCESSING involves following a lot from the time of entry to testing to the stage of getting reeled. For gravity handlers the times taken for each steps in processing of a lot are calculated and time periods of each are compared and top errors are tackled. For SRM HANDLERS the frequencies of errors are measured and the errors with high frequencies are minimized. SETUP STUDY has also been done as part of the program in which the time taken for different steps in setup is calculated and the non-value adding time is reduced.By doing setup study and lot processing the production rate can be improved by diminishing time wasters and reducing high frequency errors. However all said it would a futile attempt not to provide any solutions to the data analyzed by the above method. Withrespect to the company's functioning, feasibility and resources available solutions have been provided to the problems that were identified. The production is expected to raise with implementation of these solutions. There is also a great deal of experience and wisdom that has been culminated during these four months.

Keywords – LOT PROCESSING, SETUP STUDY, SPEL, IC, SRM HANDLERS.

Manuscript Received on December, 2012.

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I. INTRODUCTION

Semiconductor devices are electronic components that exploit the electronic properties of semiconductor materials, principally silicon, germanium, and gallium arsenide, as well as organic semiconductors. Semiconductor devices have replaced thermionic devices (vacuum tubes) in most applications. They use electronic conduction in the solid state as opposed to the gaseous state or thermionic emission in a high vacuum.

Semiconductor devices are manufactured both as single discrete devices and as integrated circuits (ICs), which consist of a number—from a few (as low as two) to billions—of devices manufactured and interconnected on a single semiconductor substrate, or wafer.

Semiconductor materials are so useful because their behavior can be easily manipulated by the addition of impurities, known as doping. Semiconductor conductivity can be controlled by introduction of an electric or magnetic field, by exposure to light or heat, or by mechanical deformation of a doped mono crystalline grid; thus, semiconductors can make excellent sensors. Current conduction in a semiconductor occurs via mobile or "free" electrons and holes, collectively known as charge carriers. Doping a semiconductor such as silicon with a small amount of impurity atoms, such as phosphorus or boron, greatly increases the number of free electrons or holes within the semiconductor. When a doped semiconductor contains excess holes it is called "p-type", and when it contains excess free electrons it is known as "n-type", where p (positive for holes) or n (negative for electrons) is the sign of the charge of the majority mobile charge carriers. The semiconductor material used in devices is doped under highly controlled conditions in a fabrication facility, or fab, to precisely control the location and concentration of p- and n-type dopants. The junctions which form where n-type and p-type semiconductors join together are called p-n junctions.

An integrated circuit or monolithic integrated circuit (also referred to as IC, chip, or microchip) is an electronic circuit manufactured by lithography, or the patterned diffusion of trace elements into the surface of a thin substrate of semiconductor material.

Additional materials are deposited and patterned to form interconnections between semiconductor devices.

Integrated circuits are used in virtually all electronic equipment today and have revolutionized the world of electronics. Computers, mobile phones, and other digital home appliances are now inextricable parts of the structure of modern societies, made possible by the low cost of producing integrated circuits.

ICs were made possible by experimental discoveries showing that semiconductor devices could perform the functions of vacuum tubes and by mid-20th-century technology advancements in semiconductor device fabrication. The integration of large numbers of tiny transistors into a small chip was an enormous

improvement over the manual assembly of circuits using discrete electronic components. The integrated circuit's mass production capability, reliability, and building-block approach to circuit design ensured the rapid adoption of standardized Integrated Circuits in place of designs using discrete transistors.There are two main advantages of ICs over discrete circuits: cost and performance. Cost is low because the chips, with all their components, are printed as a unit by photolithography rather than being constructed one transistor at a time. Furthermore, much less material is used to construct a packaged IC die than to construct a discrete circuit. Performance is high because the components switch quickly and consume little power (compared to their discrete counterparts) as a result of the small size and close proximity of the components. As of 2012, typical chip areas range from a few square millimeters to around 450 mm2, with up to 9 million transistors per mm2.

Integrated circuit originally referred to a miniaturized electronic circuit consisting of semiconductor devices, as well as passive components bonded to a substrate or circuit board. This configuration is now commonly referred to as a hybrid integrated circuit. Integrated circuit has since come to refer to the single-piece circuit construction originally known as a monolithic integrated circuit. Wafer-scale integration (WSI) is a system of building very-large integrated circuits that uses an entire silicon wafer to produce a single "super-chip". Through a combination of large size and reduced packaging, WSI could lead to dramatically reduced costs for some systems, notably massively parallel supercomputers. The name is taken from the term Very-Large-Scale Integration, the current state of the art when WSI was being developed.

A system-on-a-chip (SoC or SOC) is an integrated circuit in which all the components needed for a computer or other system is included on a single chip. The design of such a device can be complex and costly, and building disparate components on a single piece of silicon may compromise the efficiency of some elements. However, thesedrawbacks are offset by lower manufacturing and assembly costs and by a greatly reduced power budget: because signals among the components are kept on-die, much less power is required (see Packaging).

A three-dimensional integrated circuit (3D-IC) has two or more layers of active electronic components that are integrated both vertically and horizontally into a single circuit. Communication between layers uses on-die signaling, so power consumption is much lower than in equivalent separate circuits. Judicious use of short vertical wires can substantially reduce overall wire length for faster operation.

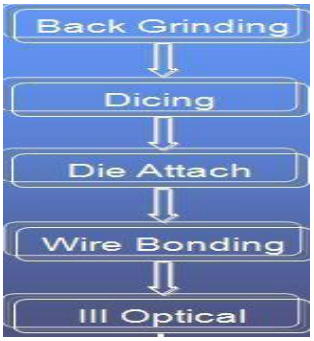
II. PROCESSES:

SPEL semiconductor has different sections for assembling and testing operations. The processes are divided into assembly and testing.

Assembly Process: The entire assembly package is divided into two sections.

1. Front on Line (FOL)
2. End on Line (EOL)

FOL:

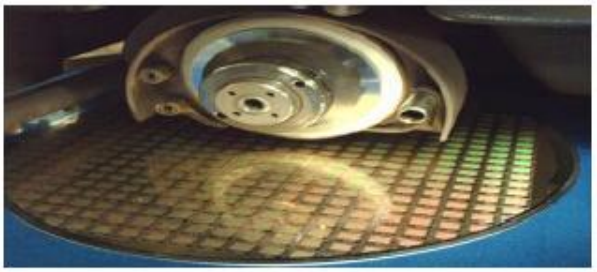


In this FOL process the tested Wafer is subjected to a series of machinery. **a.)Back grinding:**

Back-grind is the process of thinning down the wafers, by grinding on the back side of the wafer to the required final thickness depending on the package type. The thickness shall be reduced for 4” to 8”.

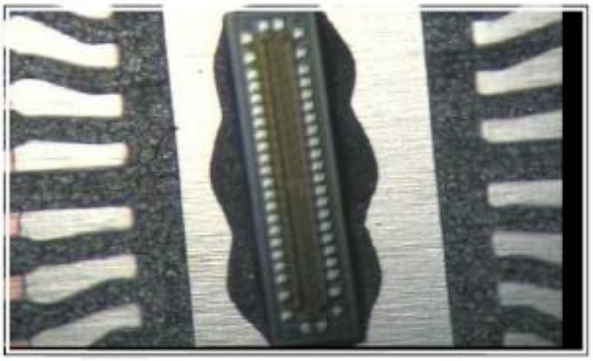
b.) Dicing:

It is the process of separating the individual dies from the wafer by suitable cutting techniques. The cutting is done generally using diamond coated blades so as to have a fine and accurate cut of the wafer. To move down the unwanted material we use recycled water .



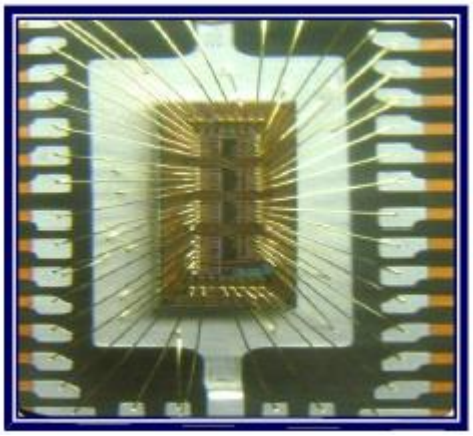
c.) Die Attach:

The diced dies are picked and bonded to the island of the lead frame with the help of electrically conductive adhesive material called silver epoxy. This die sheet is made to stick with epoxy and dried to an extent and the lead plate is placed on a heating pad on which the plate is molded and the die with epoxy is said to be fixed an got down to room temperature.



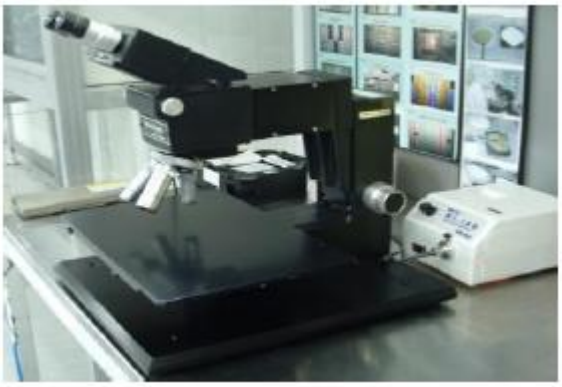
d.)Wire Bonding :

It is the process of interconnecting the pads in the die to the leads of the leadframe using gold wire (99.99% pure)



e.) III Optical Inspection:

All the FOL rejects are identified manually through optical inspection using microscope.



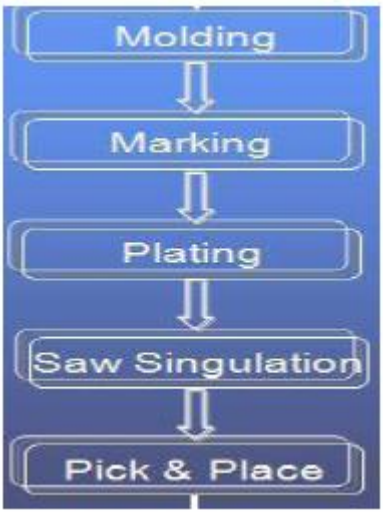
The rejections are marked by "X" on the scrap portion of the leadframe and sent to the next stage for

III. FURTHER PROCESSING.

EOL:

In this section the die which is in lead frame mush undergone through various steps of operations and then form as an IC, which is required to the customer.

The process carried out in EOL stage are



MOLDING:

Why Molding is necessary?

•It protects the internal circuit from all external environment.

•For easy handling.

•To Provide Heat dispersion.

Raw Material: Wire Bonded Leadframes, Epoxy Molding Compound

The wire bonded leadframe is molded using "epoxy molding compound". It is a thermo set plastic.

DEJUNK & TRIM:

The interconnecting metal Dam bar which connects all the leads to block the mold compound flow during molding, is removed.

Why Dejunk?

The metal between the package leads will result in SHORT failure during the electrical testing of the devices after the assembly.

MARKING:

Marking is the process of engraving the required mark information using LASER on top / bottom of the package for easy identification and traceability.

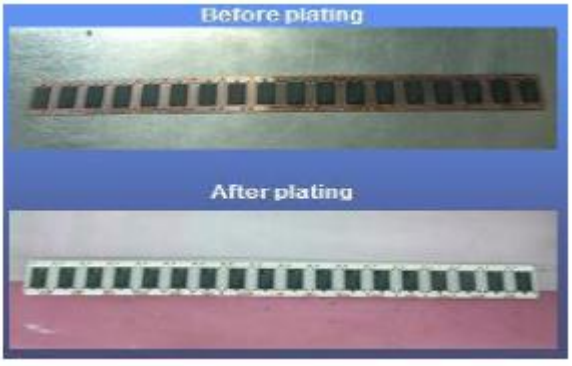
Marking particulars are: Device type, Assembly location, Date of manufacturing etc.,

PLATING:

It is a process of applying a coat of metal or an alloy over the leads of an Integrated Circuit.

Why it is necessary?

Better appearance.

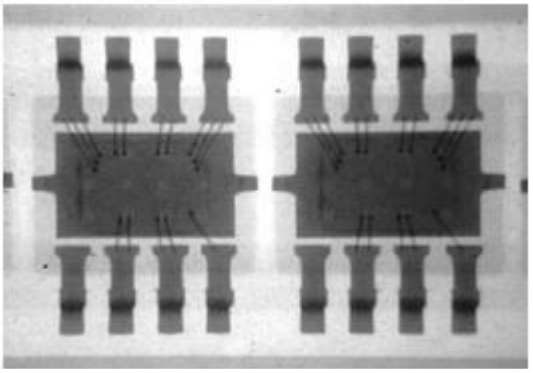


FORM & SINGULATION:
The leadframe is singulated into individual IC and formed into the required profile.

4.3 TESTING:
Once the front-end process has been completed, the semiconductor devices are subjected to a variety of electrical tests to determine if they function properly. The proportion of devices on the wafer found to perform properly is referred to as the yield.
WAFER TEST
The highly serialized nature of wafer processing has increased the demand for metrology in between the various processing steps. Wafer test metrology equipment is used to verify that the wafers haven't been damaged by previous processing steps up until testing. If the number of dies—the integrated circuits that will eventually become chips— etched on a wafer exceeds a failure threshold (i.e. too many failed dies on one wafer), the wafer is scrappedrather than investing in further processing.
DEVICE TEST
Once the front-end process has been completed, the semiconductor devices are subjected to a variety of electrical tests to determine if they function properly. The proportion of devices on the wafer found to perform properly is referred to as the yield.
The fab tests the chips on the wafer with an electronic tester that presses tiny probes against the chip. The machine marks each bad chip with a drop of dye. Currently, electronic dye marking is possible if wafer test data is logged into a central computer database and chips are "binned" (i.e. sorted into virtual bins) according to predetermined test limits. The resulting binning data can be graphed, or logged, on a wafer map to trace manufacturing defects and mark bad chips. This map can be also used during wafer assembly and packaging.
Chips are also tested again after packaging, as the bond wires may be missing, or analog performance may be altered by the package. This is referred to as "final test".
Usually, the fab charges for test time, with prices in the order of cents per second. Test times vary from a few milliseconds to a couple of seconds, and the test software is optimized for reduced test time. Multiple chip (multi-site) testing is also possible, since many testers have the resources to perform most or all of the tests in parallel.
Chips are often designed with "testability features" such as scan chains and "built-in self-test" to speed testing, and reduce test costs. In certain designs that use specialized analog fab processes, wafers are also laser-trimmed during test, to achieve tightly- distributed resistance values as specified by the design.
Good designs try to test and statistically manage corners: extremes of silicon behavior caused by operating temperature combined with the extremes of fab processing steps. Most designs cope with more than 64 corners.
TEST ESCAPE ANALYSIS:

(TEST FAIL DETAILS CAN BE KNOWN BY DOING BELOW OPERATONS)
1) X-ray test
2) Non-Destructive test
3) Destructive test

X-ray test can give the information about problems in bonding, breakages in connections etc..



Non-Destructive test reveals the problems during die attach i.e. epoxy is properly fixed on lead frame
Destructive test can gives the problems of die. For this first we have to remove the pellet by doing acidification, hence the IC is lost that's why this test is called destructive test.
 Here we design the interfacing media between handler and tester only.
 The mother boards are imported from others and we can code it (or) follow customer's codes.
Significant Defect:
a) Defects that shall pass the electrical test but however have a very high risk of potential field failure due to reliability concern.
b) Defects that shall make the devices totally unfit for use shall also come under this category. (Eg., Reverse Molding, Reverse Forming, Reverse Marking etc)
c) The devices and the lot that do not meet the acceptance criteria in process monitor tests shall come under this category.
d) Any major violation of customer's instruction/ requirements shall come under this category. (Usage of wrong material such as molding compound, wrong plating composition specification, wrong marking information etc).

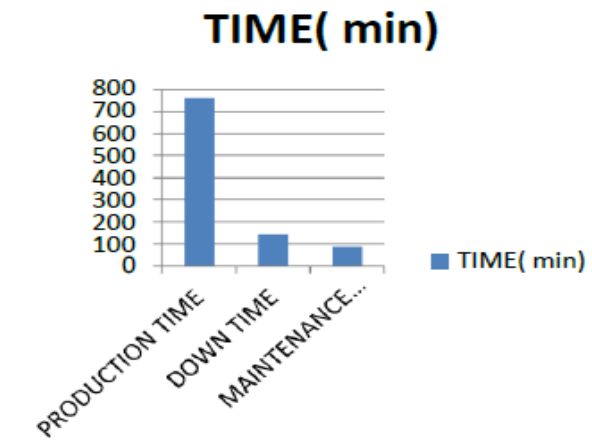
Critical Defect:
Defects that shall pass the electrical test but however have a very low risk of field failure due to reliability concern.
Major Defect:
a) Defects that would result in Electrical Failure and hence could make the unit non- functional.
b) Defects that could be a cause for low electrical test yield shall come under this category.
c) Defects with external package dimensions that shall not meet the appropriate package outline drawings.

Minor Defect:
Defects categorized as poor workmanship or cosmetic related. Defects that could be a cause for low assembly yield shall come under this category.
OPERATION OF SRM HANDLER:
First the ICs which are to be tested are poured into a vibrating

bowl, then the arrangement in bowl can set the ICs in proper order and send it into rotator. The sucker mechanism in rotator sucks the ICs and placed them into precissor1, this check the alignment and send it to rotator which aligns the IC and then checks the marking. If this marking fails then IC directly goes to appropriate rejection bucket. Else it goes to another precissor2 and checks the alignment again and goes for packing in tape or tubes. The bad ICs goes to appropriate rejection buckets according to their failures.

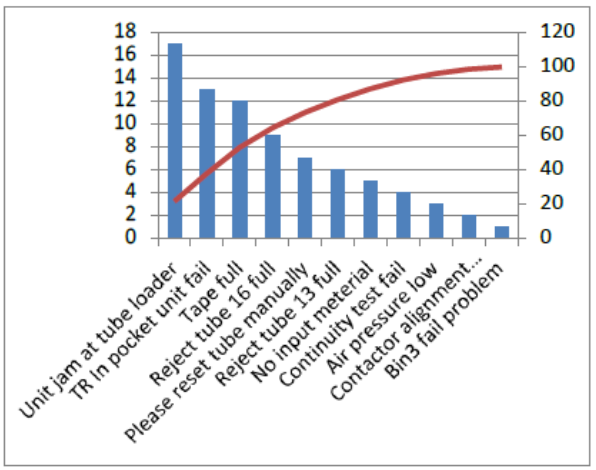
TIME ANALYSIS OF SRM HANLDERS-

HANDLER# H-58



Here, a sample of 2-3 Week's PARETO charts is shown

HANDLER#H-58



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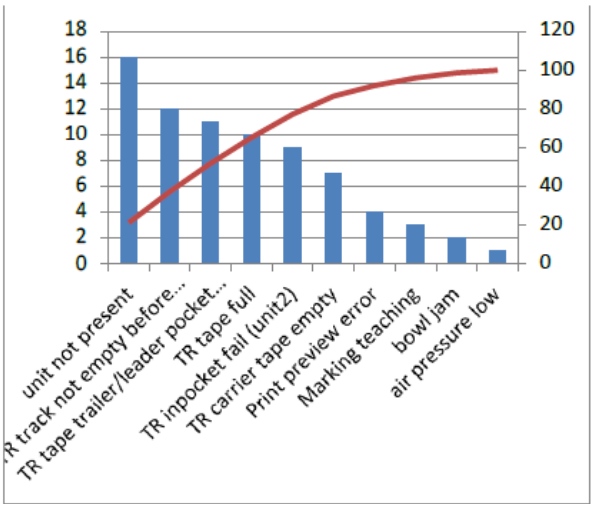

TTACKING THE PROBLEM

Proposed Solutions for Reduction of down Time due to these major contributors:

1. Unit not present: Why it occurs:

Generally, Unit not present occurs if any IC in not present at the input side of the machine i.e. at the nozzle which is picking up the IC's. This is mainly because of SETUP problem. If the setup is done with fewer loads, then the UNIT NOT PRESENT error occurs.

How to fix it:

Basically, this error is completely SETUP related. This is the sole duty of the operator to monitor whether the Unit is present at the nozzle or not. So, the operator must monitor periodically to avoid this type of error. SETUP must be done with Optimum Load

The input material in the bowl should be large enough every time so that there will be no question of Unit not present error.

2. Bowl Jam: Why it occurs:

Bowl jam is the error in which all the IC's get jammed and can't enter in to the input track. This also occurs mainly due to the SETUP problem or imperfect SETUP. If the setup is done with too much load, then BOWL JAM occurs.

How to fix it:

Bowl jam occurs most frequently in all the machines due to the fact that the IC's not entering in to the input track because of blocking of their way in to the track caused by single IC.

So, in order to fix it, SETUP must be done with optimum load.

Also, there must be a provision for an air blower and a sensor at the input track so that as soon as Bowl jam occurs, automatically the air should be blowed at the input track so that the IC gets out of its position without blocking other units. This should be automated.

3. Unit jam at Vision Table: Why it occurs:

Unit jam at vision table occurs mainly due to the wrong orientation of the unit at the vision table. So, the cause of this error must be due to the Precisor's problem of not positioning the IC in correct position.

How to fix it:

The general process that we would follow when Unit jam error occurs is to remove the unit from the site and place it in the bowl. But, if we would concentrate on the Precisor itself whether it has done its job correctly or not, then we can easily reduce the error of Unit jam.

So, Fine Tuning must be done to avoid the problem.

4. GPIB Tester timeout: Why it occurs:

GPIB-'General Purpose Interface Bus' are the cables used for interfacing the tester and handler. The tester time out occurs in case the unit is not tested with in the test time frame.

As soon as the unit reaches the test site, SOT (Start of Test) signal is sent to the tester by the handler and then test is being done. After the test completed, whether pass or fail the tester sends 10

EOT (End of Test) signal to the handler. If the SOT and EOT are not generated within the stipulated time then the tester time out occurs.

How to fix it:

When this error occurs, the IC is sent in to the bucket by default and is again tested in the re-test process. This error can also be caused due to any disturbance in the cable equipment so that it can't communicate with the handler with in the time frame.

So, care must be taken in fixing these cables so that the error gets minimized.

If we can increase the time frame of the test time in the program loaded, we can overcome this error but it takes some more time to process completely. But yield is much more important than time taken for it so better increase the test time frame.

5. TR Inpocket fail: Why it occurs:

The TR Inpocket fail error occurs if any accumulation of dust on the unit occurs before entering in to the reel or even any wrong marking on the units.

Generally, as soon as this error occurs, it is advisable to replace the IC from the good samples so that all the good ones will be entering in to the reel.

How to fix it:

In order to fix this error, the unit must be made free of the accumulation of dust on it and care should be taken during the marking of IC's.

CONCLUSION:

As the quote says- "IT TAKES MONTHS TO FIND A CUSTOMER BUT ONLY SECONDS TO LOSE ONE". Even though maintaining a healthy relationship with the customer would not ensure development of the company. The quality makes the difference.

So in order to have a good bonding with the customer, the first thing that has to be focused is on the Quality. So in order to ensure such quality, a close monitoring is required periodically. This evolves the concept of "Test escape study and implementation of error proof mechanism for each test system/handlers". In this procedure, each and every lot is observed closely and can come up with solutions to counteract the effect of the loop holes.

Test escape study is nothing but observing the handlers during their process and checking that if there is any possibility of an IC that is not tested by the tester.

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