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Analysis of Different Multiplier with Digital Filters Using VHDL Language

Ruchi Sharma

Abstract— Performance as well as Area are the two main design tolls, power consumption also become a vital concern in VLSI system design. A system's performance is generally determined by the performance of the multiplier because the multiplier is the slowest element in the system. area and speed are usually conflicting constraints so that for improving the speed of the system results in larger areas. As a result, a multipliers with optimized area & speed has been designed with fully parallel algorithms. The need for low-power VLSI system arises from two main forces.

Keywords: system's performance, area, multiplier, booth algorithm.

I. MOTIVATION

The scale of integration keeps growing rapidly & many sophisticated signal processing systems are being designed on a VLSI chip. These signal processing applications not only required great computation capacity but also consume considerable amount of energy. A system's performance is generally determined by the performance of the multiplier because the multiplier is the slowest element in the system. Furthermore, multipliers are very area consuming. Hence, optimizing the speed and area of the multiplier is a major design issue. However, area and speed are usually conflicting constraints so that for improving the speed of the system results in larger areas. As a result, a multipliers with optimized area & speed has been designed with fully parallel algorithms. The need for low-power VLSI system arises from two main forces. First, with the steady growth of operating frequency and processing capacity per chip, large amount of current has been delivered and the heat generate due to large power consumption must be removed by proper cooling techniques. Second, battery life in portable or mobile electronic devices is limited. Low power design directly leads to prolonged operation time in these portable devices. Therefore low-power multiplier design has been an important part in low- power VLSI system design. Extensive work has been done on designing low-power multipliers at technology, physical, circuit and logic levels.

II. INTRODUCTION

Multiplier is one of the very important hardware blocks in most digital and high performance systems such as FIR filters, digital signal processors and microprocessors etc. In this project, we worked on an efficient implementation of high speed multiplier using the shift and add method, Radix_2, Radix_4 modified Booth multiplier algorithm. In this project we compare the working & the characteristics of the three multiplier by implementing each of them separately in FIR filter.

The parallel multipliers like radix 2 and radix 4 modified booth multiplier perform the computations using lesser adders and lesser iterative steps. As a result of which they cover lesser space as compared to the serial multiplier. This is a very important criterion because in the fabrication of chips and high performance system requires components which are as small as possible.

In this paper, after making comparison on power consumption between different multipliers we find that serial multipliers consume more power. So power is an important criterion there we should prefer parallel multipliers like booth multipliers to serial multipliers. The low power consumption quality of booth multiplier makes it a preferred choice in designing different circuits

In this we first designed three different type of multipliers using shift and method, radix 2 and radix 4 modified booth multiplier algorithm. We used different type of adders like sixteen bit full adder in designing that multiplier. Then we designed a 4 tap delay FIR filter and in place of the multiplication and additions we implemented the components of different multipliers and adders. Then we compared the working of different multipliers by comparing the power consumption by each of them. The result of this paper helps us to choose a better option between serial and parallel multiplier in fabricating different systems. Multipliers form one of the most important component of many systems. So by analyzing the working of different multipliers helps to frame a better system with less power consumption and lesser area.

The result of this paper helps us to make a proper choice of different multipliers in fabricating in different arithmetic units as well as making a choice among different adders in different digital applications according to requirements. All the programs and results have been given in the following sections.

2.1 Low power and area efficiency

Power consumption increase in a standard CMOS VLSI design for FFT application is due to the complex multiplication within the butterfly design. There are several methods of computing FFT algorithm in the signal processing in literature which involves different number of computation. This dissertation compares the conventional radix-4 architecture and enhanced radix-4 architecture in term of power and area by modification algorithm in FFT processor to reduce the number of mathematical computation which decreases the number of hardware. Concentration is given to FFT computation method where FFT algorithm encompasses many complex multiplication and addition within the butterfly processing unit which significantly consumes power in the FFT with large active chip area consumption.

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Tools Required for Simulation :

- XILINX 8.1
- XILINX ESTIMATOR

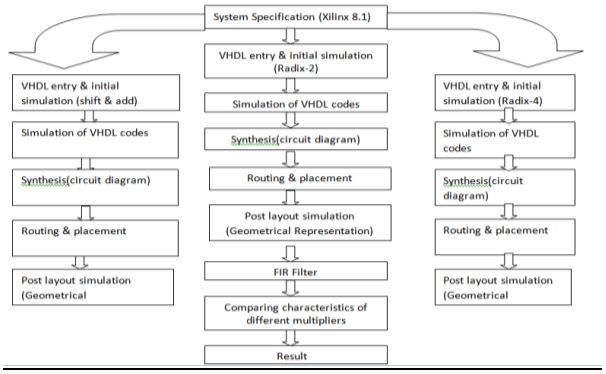
III. XILINX POWER ESTIMATOR

The XPower Estimator (XPE) spreadsheet is a power estimation tool typically used in the pre-design and pre-implementation phases of a project.

XPE helps in architecture evaluation and device selection and helps you select the appropriate power supply and the thermal management components which may be required for your application.

It is a pre-implementation tool, can be used in the early stages of a design cycle when the RTL description of the design is incomplete. After implementation, the XPower Analyzer (XPA) tool (available in the ISE Design Suite software) can be used for more accurate estimates and power analysis.

IV. FLOW DIAGRAM



V. PROPOSED ALGORITHM

In this paper, we worked on an efficient implementation of high speed multiplier using the shift and add method, Radix_2, Radix_4 modified Booth multiplier algorithm. In this paper, we compare the working & the characteristics of the three multiplier by implementing each of them separately in FIR filter.

5.1 Booth Multiplication Algorithm for Radix 2

Booth algorithm is the procedural algorithm used for multiplying binary integers in signed –2's complement representation. We will illustrate the booth algorithm with the following example:

Example,

2ten x (- 4)ten

0010two * 1100two

Step 1: Making the Booth table

I. From the two numbers, pick the number with the smallest difference between a series of consecutive numbers, and make it a multiplier. i.e., 0010 -- From 0 to 0 no change, 0 to 1 one change, 1 to 0 another change ,so there are two changes on this one 1100 -- From 1 to 1 no change, 1 to 0 one change, 0 to 0 no change, so there is only one change on this one.
Therefore, multiplication of 2 x (– 4), where 2ten (0010two) is the multiplicand and (– 4)ten (1100two) is the multiplier.

II. Let A = 1100 (multiplier)
Let B = 0010 (multiplicand)
Take the 2's complement of B and call it –B
–B = 1110

III. Load the A value in the table.

IV. Load 0 for A-1 value it should be the previous first least significant bit of A.

V. Load 0 in U and V rows which will have the product of A and B at the end of operation.

VI. Make four rows for each cycle; this is because we are multiplying four bits numbers.

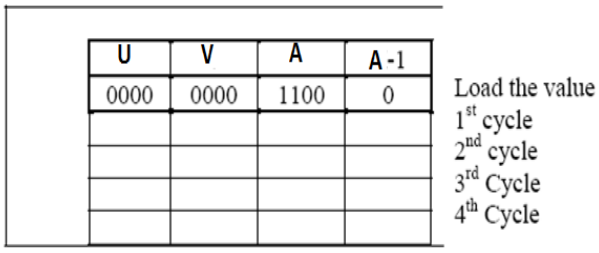


Fig. Algo step 1

Step 2: Booth Algorithm

Booth algorithm needs the examination of the multiplier bits, and shifting of the partial product. Before the shifting, the multiplicand may be added to partial product, subtracted from the partial product, or left unchanged according to the following rules:

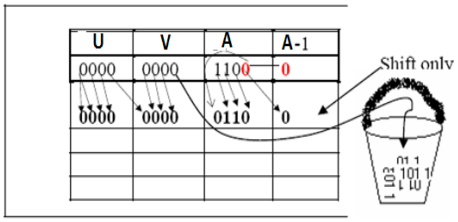
Look at the first least significant bits of the multiplier "A", and the previous least

significant bits of the multiplier "A - 1".

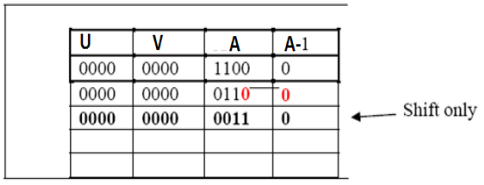
1.) 0 0 Shift only
1 1 Shift only.
0 1 Add B to U, and shift
1 0 Subtract B from U, and shift or add (-B) to U and shift

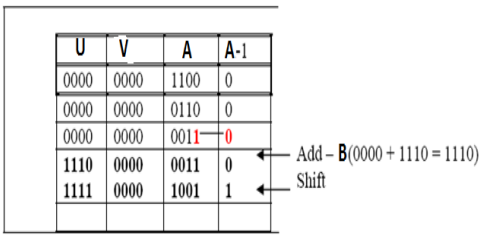
2.) Take U & V together and shift arithmetic right shift which preserves the sign bit of 2's complement number. Thus a positive number remains positive, and a negative number remains negative.

3.) Shift A circular right shift because this will prevent us from using two registers for the A value.



Repeat the same steps until the four cycles are completed.





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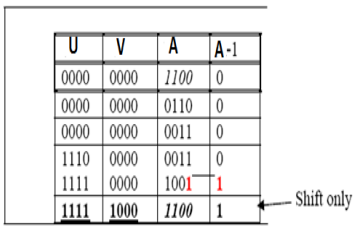

Fig: step 2 Example of booth Algo

We have finished four cycles, so the answer is shown, in the last row of U and V Which is (1111100) two.

5.2 Booth Algorithm for Radix-4

Booth algorithm which scan strings of three bits with the algorithm given below:

- Extend the sign bit 1 position if necessary to ensure that n is even.
- Append a 0 to the right of the LSB of the multiplier.
- According to the value of each vector , each Partial Product will be 0, +y , -y, +2y or - 2y.
- For product generator, multiply by zero means the multiplicand is multiplied by "0".Multiply by "1" means the product still remains the same as the multiplicand value. Multiply by "-1" means that the product is the two's complement form of the number. Multiply by "-2" is to shift left one bit the two's complement of the multiplicand value and multiply by "2" means just shift left the multiplicand by one place.

VI. EXPERIMENTAL WORK

After analyzing all the three multipliers by booth algorithm, and compare their characteristics in terms of multiplication speed, no of computations required, no of hardware, we come on finding that parallel multipliers are better than series multipliers.

By implementing both Radix-2 & Radix -4 multiplier using booth algorithm we analysis that their computation speed increases so much.

Then , in this project these multipliers implement with FIR filters to compare the speed, power consumption, computations, hardware requirement of the system.

We have done the coding of all the multipliers separately in VHDL & simulate it to get the accurate waveforms as output.

Then we implement these multipliers separately with FIR filters using computation techniques like FFT, DFT. These coding also written in VHDL language & simulate it to get the RTL circuit of each system.

Also get the lookup table , where we get the exact no of i/p, o/p/ no of slices requirement etc for the system.

Xilinx Estimator analysis these simulated results & determine the power consumption of each system. These results are given below.

VII. PROJECT EVALUATION

Results of Different Multipliers

8.1 Array Multiplier

Number of Slices	81
Number of 4 input LUTs	140
Number of bonded INPUT	16
Number of bonded OUTPUT	16
CLB Logic Power	2.40W

- **HDL Synthesis Report**

Macro Statistics

# Xors	: 56
1-bit xor2	: 8
1-bit xor3	: 48

8.2 Radix -2 Booth Multiplier

Number of Slices	77
Number of 4 input LUTs	141
Number of bonded INPUT	16
Number of bonded OUTPUT	16
CLB Logic Power	2.023W

- **HDL Synthesis Report**

Macro Statistics

# Adders/Subtractors	: 4
9-bit adder	: 4
# Xors	: 48
1-bit xor3	: 48

8.3 Radix -4 Booth Multiplier

Number of Slices	97
Number of 4 input LUTs	171
Number of bonded INPUT	16
Number of bonded OUTPUT	17
CLB Logic Power	1.84W

- **HDL Synthesis Report**

Macro Statistics

# Adders/Subtractors	: 4
9-bit adder	: 4
# Xors	: 48
1-bit xor3	: 48

VIII. MULTIPLIER SIMULATION

Output waveforms:

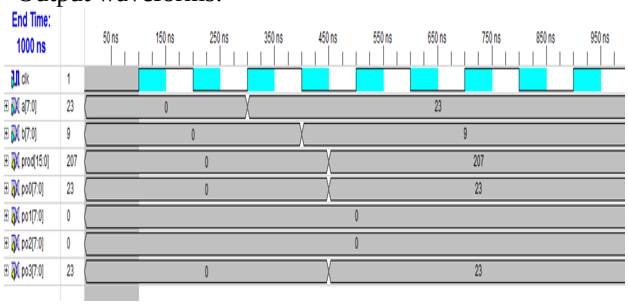

Fig1 : Output of shift & add multiplier

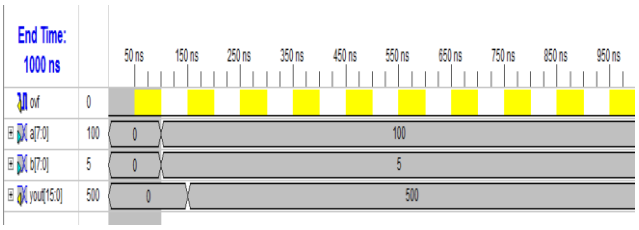

Fig 2: Output of radix 2 multiplier

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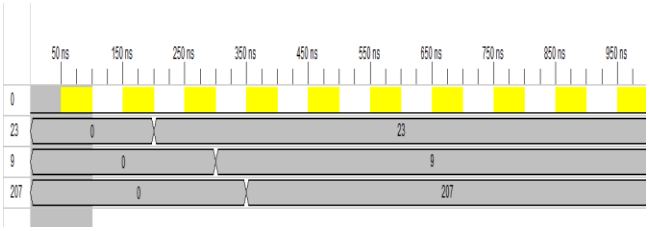

Fig 3: Output of radix-4 multiplier

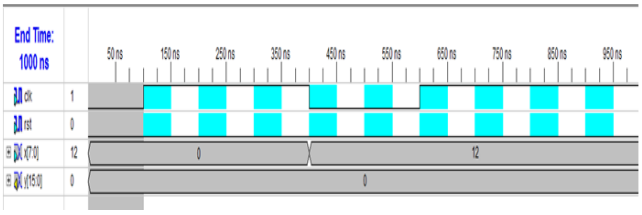

Fig 4 : Output of fir filter with shift & add multiplier

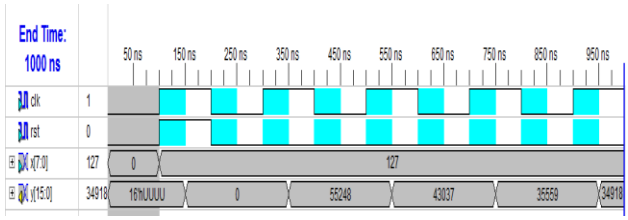

Fig 5: Output of fir filter with radix-2 multiplier

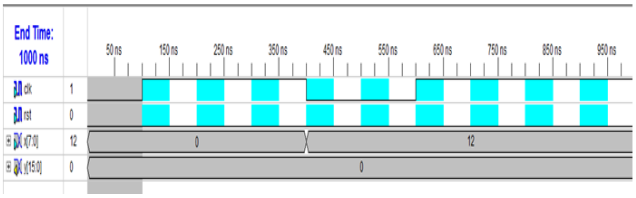

Fig 6: Output of fir filter with radix-4 multiplier

IX. POWER ESTIMATION

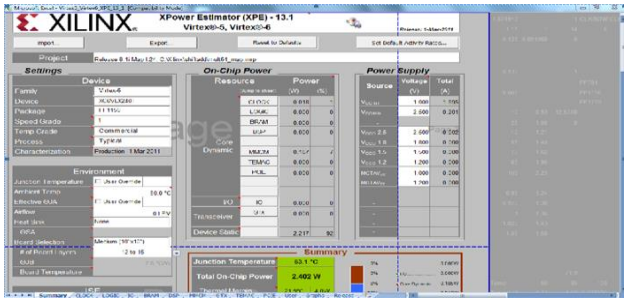

Fig 7: Power calculation of shift & add multiplier

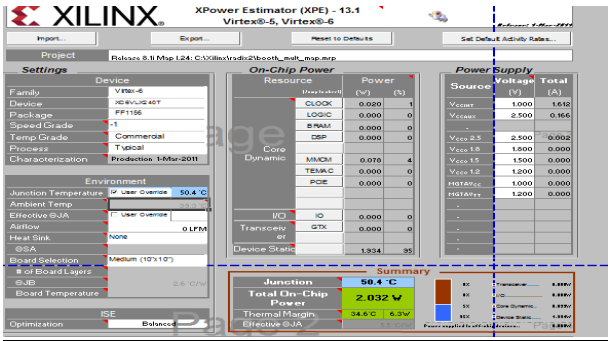

Fig 8: Power calculation of radix 2 multiplier

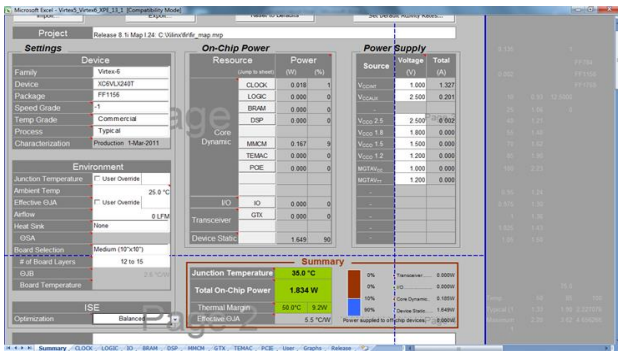

Fig 9: Power calculation of radix-4 multiplier

X. CONCLUSION

This paper clear concept of different multiplier and their implementation in tap delay FIR filter. We found that the parallel multipliers are much option than the serial multiplier. We concluded this from the result of power consumption and the total area. In case of parallel multipliers, the total area is much less than that of serial multipliers. Hence the power consumption is also less. This is clearly depicted in our results. This speeds up the calculation and makes the system faster.

While comparing the radix 2 and the radix 4 booth multipliers we found that radix 4 consumes lesser power than that of radix 2.

XI. FUTURE WORK

As an attempt to develop arithmetic algorithm and architecture level optimization techniques for low-power multiplier design, the research presented in this dissertation has achieved good results and demonstrated the efficiency of high level optimization techniques. However, there are limitations in our work and several future research directions are possible. One possible direction is radix higher-than-4. We have only considered radix-4 as it is a simple and popular choice. Higher-radix further reduces the number of PPs and thus has the potential of power saving. Another possible direction can be representation of Arguments such as in sign-magnitude or 2's compliment form which in any case would prove better according to situation and require less power and consume less time.

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