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Rapid Prototyping Environment for Power Line Modem Design, Implementation, Verification, and Optimization

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Abstract—This paper describes design, implementation, verification and optimization of a power line modem with model-based evaluation approach. Nowadays, model-based design for embedded systems is used extensively to accelerate the development time and to improve the quality of the resulting applications by systematic design and test. The majority of DSP designers today use the MathWorks software includes MATLAB and/or Simulink as a foundation tool not only for simulation but also for real-time target specific C-code generation. In our modem project, all parts including transmitter, receiver, I/O drivers and startup protocols have been realized entirely in Simulink environment for simulation and hardware implementation. A floating-point DSP has been carried out to minimize the time required to convert simulation software into real-time code. In order to verify the algorithms, real-time data exchange has been developed to test our DSP designs in-situ with real data. Finally, for code optimization, profiling method has been employed to identify segments of generated code that may benefit from additional modification.

Index Terms— High Voltage Power Line Modem, Legacy Code Integration, Model-based Design, Profiler, S-function and Target for TI C6000.

I. INTRODUCTION

The idea for utilization of high voltage power lines for communication has been presented from early developments of the power utility systems [1]. Through all over the world, power line carrier (PLC) systems have been planned for this purpose. Likewise the general trend in all communication systems, digital PLC is preferred to analog one. DPLC has many parts to provide reliable link for transferring voice and data over high voltage lines.

Base-band modems are the main element of a digital PLC. The desired functionality of a digital PLC entirely depends on base-band modem performance. The aim of this paper is the presentation of this modem from design concepts to hardware implementation and verification. For simplicity, HV modem will stand for base-band modem in a digital PLC at the rest of paper.

Traditional algorithm development procedure for DSP is to write C or assembly code in an integrated development environment (IDE) and compile, debug and load an executable file on hardware. This kind of project development method has main drawbacks. The handwritten code approach is not flexible, modular and systematic and finally is not easily upgradeable [2].

In industry today the time allocated for a product design cycle is always being shortened. It is imperative to take advantage of the latest tools and technologies to speed the development of a system.

Nowadays, Simulink as a foundation tool is not only for simulation but is also for real-time target specific C-code generation. Simulink, Real-Time Workshop (RTW), Target for TI C6000, and Link for Code Composer Studio provide an integrated platform for designing, simulating, implementing, and verifying embedded signal processing systems on standard and custom TI C6000 processors [3].

We present here a systematic and efficient simulation and rapid prototyping environment together for a HV modem design and real–time implementation.

II. HV MODEM TRANSMITTER AND RECEIVER SECTIONS

For each digital communication systems, it is preferable to simulate the necessary component of that system before real-time implementation. So we first simulate HV modem specially the receiver part because of its complexity and importance. Software plays an important role here for this purpose.

MATLAB is the world's leading software for algorithm development. It lets engineers design algorithms, create test scripts, optimize component and system performance. In conjunction with a number of application-specific toolboxes and GUIs, the tool provides a vast library of mathematical modeling and computational functions that may simplify designer's development work. But, scripts cannot be easily translated to hardware-oriented code. However, Simulink is ideal for this purpose.

The MathWorks Simulink tool allows simulation of MATLAB scripts and C-coded S-function in conjunction with system components known as blocksets.

In this project, we have modeled transmitter, receiver and I/O ports for HV modem entirely in Simulink because of its indisputably similar simulation results to realistic conditions and the ability to generate a C-language real-time implementation of the Simulink model.

The transmitter of HV modem encodes symbols to TCM-64QAM constellation points which have been shaped with square root raised cosine filter and finally mixed with carrier signal. The transmitter has been modeled totally with Simulink blocks.

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For receiver part, we have used combination of application-specific blocks with C-coded S-function. The receiver has five main constituents: Timing recovery, automatic gain controller (AGC), carrier recovery, adaptive equalizer, and TCM-QAM decoder. Carrier recovery loop along with adaptive equalizer has been modeled with C-coded S-function. The rest of the items have been designed with application-specific blocks.

All variables and signals in HV modem are frame-based in Simulink for transmitter and receiver. This is important for these projects because the real-time hardware realization is of concern. The frame-based throughput rate is therefore many times higher than the sample-based alternative.

A. Timing Recovery

Squaring timing recovery has been developed for determination of timing offset from the given samples of the signal [4]. Squaring timing estimation can be categorized as feed forward frame-based method. Squaring method is preferable to fixed rate re-sampling timing recovery method like Farrow interpolation approach which has been compared for this project and finally the former method has been selected.

To achieve the best accuracy, a pre-filter and to minimize timing jitter a post-filer [5] has been considered for squaring timing recovery as sketched in Fig. 1.

B. Carrier Recovery and Adaptive Equalizer

A decision directed carrier recovery loop accompanied with an adaptive equalizer are responsible for phase/frequency offset correction and channel compensation [6]. A decision directed loop block diagram for M-QAM carrier recovery is shown in Fig. 2.

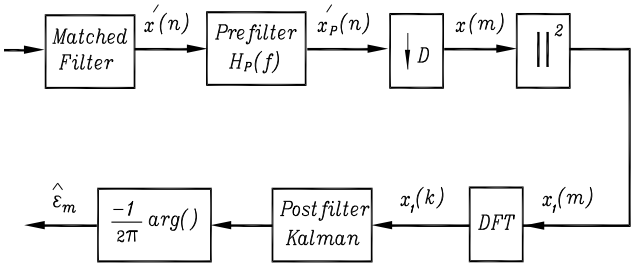

Fig. 1. Squaring timing phase recovery with pre-filter and post-filter for best timing estimation in HV modem.

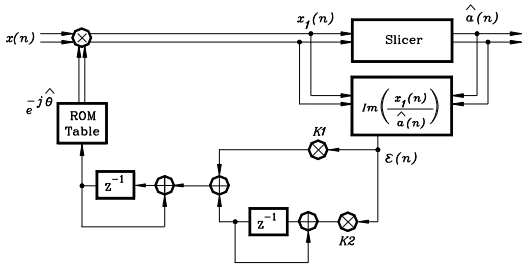

Fig. 2. Decision-directed carrier recovery loop.

Both PI loop filter coefficients should be computed precisely based on four important constants. Sampling rate, equivalent noise bandwidth (ENB), bit rate and error detector architecture will determine coefficient values. If K1 and K2 are proportional and integral carrier recovery loop filter coefficients respectively, they can be found by:

$$K_1 = \frac{(4\xi\theta_n)}{(1 + 2\xi\theta_n + \theta_n^{\,2})(2\pi)} \quad (1)$$

$$K_2 = \frac{(4\theta_n)^2}{(1 + 2\xi\theta_n + \theta_n^{\,2})(2\pi)} \quad (2)$$

Table I summarizes parameters and constants of the HV model in order to accomplish carrier synchronization for a 64QAM coherent demodulator.

Table I. The HV Model Carrier Recovery Loop Constants

Parameter setting in the developed software		
Parameter	Name	Value
B_L	ENB carrier loop	(3/100) r_b=1314 Hz
T	symbol period	1/7300
M	sample per symbol	4
f_c	carrier frequency	4500 Hz

For mutual dependency of channel compensation and phase/frequency offset correction, a base-band adaptive equalizer should be indeed replaced between multiplier and slicer block in Fig. 2.

Because of an Algebraic loop diagnostic error for carrier recovery and equalizer loop in Simulink in frame-based mode, a C-coded S-function has been written.

In both simulation and real-time application, a compiled version of C-source file of an S-function is required. Simulink and Real-Time Workshop (RTW) need the mex-file to read the information of the S-function. It is also possible to generate the mex dll file for an S-function via MATLAB's mex command. However, MATLAB needs to be set up properly before designer use the mex command.

In the recent release of MATLAB, there is an alternative to a hand-coded S-function. Now it is possible to use the S-Function Builder block known as User-Defined Functions to implement simply C coded S-functions. This is a Simulink block that builds an S-function from specifications and C code that designer supply. The block also serves as a wrapper for the generated S-function. For carrier recovery and equalizer loop all required Inport/Outport and its algorithm has been defined within an S-Function Builder block.

C. Trellis Coded Modulation

Impulsive character of the PLC dominant noise known as corona requires a higher signal to noise ratio (SNR) than in the AWGN channel. The corona noise on power line is considered as a Gaussian noise with time-variable RMS value [1]. Trellis coded modulation (TCM) represents a common method used in the digital PLC system available on market to overcome corona noise.

TCM is a technique in which modulation and coding are combined together. For band-limited channels, trellis codes are feasible by means of increasing performance.

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Trellis codes expand neither the bandwidth nor the transmitted power, which is an appealing property over many other codes. The TCM can be divided to three sections: trellis encoding, set partitioning and decoding.

There are several methods for decoding convolutional codes. In HV modem Viterbi algorithm selected for symbols decoding, because I) its efficient way of computing the distance between the received sequence of symbols and all possible sequences II) it is fast enough to allow real-time decoding for short constraint length with high-speed processors. In summary, HV modem physical layer has the main following characteristics. It is fixed-step, floating-point, frame-based, multi-rate, and single-task. All of these issues has been set through Simulink and finally implemented to the C6713 Texas Instrument (TI) digital signal processor (DSP) by means of RTW, Target for TI C6000, Link for Code Composer Studio and CCS.

III. CUSTOM DEVICE DRIVER VIA LEGACY CODE INTEGRATION

To communicate with external world, digital and analog port initialization and utilization is inevitable for any modem.

There are some blocks for C6713 DSK board such as ADC, DAC, and LED in Simulink (Target for TI C6000™ library), but they were not sufficient for HV modem application. It is needed to configure Multichannel Buffered Serial Port (McBSP) for providing serial data communication with modem and finally defining General-Purpose Input/Output (GPIO) pins for status indication.

By the use of Real-Time Workshop Custom Code blocks and C6000 DSP Core Support from Target for TI C6000™ library together with legacy code integration, we can implement any custom device driver on Texas Instruments DSP platform [3].

For our application, it is necessary to configure Enhanced Direct Memory Access (EDMA), McBSP and GPIO, in such a form that they can be added to the generated project via Simulink.

In HV modem, all McBSPs were linked to two EDMA channels in ping-pong scheme to decrease the CPU load and prevent losing of data from I/O while algorithm is being executed. Moreover, the serial data communication and codec EDMA channels raise an interrupt for transmitter section and a separate one for receiver when the transfer request completes.

The following items declare I/O driver initialization and definition procedures which can be effectively integrated with HV modem transmitter and receiver algorithms.

HWI block: for setting up an interrupt service routine (ISR) to be executed when an EDMA interrupt is raised.

EDMA ISR: installs an ISR to be called when an EDMA interrupt is raised.

Config EDMA: it configures the EDMA for serial communications, ADC and DAC. The EDMA blocks are used to create linked EDMA events for both receive and transmit side. Also it is used for setting up an EDMA channel event or EDMA reload table.

Start System: it adds initialization to the model start function.

System enable: it adds enable code to the model start function.

Model Header: it adds include file directives and typedef statements to the model header file.

Model source: adds variable and function declarations to the model source code file.

In addition to the blocks mentioned above, a handwritten C-code must be added to the project for I) declaration of EDMA buffers, II) body of functions for registers configuration, III) interrupt service routines and IV) I/O read/write functions. The path of the C-code and header files brings in Board Info of C6000 Target Preference block. So the Simulink environment can use this file in compilation procedure for building a project in Code Composer Studio (CCS). Furthermore, it is necessary to add some virtual I/O ports in model, which represent a pointer to the signal buffer name to communicate with the algorithm sections.

IV. DSP FIRMWARE VERIFICATION USING SIMULINK AND RTDX

Historically engineers have used a number of different ways to verify their DSP designs once they had a successful compilation, which in itself can fee like a big achievement.

RTDX stands for Real-Time Data Exchange and is a data communications technology developed by Texas Instruments (TI) for sending and receiving data between the DSP and Code Composer Studio (CCS) over a JTAG (Joint Test Action Group) interface [7]. Engineers use RTDX as a way to debug and test their DSP designs in-situ with real data. The Mathworks introduced an improved RTDX capability that allows the use of RTDX without writing separate scripts.

In this project we have mostly benefited from the advantages of RTDX through Simulink. To have an efficient and complete DSP and Simulink data exchange procedure, two models must be developed I) Target model or a model for hardware implementation and II)Host model or a model for verification [3].

In target model some RTDX channels must be assigned to desired variables. Target model can be implemented on the hardware. In host model, by the proper path allocation of .out file and project file, the previous assigned channel will be opened and the designer would have the real-time access to desired variables.

In HV modem, the received QAM constellation-points have been assigned for real-time visualization via BlackhawkUSB560m JTAG Emulator (capable of high-speed RTDX). These points contain all the necessary information for a QAM communication system behavioral validation (Fig. 3). So, HV modem performance was easily evaluated and verified by means of RTDX between C6713 DSP and Simulink.

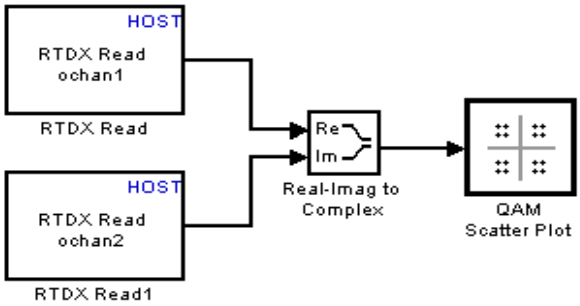

Fig.3. Host model in Simulink for visualization of received QAM-constellation through RTDX channels.

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V. HV MODEM PROTOCOLS

Beyond physical layer of each communication system several protocol layers can be used to guarantee a reliable, high capacity and secure link. As the HV modem is one of the parts of a digital PLC system only reliability is the main concern.

To define the logical behavior of the HV modem, stateflow charts have been employed. These charts define state machines that can be used in the Simulink environment.

At the present version of the HV modem three important startup and running protocols have been prepared.

If the HV modem receives constant amplitude zero auto correlation (CAZAC) sequence correctly, which is a periodic training sequence for fast equalizer convergence [8], then modem will pass through to its normal operation. Otherwise it remains in training mode and handshakes once more. This startup protocol entitled as data terminal ready (DTR).

The second protocol known as data carrier detection (DCD), determines the receiver activation or inactivation mode. Activation or inactivation depends on the incoming signal power level.

The last needed protocol is to identify some undesired faults which may happen during transferring data between modems like link disconnection. It has been also considered in HV modem.

Besides the behavioral protocols, High-level Data Link Control (HDLC) has been considered for HV modem to provide a reliable data communication between two modems. Its most prominent feature is that it can transmit any types of bit stream transparently. HDLC supports point-to-point link only and does not support point-to-multipoint link. HDLC supports neither IP address negotiation nor authentication. HDLC can only be encapsulated on synchronous link. A synchronous /asynchronous interface can also apply HDLC provided that it works in synchronous mode. An HDLC frame is composed of flag field, address field, control field, information field and checksum field.

The data and voice multiplexer (MUX) unit in a PLC system configures data in HDLC framing format.

VI. PROFILING AND OPTIMIZING GENERATED CODE

After verification, any projects need to be optimized for maximum execution speed or code size. For instrumentation of the generated code the used CPU cycles of the core part (CPU load) are counted as a measure for the mean execution time.

In CCS four levels of compiler optimizations are available, with -o3 to invoke the highest level of optimization. Level 0 allocates variables to registers. Level 1 performs all level 0 optimizations, eliminates local common expressions, and removes unused assignments. Level 2 performs all the level 1 optimizations plus loop optimizations and rolling. Level 3 performs all level 2 optimizations and removes functions that are not called. There are also compiler optimizations to minimize code size (with possible degradation in execution speed).

Besides compiler optimization settings, Simulink provides additional optimization procedure which enable designer to exactly revise the most time consuming algorithms. The code profiler in the Target for TI C6000, measures the execution time of code segments generated by individual subsystems. A code profile report helps algorithm developer identify segments of generated code that may benefit from additional optimization. In many cases, the generated code is fast and efficient enough to be used in final production [3].

All optimization levels via CCS compiler and Simulink options have been realized for HV modem.

VII. HV MODEM HARDWARE

The hardware of HV modem has two major parts: the main card and daughter card for peripheral interface as can be observed in fig. 4.

At the heart of main card, there is a floating point TI DSP processor. A floating-point processor is utilized to minimize the time required to convert simulation software into real-time code. The processing power of this DSP is enough to minimize the hand optimization effort for rapid prototyping.

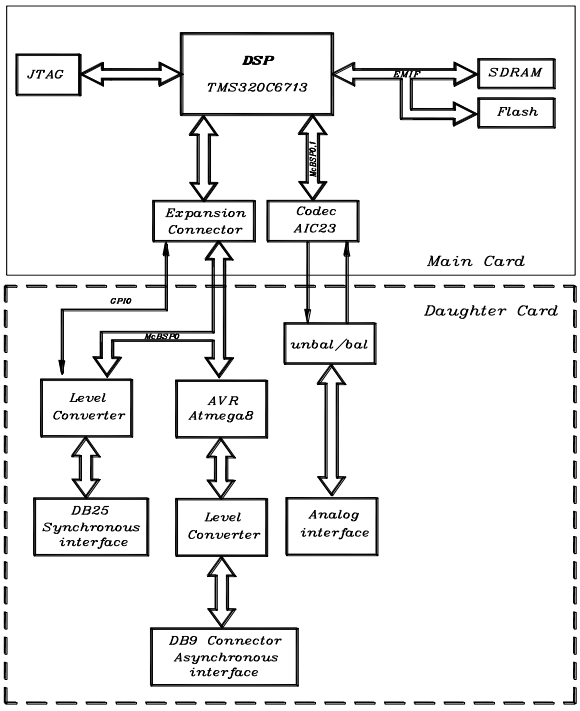

Fig. 4. HV modem hardware sections. Main card (upper) for algorithm development and daughter card (lower) for peripheral interface.

The C6713 DSK is a low-cost standalone development platform that enables users to evaluate and develop applications for the TI C67xx DSP family [9].

The heart of the DSK C6713 is the advanced VLIW architecture floating point digital signal processor TMS320C6713 from Texas Instruments. This RISC architecture DSP provides 8 instruction units which operate in parallel, yielding a maximum performance of 2400 MIPS, 1800 MFLOPS with a clock rate of 300MHz. Up to 256Kbytes internal memory and a two level cache architecture (64Kbytes L2 cache, 4Kbytes L1 program cache and 4Kbytes L1 data cache) guarantee the memory bandwidth required to sustain high data throughput [9].

Also the DSK board includes 8MB of synchronous dynamic random access memory (SDRAM) and 256KB of non-volatile Flash memory [9].

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The DSK includes a 32-bit stereo codec TLV320AIC23 (AIC23) for analog input and output. It connects to a 12-MHz system clock. Variable sampling rates from 8 to 96 kHz can be set readily.

Daughter card standard expansions are also provided on the DSK board.

The DSK C6713 board uses two crystal oscillators. One of them is a DSP clock source and the other is used for JTAG emulator section and codec. In HV modem, we have mixed both crystal oscillators for having synchronization between interrupts of EDMA buffers of serial data communication interface and codec.

The daughter card for peripheral interface will be placed on top of the DSK board and use the DSK signals through the expansion connectors. It contains an AVR micro controller for converting asynchronous data to synchronous data format, RS232 level converters for serial data communication, two transformers for attaining matching and balanced analogue interface and 48VDC/5VDC power supply converter.

VIII. HV MODEM EXPERIMENTAL TEST AND RESULTS

To test and evaluate the performance of HV modem, three different experimental methods have been applied.

First, it has been examined in analog loop back fashion. In this criterion, a text file has been imported to modem and the received file has been saved. By a simple comparing between received and sent file, the accurate operation of modem was confirmed.

Since the HV modem is the main part of a digital PLC system, as the second experimental work, a MUX for data interface and a digital PLC system were used to verify the operation status of modem. An extenuative channel emulates the real 63KV line here. Again by comparing between received and sent file and additionally by testing the quality of voice, the modem accurate process has been proved.

For the third evaluation approach, the designed HV modem has been installed in two 63KV substations. At this step, perfect modem operation is the main goal of HV modem project. Here, the bit-error rate (BER) indicates modem functionally. By using Acterna E1 and Data Tester EDT-135, BER=10e-4 has been obtained in real high voltage power line.

Low signal to noise ratio (SNR) is another factor that can constrain modem desired functionality. For HV modem if the SNR value is below 20dB, the error rate will increase severely.

As discussed in previous section, CPU load is a measure in DSP for algorithms process mean execution time. The maximum CPU load for whole HV modem parts is about 85% with a clock rate of 216MHz. It is probably comparable to optimized handwritten code.

Because of this modular, systematic and rapid design, implementation, verification and optimization method, the HV modem algorithms and protocols will be easily upgradeable.

IX. CONCLUSION

We have efficiently designed, systematically implemented, simply verified and fragmentally optimized a HV modem as the main part of a digital PLC system. All the modem components have been developed in Simulink for simulation and finally for hardware implementation. By means of Simulink and its powerful toolboxes and Blocksets along with CCS, an integrated platform has been provided for signal processing engineers.

For Simulink model of HV modem, all signals are frame-based and it has fixed-step and discrete solver options which are appropriate for an achievable and efficient hardware realization. Moreover, Legacy code integration capability through Simulink, simplifies initialization, configuration and implementation of any custom device driver on Texas Instruments DSP platform.

Although HV modem is a reconfigurable communication system which means any change and modification can be effortlessly done in a short time; however, additional options are needed to have hardware-specific and a user-friendly modem. Now, we are focusing on developing a special purpose hardware which fulfills the desired requirements and concentrating on adding a parameter set menu through graphical user interface. Moreover, adaptive rate selection depends on line conditions like SNR level; bandwidth and so on is another feature that will be considered for future version of HV modem.

ACKNOWLEDGMENT

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