CNT – A Solution for Interconnects

Sandeep Dhariwal, Vijay K. Lamba, Ritu Vijay

***Abstract*--In this paper we have studied the properties of CNT as interconnects and calculated the parameters to analyse our results through table and plots. Due to their excellent electrical properties and small size, metallic carbon nanotubes (CNTs) are promising materials for interconnect wires in future integrated circuits. Simulations have firmly established CNTs as strong contenders for replacing or complementing copper interconnects. As copper wires are scaled down to narrow dimensions to keep up with the miniaturization of the transistors according to Moore's Law, they suffer from adverse narrow-width effects degrading the chip performance. In the long term, the introduction of another interconnects material as a replacement for copper might be the solution. In this review paper, CNTs offer great promises as alternative interconnect materials.**

***Index Terms*— CNT, SWCNT, MWCNT, RLC Model.**

I. INTRODUCTION

The resistance of copper interconnects, with cross-sectional dimensions of the order of the mean free path of electrons (~40 nm in Cu at room temperature) in current and imminent technologies [1], is increasing rapidly under the combined effects of enhanced grain boundary scattering, surface scattering and the presence of the highly resistive diffusion barrier layer [1, 2]. Carbon nanotubes have recently been proposed as a possible replacement for metal interconnects in future technologies [4, 5]. Because of their extremely desirable properties of high mechanical and thermal stability, high thermal conductivity and large current carrying capacity [6, 7, 8], CNTs have aroused a lot of research interest in their applicability as VLSI interconnects of the future. However, the high resistance associated with an isolated CNT (greater than 6.45 KΩ) [9] necessitates the use of a bundle (rope) of CNTs conducting current in parallel to form an interconnection [4, 5]. CNTs are also classified into single-walled and multi-walled (comprising multiple concentric cylindrical shells) nanotubes. Although multi-walled CNTs (MWCNTs) are predominantly metallic, it is difficult to achieve ballistic transport over long lengths with them [10, 11]. Single-walled CNTs (SWCNTs) on the other hand have electron mean free paths of the order of a micron [9]. Hence, in the domain of interconnects, metallic SWCNTs are the preferred candidates.

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II. TRENDS IN VLSI TECHNOLOGY

The resistivity of copper interconnects, with cross-sectional dimensions of the order of the mean free path of electrons (~40 nm in Cu at room temperature) in current and imminent technologies [14], is increasing rapidly under the combined effects of enhanced grain boundary scattering (Fig. 1) [12, 15]. The steep rise in parasitic resistance of copper interconnects not only increases interconnect delay at the global level but also at the local level [13]. More importantly, in combination with the decreasing thermal conductivity of low-k dielectrics and increasing current density

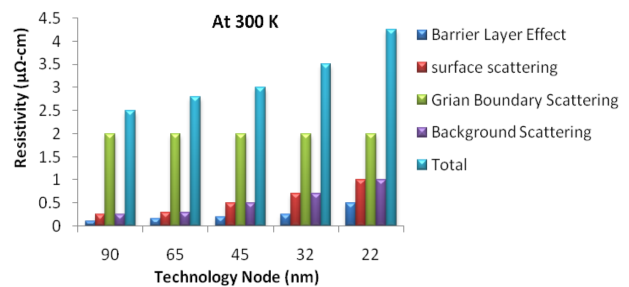

Fig 1: Scaling of metal resistivity for the ITRS intermediate tier wires (at 300K), mainly as a result of the increasing impact of surface and grain boundary scattering of electrons [12]. The impact is even higher for local tier wires and vias (or contacts) that have the smallest cross-sectional dimensions among all on-chip interconnects.

demands from small dimension interconnects, the rising Cu resistivity also poses a reliability concern due to Joule heating induced significant metal temperature rise [12]. The large metal temperature rise, which exponentially degrades interconnect electromigration (EM) lifetime, severely limits the maximum current carrying capacity of future Cu interconnects as shown in fig. 2. As requirements increase, it is increasingly necessary that interconnect be considered as part of a system that includes the package and the silicon chip to satisfy the total technology need for the IC.

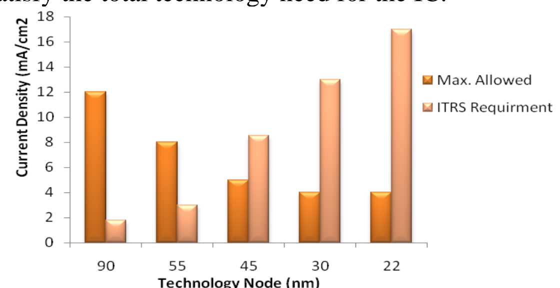

Fig 2: Maximum allowed current density (duty ratio=0.001) in local vias from self-consistent electromigration lifetime estimation vs. the ITRS (2003) requirement for current density in local vias, even with most optimistic scaling scenario for via height at various nodes [13].

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The increasing RC delay is one of the most crucial parameters especially for high performance products. This is a major factor for many digital applications; capacitive coupling in the local and intermediate levels is a highly sensitive issue for low power applications [72]. The use of 3D interconnects and optical interconnects might also be used with multiple wavelengths in a single waveguide (wavelength-division multiplexing (WDM) to provide not only higher bandwidth density for global interconnects

III. LIMITATIONS OF COPPER

To understand the trend of increasing resistivity, we look at the ITRS roadmap [18] and some of the past works [17]. From ITRS reports [18], we find that the copper resistivity for future technologies is increasing at a very fast rate as shown in Figure 3. We find that, the increase in resistivity is not much when we move from 90nm to 32nm technology node, but as

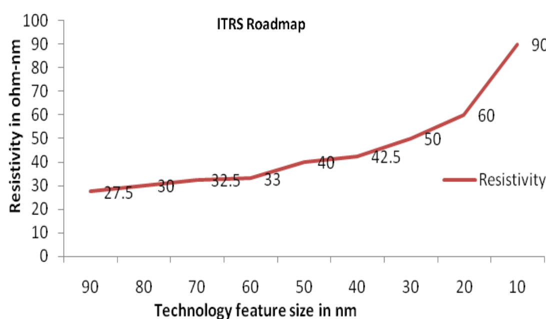

Fig 3: Resistivity increase from ITRS roadmap. There is a steep increase in resistivity as we move into 32nm and lower technology node.

we reduce the feature size further from 32nm, we see a sharp resistivity increase. Therefore, even though wire length is getting smaller, but decreasing cross section area and increasing resistivity resulting in higher interconnect delay, which in turn leads to serious architectural design concerns while designing memory architecture [16] and multicore systems [19]. As per ITRS predictions [20], for nanometer size gate lengths interconnect delay is mostly affected by resistive and capacitive parasitic. Along with electron mean free path grain boundary, surface scattering [21, 22], another effect of dimension scaling is increase in current density. The increased heating due to the rise in power dissipation assists electro migration.

IV. INTRODUCTION TO CNTS AS INTERCONNECTS

Carbon nanotubes have been proposed as solutions to many problems in various industries. Their high electrical and thermal conductivity, as well as their ability to be deposited in either metallic or semiconducting states, has attracted interest for possible applications in interconnect structures. The basic structure of a CNT—as a rolled-up graphene sheet to form a SWCNT, or several concentric tubes to form a multiwalled CNT (MWCNT. Changing the direction of roll-up leads to different "chiralities," which are identified by the chiral indexes (m, n) (when either m or n is zero it is called zigzag chirality, m = n is called armchair, while all other nanotubes are called chiral), figure 4. SWCNTs are metallic when the difference between the chiral indexes is an integer multiple of 3 (m − n = 3i), and are semiconducting otherwise.

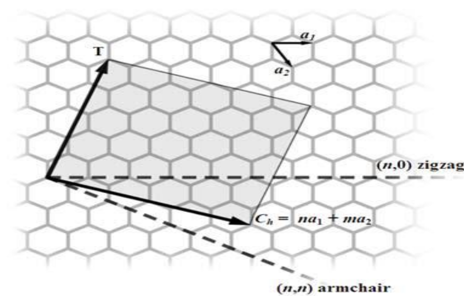

Fig 4: Single Graphene Sheet

CNTs have aroused major research interest in their applicability as very-large-scale integration (VLSI) interconnects for future generations of technology because of their desirable properties such as large electron mean free paths, mechanical strength, high thermal conductivity, and large current carrying capacity. As interconnect dimensions scale and copper resistivity increases due to size effects, CNT interconnect become more attractive.

A. Classification of Carbon Nano Tubes

Depending on the direction in which CNTs are rolled up (chirality), they demonstrate either metallic or semi-conducting properties. In fact, nanotubes come in a variety of forms: long, short, single-walled, multi-walled, open, closed, with different types of spiral structure, etc. However, SWNTs show a strong tendency to bundle up into a 1-D.

1. Single Wall Carbon Nanotube

Single-walled carbon nanotubes (SWNTs) are nanometer-diameter cylinders consisting of a single graphene sheet wrapped up to form a tube. SWCNTs consist of only one graphene shell, and their diameter may vary from 0.4 nm to 4 nm with a typical diameter of 1.4 nm [23, 24]. Since their discovery in the early 1990s [31, 32], there has been intense activity exploring the electrical properties of these systems and their potential applications in electronics. Experiments and theory have shown that these tubes can be either metals or semiconductors, and their electrical properties can rival, or even exceed, the best metals or semiconductors known. The first studies on metallic tubes were done in 1997 [33, 34] and the first on semiconducting tubes in 1998 [35]. The remarkable electrical properties of SWNTs stem from the unusual electronic structure of the two-dimensional material, graphene, from which they are constructed [36, 37]. Graphene - a single atomic layer of graphite - consists of a 2D honeycomb structure of sp^2 bonded carbon atoms. The bandgap is predicted to be $Eg = 0.9$ eV/d [nm], where d is the diameter of the tube. Nanotubes can therefore be either metals or semiconductors, depending on how the tube is rolled up. This remarkable theoretical prediction has been verified using a number of measurement techniques. Perhaps the most direct used scanning tunneling microscopy to image the atomic structure of a tube and then to probe its electronic structure[38, 39]. For bundles of SWCNTs, it has been proven experimentally and theoretically that increasing diameter always lowers conductivity [23, 27–29] .

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This is because the number of nanotubes decreases quadratically with increasing diameter whereas electron mean free path increases only linearly with diameter.

2. Multiwall Carbon Nanotube

Metallic carbon nanotubes (CNTs) possess great potential as transmission lines, interconnects or passive components in nanoelectronic circuits, because their current density, thermal stability and mechanical properties greatly surpass those of conventional metal wires. Multi walled carbon nanotubes (MWCNT) consist of concentric CNT cylinders held within each other by van der Waals forces. The distance between shells is approximately 3.4Å, which is the van der Waals distance for two graphite carbon lattices. MWCNTs consist of several concentric graphene cylinders, and their outer diameters may vary from a few to 100 nm [24, 25], and the spacing between the walls is 0.32 nm, the same as the spacing between graphene sheets in graphite [24]. Large diameter semiconductor shells (D >5 nm) have bandgaps comparable to or smaller than the thermal energy of electrons and act like conductors at room temperature [24–26]. The MWCNTs can differ in their chirality and can consist of both semiconducting and metallic nanotubes, figure 5. For a SWCNT with a random chiral angle and a diameter *d,* there is a 66% chance for it to be semiconducting with a bandgap around $Eg \approx 0.7$/rf eV/nm, that *is* $Eg \approx 0.7$ eV for a 1-nm semiconducting SWCNT.

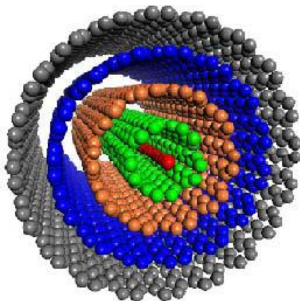

Fig 5: Multi-Walled Carbon Nanotube (MWCNT)

On the contrary, consider a MWCNT with a diameter of 30 nm. Most of the shells will behave metallic even though there are indeed semiconducting (in 66% of the cases) because their bandgap will be negligible with respect to the thermal energy at room temperature $kT = 26$ meV. In other words, the inverse relationship between bandgap and diameter favors large MWCNTs for interconnect applications [40, 41]. For MWCNTs, theoretical models suggest that increasing diameter increases the conductivity of long MWCNTs while decreasing the conductivity of short MWCNTs [28]. However due to the complexity of theoretical modeling and unconventional metallic states of MWNTs, electronic characteristics of MWNTs are not well-understood, and most of what has been found is on their dc properties [7].

V. Advantages of CNTs

CNTs offer several advantages compared to Cu/low-κ interconnects because of their one dimensional nature, the peculiar band-structure of graphene, and the strong covalent bonds among carbon atoms:

(1) HIGHER CONDUCTIVITY (LOWER RESISTANCE): Due to their one-dimensional nature, the phase space for electron scatterings in CNTs is quite limited, and electron mean free path is in the micron range for high quality nanotubes in contrast to 40 nm in bulk copper [49]. The conductivity of densely-packed CNTs is higher than Cu interconnects for large lengths. Conductivity of short CNT bundles, however, is limited by their quantum resistance, the minimum resistance of a quantum wire in the absence of reflections at the CNT-metal electrode interface or scattering along their length. Quantum resistance is a fundamental limit whose value depends on the number of conduction channels. Metallic SWCNTs have two conduction channels, and their quantum resistance is 6.5 kΩ [43, 50].

(2) RESISTANCE TO ELECTROMIGRATION: The strong sp^2 carbon bonds in graphene lead to an extraordinary mechanical strength and a very large current conduction capacity for CNTs; 109 A/cm^2 in contrast to 106 A/cm^2 in Cu before damage or breakdown of the material is observed. Current densities higher than 109 A/cm^2 have also been reported for MWCNTs at high temperature conditions (250^{0}C) [51]. In practice, the maximum current density in CNT interconnects, however, may become limited by the contacts.

(3) THERMAL CONDUCTIVITY: The longitudinal thermal conductivity of an isolated CNT is expected to be very high, on the order of 6000 W/mK, as suggested by theoretical models [52] and extrapolations on measured data from porous bundles [52, 53]. From the experiments of CNT thermal and source bumps for flip-chip high power amplifiers [54], the thermal conductivity of MWCNTs exhibits 1400 W/mK, which is calculated using the experimentally obtained thermal resistance, an area of CNT bundle, and the site density of CNTs.

A. Integration Options

CNTs can potentially replace Cu/low-κ interconnects at most levels of interconnect hierarchy [54] except in places where low-resistance short interconnects are needed. SWCNTs can be integrated for on-chip interconnect applications in the following forms:

(1) SWCNT-BUNDLES: A bundle of densely packed SWCNTs with the same dimensions as Cu/low-κ interconnects with high-quality contacts with the electrodes would be an ideal candidate for replacing Cu/low-κ interconnects to lower the interconnect resistance and address the problem of size effects in copper wires. This integration option provides significant delay improvements for long interconnects where the RC delay is dominant [42, 55–57].

(2) FEW-LAYER SWCNT INTERCONNECTS: A few-layer arrangement of SWCNTs can reduce the capacitance of the CNT-based interconnects by as large as 50% and can significantly decrease the electrostatic coupling between adjacent interconnects. This helps to reduce the delay and power dissipation of local interconnects. This arrangement is particularly interesting for short local interconnects where the delay is dominated by capacitive loading of interconnects and not their resistance [55].

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(3) LARGE-DIAMETER MWCNTS: It has been proven both theoretically and experimentally that all shells within MWCNTs can conduct if proper connections are made to all of them [44, 45, 46, 58]. There are reports of very large mean free paths in high-quality MWCNTs [44, 59], and theoretical models suggest that long large-diameter MWCNTs can potentially outperform Cu and even SWCNTs if the level of disorder in these tubes can be kept as low as those in SWCNTs and all shells can be properly connected to metal contacts [47]. Such MWCNTs would be suitable for semi-global and global interconnects.

(4) GRAPHENE NANORIBBONS (GNR): Graphene nanoribbons can be considered as unrolled CNTs. They share many of the fascinating properties of CNTs while conventional top-down lithography can be used to pattern them [60–64]. There may also be ways to control the chirality and hence their metallic or semiconductor nature[60]. If edges are not perfect, electrons can getscattered at the edges and the mean free path becomes a function of GNR width and propagation mode [60, 64]. This would be a disadvantage for GNRs compared to CNTs that have no edges.

VI. Model For An Isolated SWCNT

The equivalent circuit model for an isolated single-walled carbon nanotube [67] is shown schematically in Fig.6 . The model and its components are explained in detail in the following subsections

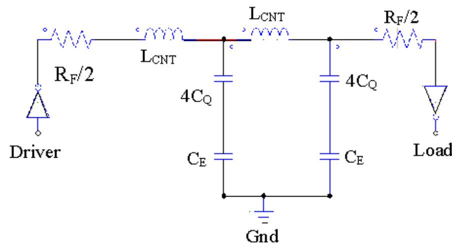

Fig 6: Equivalent circuit model [67] for an isolated SWCNT, length less than the mean free path of electrons, assuming ideal contacts.

A. Resistance of an Isolated SWCNT

The conductance of a carbon nanotube is evaluated using the two-terminal Landauer-Buttiker formula. This formula states that, for a 1-D system with N channels in parallel, the conductance $G=(Ne^2/h)T$, where T is the transmission coefficient for electrons through the sample [9]. Due to spin degeneracy and sublattice degeneracy of electrons in graphene, each nanotube has four conducting channels in parallel ($N=4$). Hence the conductance of a single ballistic single-walled CNT (SWCNT) assuming perfect contacts ($T=1$), is given by $4e^2/h$ = 155 µS, which yields a resistance of 6.45 KΩ [9]. This is the fundamental resistance associated with a SWCNT that cannot be avoided [68]. As shown in Fig. 6, this fundamental resistance (R_F) is equally divided between the two contacts on either side of the nanotube.

$$R_F = \frac{h}{4e^2} \qquad (1)$$

The mean free path of electrons (the distance across which no scattering occurs) in a CNT is typically 1 µm [65, 69, 70]. For CNT lengths less than 1 µm, electron transport is essentially ballistic within the nanotube and the resistance is independent of length (6.45 KΩ). However, for lengths greater than the mean free path, resistance increases with length as shown in Equation 5 [71], where L_0 is the mean free path and L is the length of the CNT. This has also been confirmed by experimental observations [66, 70]. In the equivalent circuit, this additional scattering resistance would appear as a distributed resistance per unit length to account for resistive losses along the CNT length.

$$R_{CNT} = \left(\frac{h}{4e^2}\right)\frac{L}{L_0} \qquad (2)$$

In practice, the observed d.c. resistance of a CNT (at low bias) is much higher than the resistance derived above. This is due to the presence of imperfect metal-nanotube contacts which give rise to an additional contact resistance. As observed in [72], making a reliable contact to a CNT is very challenging, and the resistance arising from these imperfect contacts is often so high that it masks the observation of intrinsic transport properties. The observed resistance for CNTs has typically been in the range of 100 KΩ [72, 73], although in a few cases the lowest observed resistance has been seen to approach the theoretical limit of ~7 KΩ [73]. In the equivalent circuit, this additional imperfect contact resistance would appear in series with the fundamental resistance (R_F) divided equally among the two end contacts as shown for R_F. An important consideration for conductance in nanotubes is its dependence on voltage bias. At high electric fields, current through a nanotube saturates [74]. However, it can easily be shown that a low voltage bias is always applicable in the domain of VLSI interconnect applications, as has also been argued in [75]. In this bias range, the nanotubes display excellent ohmic behavior [74], hence the resistance models described above are valid. The total resistance of a CNT is then expressed as the sum of resistances arising from the above three aspects: the fundamental one-dimensional system (CNT) contact resistance, scattering resistance and the imperfect metal-nanotube contact resistance. Evidently the resistance associated with an isolated CNT is too high for realizing an interconnection. Hence, a bundle/rope of CNTs is needed that has much lower effective resistance and may work effectively as an interconnection.

B. Capacitance of an Isolated SWCNT

The capacitance of a CNT arises from two sources. The *electrostatic capacitance* (C_E) is calculated by treating the

$$C_E = \frac{2\pi\varepsilon}{\ln\left(\frac{a}{d}\right)} \qquad (3)$$

CNT as a thin wire, with diameter 'd', placed a distance 'a' away from a ground plane, and is given by the formula in Equation 3 (C_E per unit length) [17] for $a>2d$. The quantities y and d are shown in Fig. 7. For $d=1$ nm, $a=1$ µm, C_E ≈30 aF/um. This is the intrinsic plate capacitance of an isolated CNT.

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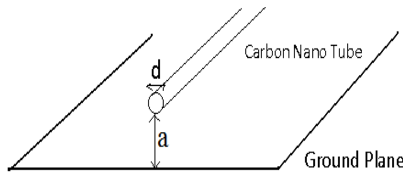

Fig 7: Isolated conductor, with diameter 'd', over a ground plane at a distance 'a' below it.

The *quantum capacitance* (C_Q) accounts for the quantum electrostatic energy stored in the nanotube when it carries current. Due to the Pauli exclusion principle, it is only possible to add electrons into the nanotube at an available quantum state above the Fermi energy level. By equating this energy to an effective capacitance, the expression for the quantum capacitance (per unit length) is obtained as shown in Equation 4 [67], where h is the Planck's constant and v_F is the Fermi velocity. For a carbon nanotube ($v_F \approx$ 8x10^{5}m/s), $C_Q \approx$100aF/µm [67].

$$C_Q = \frac{2e^2}{h\upsilon_F} \qquad (4)$$

As a CNT has four conducting channels as described in the previous sub-section, the effective quantum capacitance resulting from four parallel capacitances C_Q is given by $4C_Q$. The same effective charge resides on both these capacitances (C_E and $4C_Q$) when the CNT carries current, as is true for any two capacitances in series. Hence these capacitances appear in series in the effective circuit model shown in Fig.7.

C. Inductance of an Isolated SWCNT

The inductance associated with an isolated SWCNT can be calculated from the magnetic field of an isolated current carrying wire some distance away from a ground plane, as depicted in Fig. 8. In addition to this *magnetic inductance* (L_M), the *kinetic inductance* is calculated in [67] (following [76]) by equating the kinetic energy stored in each conducting channel of the CNT to an effective inductance. The four parallel conducting channels in a CNT give rise to an effective kinetic inductance of $L_K/4$. The expressions for L_M and L_K are shown in Equation 5 below.

$$L_M = \frac{\mu}{2\pi}\ln\left(\frac{\mathrm{a}}{\mathrm{d}}\right) \qquad (5)$$

$$L_K = \frac{h}{2e^2\upsilon_F} \qquad (6)$$

For *d=1 nm* and *a=1 um*, L_M (per unit length) evaluates to ≈1.4 pH/um. On the other hand, L_K (per unit length) for a CNT evaluates to 16 nH/um. However, the *kinetic inductance* (L_K) in [76] is derived considering no potential drop along the nanotube; hence it must be treated with care. Since $L_K >> L_M$, the inclusion of L_K can have a significant impact on the delay model for interconnects.

VII. Result Analysis

Based upon the isolated RLC model of single wall carbon nano tube, we have extracted the capacitance and inductance parameters and they are analyzed as follows.

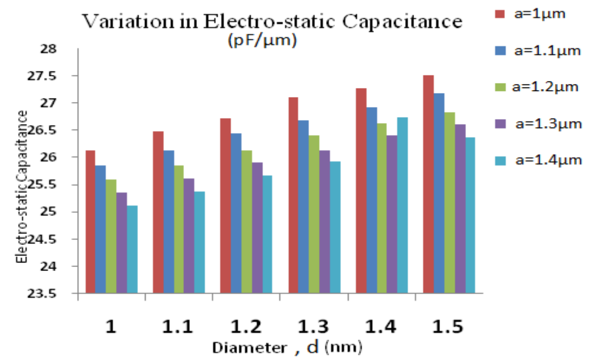

Fig. 8 variation in C_{EQ}

A. CNT Capacitance

We have noticed the changes in the capacitance by changing the different parameters as shown in the fig. 8. From equation 3, electrostatic capacitance (C_{ES}), Diameter 'd', height above ground plane 'a' are plotted at 22nm node technology(a=1µm, d=1nm). From fig. 8, we conclude that Electrostatic Capacitance (C_{ES}) increases with the increase in the diameter of CNT and correspondingly the Electrostatic Capacitance (C_{ES}) decreases with the increase in the height of the SWCNT over the ground plane taken over at each of the diameters.

B. CNT Inductance

From equation 5, Magnetic Inductance (L_M), Diameter 'd', height above ground plane 'a' are plotted at 22nm node technology (a=1µm, d=1nm). From fig.9, we conclude that Magnetic Inductance (L_M) decreases with the increase in the diameter of CNT and correspondingly the Magnetic Inductance increases with the increase in the height of the SWCNT over the ground plane taken over each of the diameters.

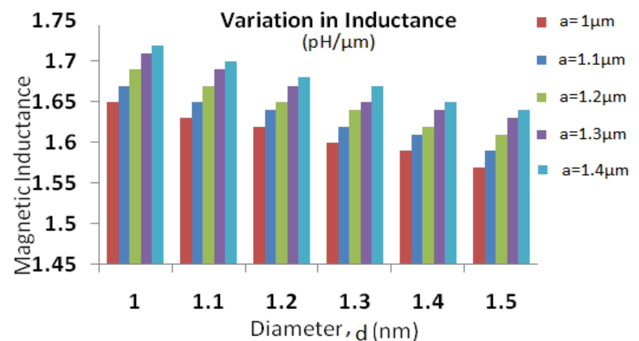

Fig. 9 Variation in Magnetic Inductance

Although thermal challenges are not expected to cause any fundamental problems, because dense single-walled CNT bundle technology is very stable for interconnect applications. Also, lowering of metal nanotube contact resistance will be vital, especially for local interconnect and via applications.

Our next result is based on two node technologies i.e. at 22nm and 18nm. We have calculated the results for the SWCNT Model over a ground plane at two node technology i.e. at 22nm and 18nm node. Various parameters calculated below are obtained from the equations taken above (in the section 6.2, 6.3) in this paper. In the table 1, L_{CNT} is the length of the carbon nanotube.

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All parameters above in the table are for local interconnect. And Various Parameters considered for the results are length of CNT = 1µm, mean free path of electron in the CNT = 1 µm, relative Permittivity (ε_r) = 3.9, fermi Velocity = $8x10^5$ m/s, contact resistance = 50kΩ, diameter of SWCNT = 1nm, height above ground = 1 µm, Voltage = 1Volt at 1GHZ and 10 GHZ. In the above table 1, at 18 nm node technology the biasing voltage and height above the ground plane are voltage = 0.8V at 1GHZ and 10 GHZ and height above ground = 0.7 µm. If we compare both the node technologies in the table 1, we find that as we are going to the miniaturization, delay is more or less almost same but the significant achievement is in the low power dissipation. In today's scenario this is the major parameter at which work is going on. In this review paper we have tried to presents the usefulness of a new interconnect i.e. single wall CNT that will lead the interconnect technology in the future.

Table 1: Comparative Analysis at two different nodes

Parameters (per unit length)		**at 18nm node**	**at 22nm node**
Resistance (R_F/2)	$L_{CNT} \leq$ Mean free path (l_{mfp})	3.2 mΩ	3.2 mΩ
	$L_{CNT} >$ Mean free path (l_{mfp})	32 mΩ	32 mΩ
Capacitance (C_{EQ})		30 aF	28.6 aF
Inductance ($L_{K'}$)		4 nH	4 nH
Delay (τ)	$L_{CNT} \leq$ Mean free path (l_{mfp})	1 nsec	1 nsec
	$L_{CNT} >$ Mean free path (l_{mfp})	1.7 nsec	1.6 nsec
Power Dissipation	freq. = 1Ghz	19.2 nWatt	28.6 nWatt
	freq. = 10Ghz	192 nWatt	286 nWatt

VIII. Conclusion

In this paper, we have taken an overview of new trends of interconnects in VLSI technology along with their limitation. Use of CNTs as an interconnect is the best possible method in nano-scale based devices as analyzed through ITRS roadmap plots. Classification of Carbon Nano Tubes and their advantages are also studied. Delay is the main factor in today's devices and systems. We have noted that local interconnect delay is smaller as compared to intermediate and global interconnect delay. Although We have studied various parameters of bundle of SWCNTs eg. Resistance, Conductance and Inductance but the main focus is on the parameter extraction of SWCNT over a ground plane. We did a comparative analysis over two nodes (18nm and 22nm) technology to compare the various parameters. We can see that power dissipation is reduced in the 18nm node technology and now a day's low power dissipated devices are in high demand as we are moving towards the nano-scale based technology.

IX. Acknowledgments

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