A Multilevel Inverter for Grid Connected Photovoltaic System by employing PID Controller

R.Anand, G.Ashok Kumar

Abstract - This paper presents a single phase five level photovoltaic (PV) inverter topology for grid connected PV systems with a novel Pulse Width Modulated (PWM) control scheme. Two reference signals identical to each other with an offset equivalent to the amplitude of the triangular carrier signal were used to generate PWM signals for the switches. A digital Proportional-Integral- Derivative (PID) current control algorithm is implemented in DSP TMS320F2812 to keep the current injected into the grid sinusoidal and to have high dynamic performance with rapidly changing atmospheric conditions. The inverter offers much less total harmonic distortion and can operate at near-unity power factor. The proposed system is verified through simulation and is implemented in a prototype, and the experimental results are compared with that with the conventional single phase three level grid connected PWM inverter.

Index terms - Grid connected PV system, Single phase five level inverter, MPPT system and Proportional-Integral-Derivative (PID) Controller.

I. INTRODUCTION

The Demand for renewable energy has increased significantly over the years because of shortage of fossil fuels and greenhouse effect. Among various types of renewable energy sources, solar energy and wind energy have become very popular and demanding due to advancement in power electronics techniques. Photovoltaic (PV) sources are used today in many applications as they have the advantages of being maintenance and pollution free. Solar electric energy demand has grown consistently by 20% to 25% per annum over the past 20 years, which is mainly due to the decreasing costs and prices. This decline has been driven by the following factors

1) An increasing efficiency of solar cells
2) Manufacturing technology improvements
3) Economies of scale

PV inverter, which is the heart of a PV system, is used to convert dc power obtained from PV modules into ac power to be fed into the grid. Improving the output waveform of the inverter reduces its respective harmonic content and, hence, the size of the filter used and the level of Electromagnetic Interference (EMI) generated by switching operation of the inverter. In recent years, multilevel inverters have become more attractive for researchers and manufacturers due to their advantages over conventional three level PWM inverters. They offer improved output waveforms, smaller filter size and lower EMI, lower Total Harmonic Distortion (THD).

The three common topologies for multilevel inverters are as follows:

1) Diode clamped (neutral clamped)
2) Capacitor clamped (flying capacitors)
3) Cascaded H-bridge inverter.

In addition, several modulation and control strategies have been developed or adopted for multilevel inverters, including the following multilevel sinusoidal (PWM), multilevel selective harmonic elimination, & Space Vector modulation. A typical single phase three-level inverter adopts full-bridge configuration by using approximate sinusoidal modulation technique as the power circuits. The output voltage then has the following three values: zero, positive ($+V_{dc}$), and negative ($-V_{dc}$) supply dc voltage (assuming that V_{dc} is the supply voltage). The harmonic components of the output voltage are determined by the carrier frequency and switching functions. Therefore, their harmonic reduction is limited to a certain degree. To overcome this limitation, this paper presents a five-level PWM inverter whose output voltage can be represented in the following five levels: zero, $+1/2V_{dc}$, V_{dc}, $-1/2V_{dc}$ and $-V_{dc}$. As the number of output levels increases, the harmonic content can be reduced. This inverter topology uses two reference signals, instead of one reference signal, to generate PWM signals for the switches. Both the reference signals V_{ref1} and V_{ref2} are identical to each other, except for an offset value equivalent to the amplitude of the carrier signal $V_{carrier}$, as shown in Fig.1.

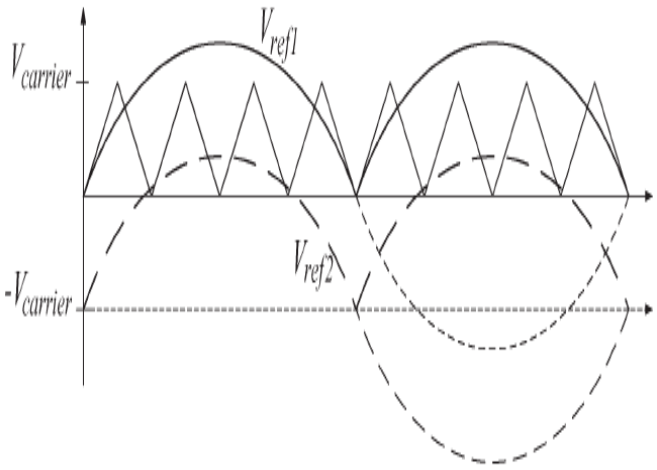

Fig.1 Carrier and reference signals

Because the inverter is used in a PV system, a PID current control scheme is employed to keep the output current sinusoidal and to have high

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dynamic performance under rapidly changing atmospheric conditions and to maintain the power factor at near unity. Simulation and experimental results are presented to validate the proposed inverter configuration.

II. FIVE LEVEL INVERTER TOPOLOGY AND PWM LAW

The proposed single phase five level inverter topology is shown in Fig.2. The inverter adopts a full-bridge configuration with an auxiliary circuit. PV arrays are connected to the inverter via a dc–dc boost converter. Because the proposed inverter is used in a grid-connected PV system, utility grid is used instead of load. The dc–dc boost converter is used to step up inverter output voltage V_{in} to be more than √2 of grid voltage Vg to ensure power flow from the PV arrays into the grid.

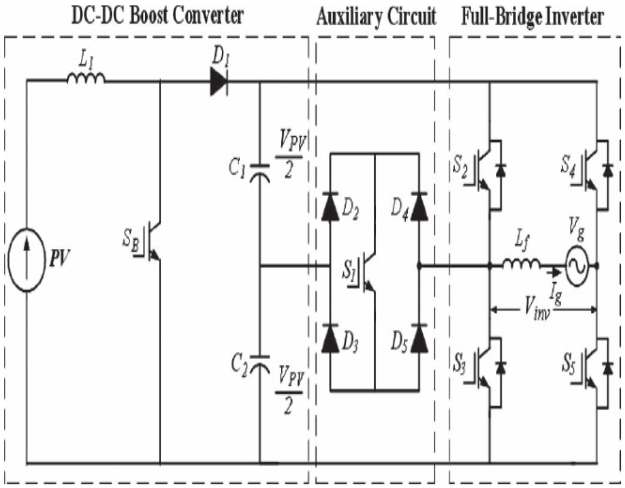

Fig.2 Single phase five level inverter topology

A filtering inductance Lf is used to filter the current injected into the grid. The injected current must be sinusoidal with low harmonic distortion. In order to generate sinusoidal current, sinusoidal PWM is used because it is one of the most effective methods. Sinusoidal PWM is obtained by comparing a high frequency carrier with a low frequency sinusoid, which is the modulating or reference signal. The carrier has a constant period; therefore, the switches have constant switching frequency. The switching instant is determined from the crossing of the carrier and the modulating signal.

III. OPERATIONAL PRINCIPLE OF THE PROPOSED INVERTER

Because PV arrays are used as input voltage sources, the voltage produced by the arrays is known as V_{arrays}. V_{arrays} boosted by a dc–dc boost converter to exceed √2Vg. The voltage across the dc-bus capacitors is known as V_{pv}. The operational principle of the proposed inverter is to generate five level output voltage, i.e., 0, $+V_{pv}/2$, $+V_{pv}$, $-V_{pv}/2$, and $-V_{pv}$. Proper switching control of the auxiliary circuit can generate half level of PV. supply voltage, i.e., $+V_{pv}/2$ and $-V_{pv}/2$. Two reference signals V_{ref1} and V_{ref2} will take turns to be compared with the carrier signal at a time. If V_{ref1} exceeds the peak amplitude of the carrier signal $V_{carrier}$, V_{ref2} will be compared with the carrier signal until it reaches zero. At this point onward, V_{ref1} takes over the comparison process until it exceeds Vcarrier.

IV. CONTROL SYSTEM ALGORITHM AND IMPLEMENTATION

The feedback controller used in this application utilizes the PID algorithm. As shown in Fig., the current injected into the grid, also known as grid current I_g, is sensed and fed back to a comparator which compares it with the reference current I_{ref} . I_{ref} is obtained by sensing the grid voltage and converting it to reference current and multiplying it with constant m. This is to ensure that I_g is in phase with grid voltage V_g and always at near-unity power factor. One of the problems in the PV generation systems is the amount of the electric power generated by solar arrays always changing with weather conditions, i.e., the intensity of the solar radiation.

A maximum power point tracking (MPPT) method or algorithm, which has quick-response characteristics and is able to make good use of the electric power generated in any weather, is needed to solve the aforementioned problem. Constant m is derived from the MPPT algorithm. The perturb and observe algorithm is used to extract maximum power from PV arrays and deliver it to the inverter. The instantaneous current error is fed to a PID controller. The integral term in the PID controller improves the tracking by reducing the instantaneous error between the reference and the actual current. The resulting error signal u which formsV_{ref1} and V_{ref2} is compared with a triangular carrier signal and intersections are sought to produce PWM signals for the inverter switches.

TABLE- I Inverter Output Voltage during S_1-S_5 Switch ON and OFF

S_1	S_2	S_3	S_4	S_5	V_{in}
ON	OFF	OFF	OFF	ON	$+V_{pv}/2$
OFF	ON	OFF	OFF	ON	+Vpv
OFF	OFF	OFF	ON	ON	0
ON	OFF	OFF	ON	OFF	-Vpv/2
OFF	OFF	ON	ON	OFF	-Vpv

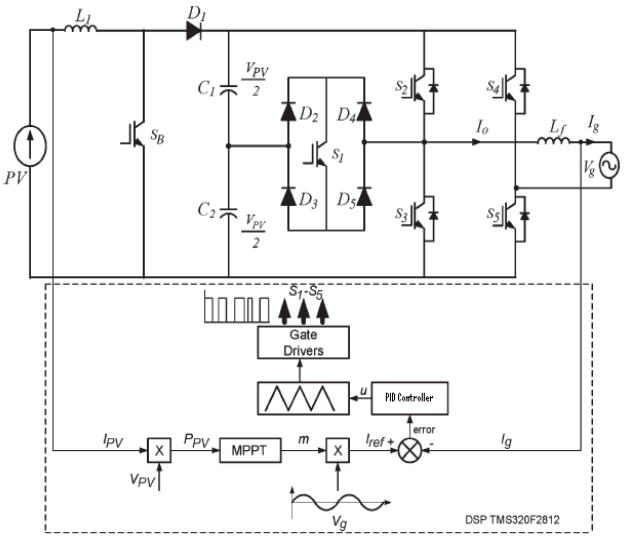

Fig.3 Five level inverter with control algorithm implemented in DSP TMS320F2812

Implementing this algorithm using a DSP requires one to transform it into the discrete time domain. Trapezoidal sum approximation is used to transform the integral term into the discrete time domain because it is the most straightforward technique. The proportional term is directly used without approximation. The Simulation result for five level inverter for grid connected PV system is obtained and as show in Fig .4, Fig .5 & Fig .6.

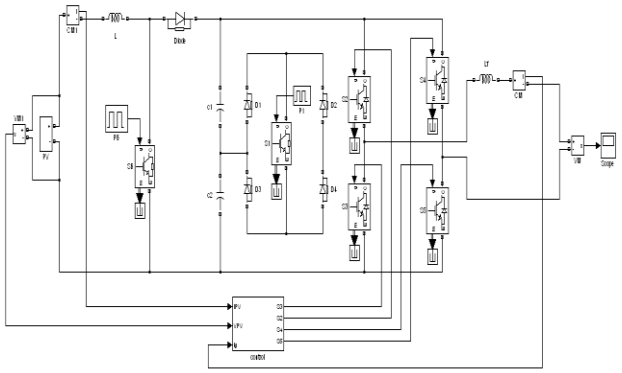

Fig.4 Simulink diagram for five level inverter

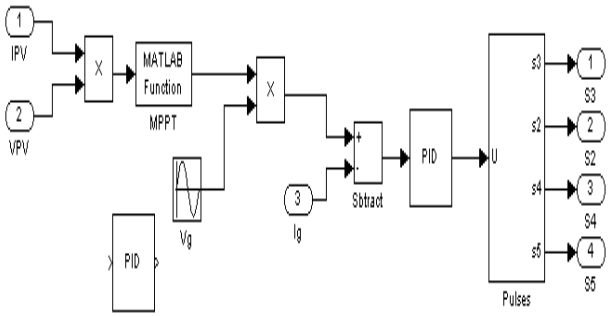

Fig.5 MPPT technology

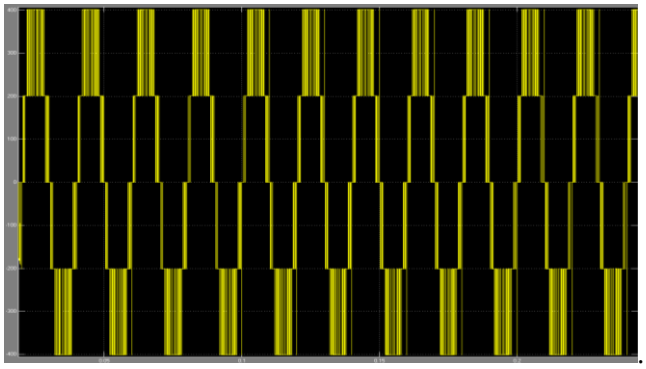

Fig.6 Simulation five level output voltage for grid connected PV System.

V. CONCLUSION

This paper presented a single phase multilevel inverter for PV application. It utilizes two reference signals and a carrier signal to generate PWM switching signals. The circuit topology, modulation law, and operational principle of the proposed inverter were analyzed in detail. A digital PI current control algorithm is implemented in DSP TMS320F2812 to optimize the performance of the inverter.

Experimental results indicate that the THD of the five level inverter is much lesser than that of the conventional three level inverter.Furthermore; both the grid voltage and the grid current are in phase at near-unity power.

The proposed five level diode clamped multilevel inverter has several promising advantages for the use of a three-phase stand-alone photovoltaic system. First, it can convert power from several relatively low dc voltage sources to a higher ac voltage by itself (without transformers or high frequency switching). Second, it increases output voltage levels without any transformer that reduce the losses and weight of the overall system. Third, in case of a five level multilevel inverter operating as a motor drive, it does not require an output filter because high order harmonics are effectively filtered off, owing to the reactance of the induction motor load; therefore, it can produce a high quality output voltage wave with a good harmonic characteristic. Finally, it reduces stresses on power switching devices, resulting in low audio and Radio Frequency (RF) noise and Electromagnetic Interference (EMI), and fewer Electromagnetic Compatibility (EMC) problems, since multilevel inverter operates with a low switching frequency and voltage switching is done for relatively lower voltage levels.

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