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Design and Implementation of OFDM (Orthogonal Frequency Division Multiplexing) using VHDL and FPGA

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Abstract— Orthogonal Frequency Division Multiplexing (OFDM) is a multi carrier modulation technique which divides the available spectrum into many carriers. OFDM uses the spectrum efficiently compared to FDMA by spacing the channels much closer together and making all carriers orthogonal to one another to prevent interference between the closely spaced carriers. OFDM provides high bandwidth efficiency because the carriers are orthogonal to each others and multiple carriers share the data among themselves. The main advantage of this transmission technique is their robustness to channel fading in wireless communication environment. The main objective of this project is to design and implement a base band OFDM transmitter and receiver using FPGA. This project focuses on the core processing block of an OFDM system, which are the Fast Fourier Transform (FFT) block and the Inverse Fast Fourier Transform (IFFT). The work also includes in designing a mapping module, serial to parallel and parallel to serial converter module. The 8 points IFFT / FFT decimation-in-frequency (DIF) with radix-2 algorithm is analyzed in detail to produce a solution that is suitable for FPGA implementation. The FPGA implementation of the project is performed using Very High Speed Integrated Circuit (VHSIC) Hardware Descriptive Language (VHDL). This performance of the coding is analyzed from the result of timing simulation using Xilinx.

Index Terms— FFT, FPGA, IFFT, OFDM, VHDL

I. INTRODUCTION

With the rapid growth of digital communication [5] in recent years, the need for high-speed data transmission has been increased. The mobile telecommunications industry faces the problem of providing the technology that is able to support a variety of services ranging from voice communication with a bit rate of a few kbps to wireless multimedia in which bit rate up to 2 Mbps. Many systems have been proposed and OFDM system has gained much attention for different reasons. Although OFDM was first developed in the 1960s, only in recent years, it has been recognized as an outstanding method for high-speed cellular data communication where its implementation relies on very high-speed digital signal processing. This method has only recently become available with reasonable prices versus performance of hardware implementation.

Since OFDM is carried out in the digital domain, there are several methods to implement the system. One of the methods to implement the system is using ASIC (Application Specific Integrated Circuit). ASICs are the fastest, smallest, and lowest power way to implement OFDM into hardware. The main problem using this method is inflexibility of design process involved and the longer time to market period for the designed chip. Another method that can be used to implement OFDM is general purpose Microprocessor or Micro Controller. Power PC 7400 and DSP Processor is an example of microprocessor that is capable to implement fast vector operations. This processor is highly programmable and flexible in terms of changing the OFDM design into the system. The disadvantages of using this hardware are: it needs memory and other peripheral chips to support the operation. Besides that, it uses the most power usage and memory space, and would be the slowest in terms of time to produce the output compared to other hardware.

Field-Programmable Gate Array (FPGA) is an example of VLSI circuit which consists of a “sea of NAND gates”. This hardware is programmable and the designer has full control over the actual design implementation without the need (and delay) for any physical IC fabrication facility. An FPGA combines the speed, power, and density attributes of an ASIC with the programmability of a general purpose processor will give advantages to the OFDM system. An FPGA could be reprogrammed for new functions by a base station to meet future needs particularly when new design is going to fabricate into chip. This will be the best choice for OFDM implementation since it gives flexibility to the program design besides the low cost hardware component compared to others.

II. METHODOLOGY

The aim is to design an OFDM transmitter and receiver using FPGA [3]. The OFDM signal is generated by implementing the Inverse Fast Fourier Transform (IFFT) function at the transmitter. At the receiver end, the Fast Fourier Transform (FFT) is implemented.

The objective is to use High-Speed-Integrated-Circuit (VHSIC) Hardware Description Language (VHDL) to produce VHDL codes that carry out FFT and IFFT function.

Figure 1 and 2 shows a detailed OFDM transmitter and receiver communications system. In this project, the main focus is in the FFT and IFFT part of the OFDM system [4].

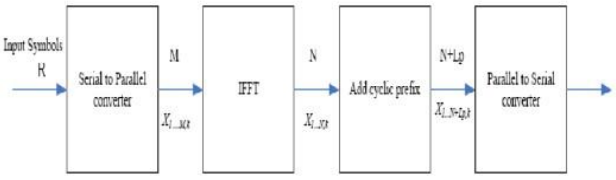

Figure 1: OFDM Transmitter

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The input symbols are input into the transmitter in series at R symbols/second. These symbols pass through a serial to parallel converter and output data on M lines in parallel. The data rate on every M line is R/M symbols/second. A symbol in this parallel stream of data is denoted as Xi, k. The index i refer to which sub channel the symbol belongs to, and i ranges from 1 to M. The k denotes the k-th collection of M symbols. The sub symbol collection from X1,k to XM, k makes up an OFDM symbol.

The M symbols are sent to an Inverse Fast Fourier Transform (IFFT) block that performs N-point IFFT operation. The IFFT transform a spectrum (amplitude and phase of each component) into a time domain signal. An IFFT converts a number of complex data points, of length that is power of 2, into the same number of points in time domain. Each data point in frequency spectrum used for an FFT or IFFT operation is called a bin. The output is N time-domain samples.

In order to preserve the sub-carrier orthogonality and the independence of subsequent OFDM symbols, a cyclic guard interval is introduced. Time and frequency synchronization can be established by means of cyclic extension in the prefix and the postfix period.

In this case, assumed a cyclic prefix of length Lp samples is pre-pended to the N samples to form a cyclically extended OFDM symbol. The cyclic prefix is simply the last Lp samples of the N inverse Fast Fourier Transform output samples.

For example, assumed N=4 and Lp=2. If the outputs of a 4 point inverse Fourier transform is [1 2 3 4]. The cyclic prefix will be [3 4]. The cyclically extended symbol would be [3 4 1 2 3 4]. Therefore, the length of the transmitted OFDM symbol is N+ Lp.

Pre-pending the cyclic prefix aids in removing the effects of the channel at the receiver. ISI can occur when multi path channel cause delayed version of previous OFDM symbol to corrupt the current received symbol. If the value of Lp is greater than or equal to the size of the transmission channel, the ISI will only affect the cyclic prefix.

The actual OFDM symbol will arrive unchanged. The cyclic prefix makes the OFDM symbol appear periodic over the band of interest. The cyclically extended symbols are passed through a parallel-to-serial converter. They are transmitted in series across the channel response of the OFDM symbol with the frequency response of the channel.

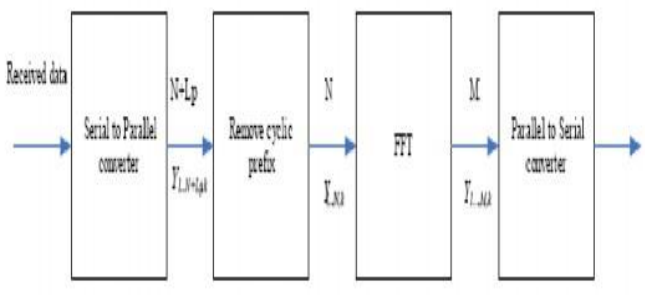

Figure 2: OFDM Receiver

The received symbol is in time domain and it is distorted due to the effect of the channel. The received signal goes through a serial to parallel converter and cyclic prefix removal.

After the cyclic prefix removal, the signals are passed through an N-point fast Fourier transform to convert the signal to frequency domain. The output of the FFT is formed from the first M samples of the output.

III. RESULTS

A. *Simulation Result of Transmitter.*

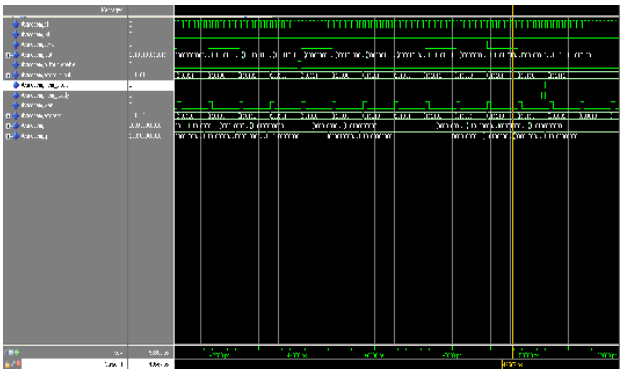

Figure 3: Simulation result of Transmitter.

B. *Simulation Result of Receiver*

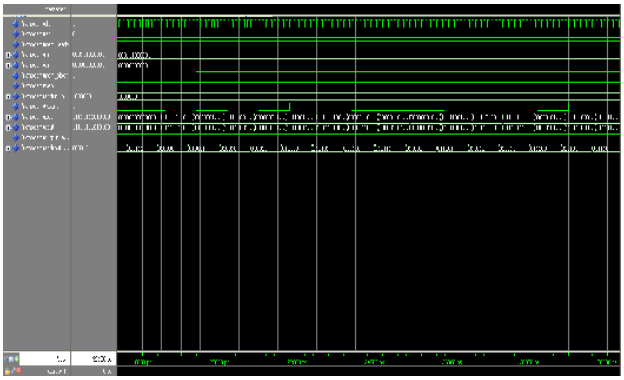

Figure 4: Simulation result of Receiver.

VI. CONCLUSION

The objective is the implementing the core processing blocks of an Orthogonal Frequency Division Multiplexing (OFDM) system, namely the Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (IFFT).

The Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (FFT) have been chosen to implement the design instead of the Discrete Fourier Transform and Inverse Discrete Fourier Transform because they offer better speed with less computational time. These methods requires the odd and even samples inputs are process separately before they are combine to give the final output. The result of the computation is in integer bits which might comprises of real and imaginary components. The decimal value of the output if greater than 0.5 is approximated to 1 and vice versa.

The design implementation is done using VHDL coding. Direct mathematical method is adopted because it is an efficient and optimized method instead of the structural implementation which is based on butterfly operation.

VII. ACKNOWLEDGMENT

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