Sleep Pass Gate Approach for Static Power Reduction in 8*8 Wallace Multiplier

R. Naveen, K. Thanushkodi, C. Saranya

Abstract— As the VLSI technology and supply/threshold voltage continue scaling down, leakage power has become more and more significant in the power dissipation of today's CMOS circuits. The leakage power dissipation is projected to grow exponentially during the next decade according to the International Technology Roadmap for Semiconductors (ITRS).This affects the portable battery operated devices directly. The multipliers are the main key for designing an energy efficient processor, where the multiplier design decides the digital signal processors efficiency. In this paper, a sleep pass gate method is used to reduce the static power dissipation in 8*8 Wallace tree multiplier architecture which has been designed by using 1-bit full adders. This method uses two complementary sleep transistors connected in parallel forming a gate pass structure. In our proposed leakage reduction method, the actual output logic state is maintained in both active and standby mode of operation. The main objective of our work is to calculate leakage power in 8*8 Wallace tree multiplier with sleep pass gate and it is compared with the 8*8 Wallace tree full adder multiplier. The proposed method reduces upto half of the static power dissipation with lesser area and delay.

Index Terms - Static leakage power, Sleep transistor, Subthreshold leakage, Wallace multiplier, 1- bit full adder

I. INTRODUCTION

The multipliers play a major role in arithmetic operations in the digital signal processing applications. Hence the need for low power multipliers has been increased. C.S.Wallace suggested a fast multiplier [1] during 1964 with combination of half adders and full adders. During that period the need for low power designs were not upto the mark, but in coming years the need for compatible and advanced systems made a demand for the new designs of basic circuits with low power, delay and fast working.

Thus the multiplier circuits are redesigned and many researches were made and among them Wallace multiplier with full adder design had showed rapid development in reducing leakage power [2].That is the key for this paper to reduce the total leakage power in 8*8 Wallace multiplier with full adders by using sleep pass gate method.

There are three sources of power dissipation in a digital CMOS circuit. The first source is the logic transitions. In this source, nodes in a digital CMOS circuit transition back and forth between the two logic levels, the parasitic capacitances are charged and discharged [3]. Current flows through the channel resistance of transistors, and electrical energy is converted into heat and dissipated away. This component of power dissipation is proportional to the supply voltage, node voltage swing, and average switched capacitance per cycle. The voltage swing in most cases is simply equal to supply voltage, the dissipation due to transitions varies overall as the square of supply voltage [3].

Short-circuit currents that flow directly from supply to ground when the Pull-Up Network (PUN) and the Pull-Down Network (PDN) of a CMOS gate both conduct simultaneously are the second source of power dissipation. With input(s) to gate stability at their logic levels, only one of the two networks conduct and no short-circuit current flow. But when the output of a gate is changing in response to change in inputs, both PUD and PDN conduct simultaneously for a brief interval. The last source of dissipation is leakage current that flows when inputs and outputs of a gate are not changing. This is termed as static power dissipation.

In olden day's technology the magnitude of leakage current was low and usually neglected. In current trends, the supply voltage is being scaled down to reduce dynamic power and MOS field-effect transistors (MOSFETs) with low threshold voltages (V_{th}) have to be used. This could be inferred as lower the threshold voltage, lower the degree to which MOSFETs in logic gates are turned off and higher is the standby leakage current [3]. Scaling down of V_{th}, leads to an exponential increase in sub- threshold leakage current. Subthreshold leakage current is the drain-to-source leakage current when the transistor is OFF. This happens when the applied gate to source voltage V_{gs} is less than threshold voltage V_{th} of transistor (weak inversion mode).

The Sub-threshold current flows due to diffusion current of minority carriers in the channel of MOSFET [4]. Figure-1 shows the subthreshold leakage trends with deep-submicron technologies.

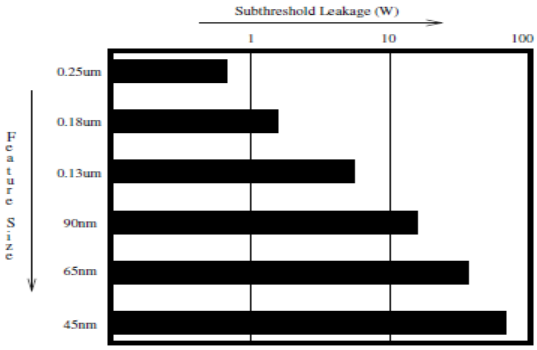

Figure 1: Subthreshold leakage power trends

In our work, we present a circuit level design technique that reduces the leakage power in conventional CMOS circuits. This paper focuses on static power dissipation in standby mode of operation using sleep pass gate. Here static power dissipation is reduced in 8*8 Wallace multiplier with full adder by using sleep pass gate. This paper is organized as follows: section 2 Existing methods, section 3 proposed method, followed by result and comparison in section 4 and conclusion in section 5.

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II. EXISTING METHODS

In this section, we mainly survey the different techniques used to reduce leakage power in 8*8 Wallace tree multiplier. All these techniques and algorithms are effective in reducing leakage power and ultimately all come down to a fundamental set of concepts: dissipation is reduced by lowering supply voltage, voltage swing, physical capacitance, switching activity or by introduction of a high resistance path between V_{DD} and ground.The input vector method by Abdollahi et.al. makes use of dependence of leakage current on the input vector to gate [5]. Additional control logic is used to put the circuit in a low-leakage standby state when it is idle and restored to its original state when reactivated. Upon reactivation, the circuit no longer retains the original state information before going into low-leakage standby state. Thus, to retain original state information, it requires special latches thereby increasing the area of circuit by about five times in worst cases.Another technique for leakage power control is power-gating approach [6] proposed by Agarwal et.al. this turns off the devices by cutting of their supply voltages. Moreover, bulky PMOS and/or NMOS devices (sleep transistors) are introduced in between either supply or ground and circuit. Introduction of sleep transistors creates virtual power and ground rails in the circuit. The sleep transistor is turned on while circuit is in active state and turned off when circuit is in idle mode. This is done with the help of sleep signals.As leakage power varies exponentially with the threshold voltage, it is necessary for sleep transistors to have a high threshold voltage. This leads to use of multiple threshold voltage CMOS (MTCMOS) technology. Douseki et.al.[9] introduced the concept of Multi-Threshold CMOS (MTCMOS) which has emerged as a very popular technique for standby mode leakage power reduction. The transistors of logic gates are low threshold devices and ground is connected to gate through a high threshold voltage NMOS gating transistor. The logical functioning of a gating transistor is similar to that of a sleep transistor. The use of this technique gives rise to existence of reverse conduction paths that reduce noise margin or as a worst case scenario results in complete failure of gates.A variation of MTCMOS technique is the Dual V_{th} technique (DTMOS) [7, 8] which uses transistors with two different threshold voltages. Low threshold transistors are used for gates in the critical paths and high threshold transistors are used for gates which are not on critical path.The 8*8 Wallace tree multiplier with full adder method replaces the full adders in the place of half adders. Hence there is no need for separate final summing system as shown in figure-2 and figure-3. So the total leakage power is reduced [2].

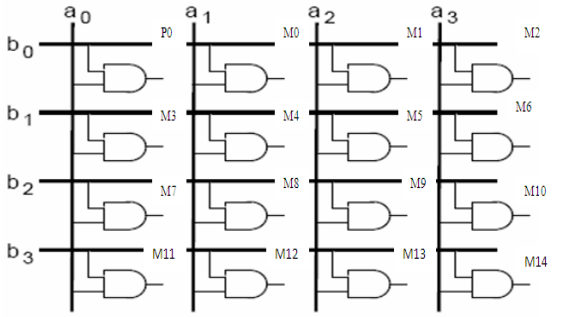

Figure 2: AND gate generating input to multiplier block diagram

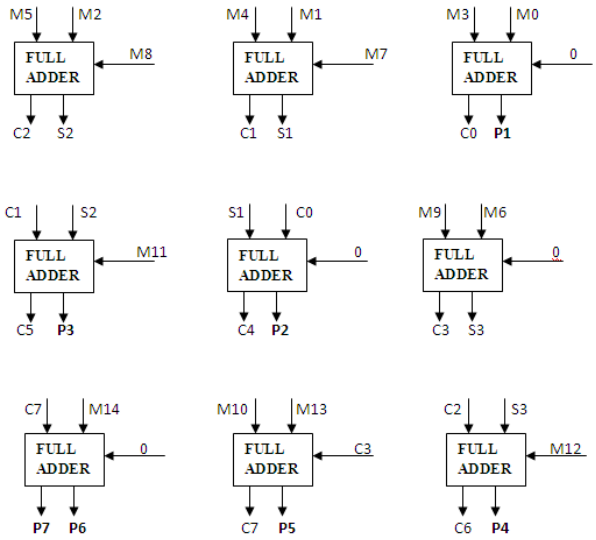

Figure 3: Multiplier block diagram being designed using full adder

Experimental results obtained using proposed method described later in this paper is compared with 8*8 Wallace tree multiplier with full adders.

III. PROPOSED METHOD

In this method the static power dissipation is reduced during standby mode of operation by introducing a high resistance in the path supply to ground by means of a CMOS analog switch. This analog solid-state switch will block or pass a signal level selectively from input to the output. This switch is comprised of a PMOS transistor and NMOS transistor. The control gates are biased in a complementary manner so that both transistors are either in on position or off position. The switches can be implemented either by a single NMOS transistor or PMOS transistor in sleep transistor or pass transistor logic as shown in figure-4. The NMOS transistors pass a strong 0 but a weak 1(threshold voltage drop. High =VDD -V_{thn}) and PMOS transistors passes a strong 1 but a weak 0(threshold voltage drop. Low = V_{thp}). Thus, NMOS switches are best for pull- down network and the PMOS switches are best for pull-up network [11].

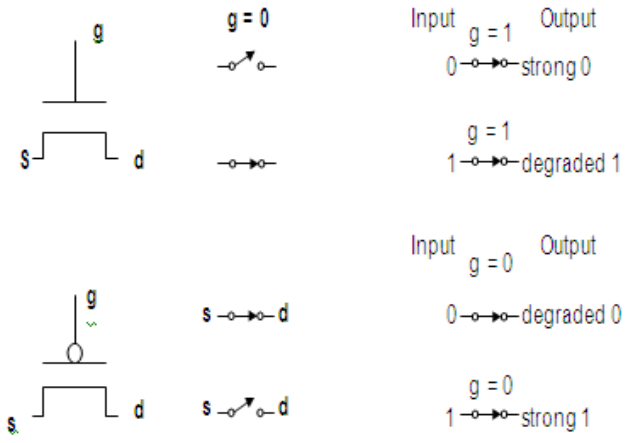

Figure 4: Pass transistor logic

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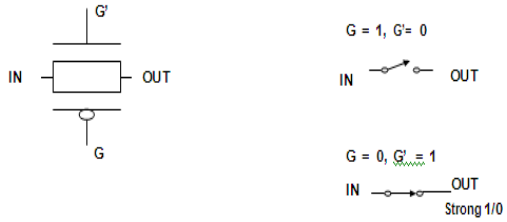

Figure 5: Sleep-Pass gate

The figure-5 represents a pair of complementary MOS transistors connected in parallel known as the CMOS pass gate configuration, which pass both 0 and 1 well. When the voltage on node G is a Logic 1, the complementary Logic 0 is applied to node active-low G' allowing both transistors to conduct and pass the signal at IN to OUT. When the voltage on node active-low G' is Logic 0, complementary Logic 1 is applied to node G, turning both transistors off and forcing a high-impedance condition on both IN and OUT nodes. This high-impedance condition represents third "state" (high, low, or high-Z). Thus, pass gate acts as an open circuit offering high resistance. This design acts as a voltage controlled resistor connecting input and output providing true bidirectional connectivity without degradation of the input signal.

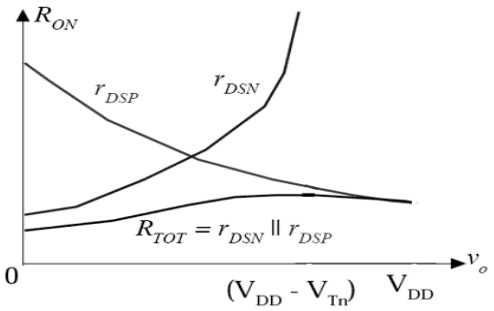

Figure 6: ON resistance of pass gate

The figure-6 plots ON resistance of pass gate as input voltage is swept from GND to VDD, assuming the output voltage closely follows. The effective ON resistance is a parallel combination of two resistances and is relatively constant across full range of input voltages. However the OFF resistance is very high and it is in the range of several mega ohms.

A. Sleep pass gate method

In this section, we describe our new leakage reduction technique, which is termed as "Sleep-Pass gate" approach. This section explains the structure of proposed method as well as, how it operates. In comparison with single sleep transistor (PMOS or NMOS) connected between PUN (Pull up network) and PDN (Pull down network), which pass degraded output. Also, the pass gate is capable of passing logic values 1 and 0 well. In addition to that, output logic state is not lost when the circuit enters from active mode to sleep mode and vice-versa. This seems very attractive in comparison with some of the existing ways to use for lower VDD values and additional transistors to maintain logic state. For example, Martin et.al. propose that some reduced VDD values sufficient to maintain the logic state [10]. The sleep circuit consists of two complementary MOS transistors S1 (PMOS) and S2 (NMOS). The sleep transistors S1 and S2 are connected in parallel to form pass gate configuration between PUN and PDN as shown in figure-7.

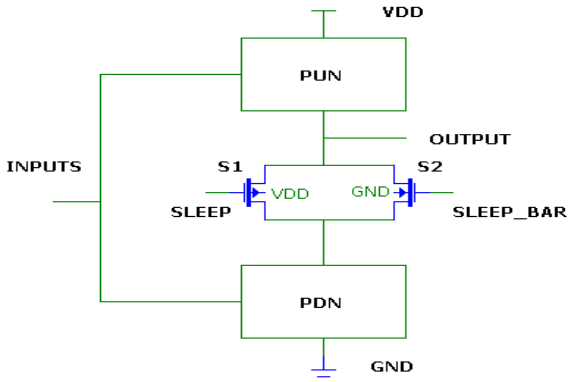

Figure 7: Diagram of proposed method

The two control signals 'sleep' and its complement 'sleep bar' feeds the gates of S1 and S2 respectively. The sleep transistors S1 and S2 are high threshold voltage devices and the logic gate transistors are standard threshold voltage devices. This is only done to provide a well balanced trade-off between high speed and leakage loss. The CMOS circuit output can be drawn either between PUN and sleep circuit or between sleep circuit and PDN.

The working of the 'Sleep-Pass gate' approach is now explained. During the normal (active) mode of operation, 'sleep=0' and 'sleep bar=1'. This makes the transistors S1 and S2 to turn ON and acts as a pass gate. The circuit behaves like a normal CMOS circuit without any hindrance from the sleep circuit. This can be seen from the DC characteristics obtained from HSPICE simulations. The figure-8 shows the DC characteristics of the NAND gate with the proposed method (the input A is fixed at 1 V and B is varied from 0 to 1 V).

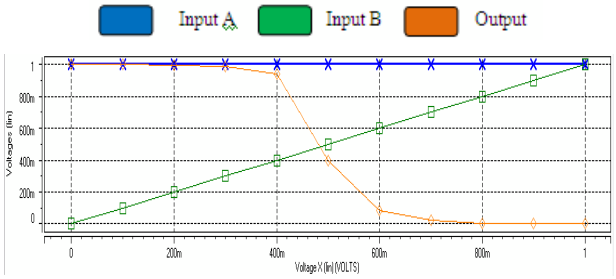

Figure 8: DC characteristic of a 2-input NAND with proposed method

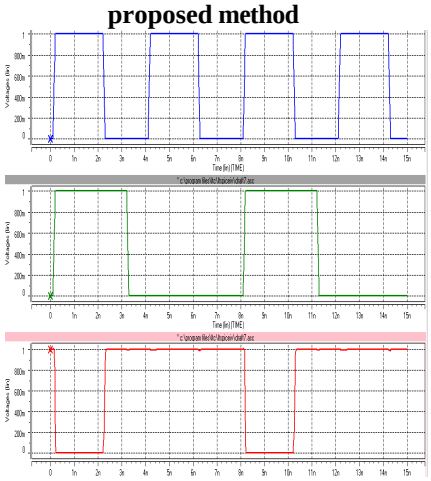

Figure 9: Input – output waveforms of 2-input NAND with proposed method

The ON resistance of the pass gate will be constant and lesser than its OFF resistance, allowing conduction between PUN and PDN. Even though the ON resistance of pass gate is not as high as its OFF state resistance, it increases the resistance of VDD to ground path, controlling the flow of leakage currents, resulting in leakage power reduction in active mode. In standby mode of operation, 'sleep=1' and 'sleep bar=0' makes the transistors S1 and S2 to turn OFF forcing a high-impedance condition between PUN and PDN nodes. Thus, the introduction of sleep pass gate increases the resistance of the path from VDD to ground during standby mode of operation resulting in reduction of leakage current. Figure-9 shows the input-output curves of the NAND gate with proposed method simulated for 100-nm technology at 1-V supply voltage. It can be observed from the curves that the proposed NAND gate produces exact output logic levels. When this technique is applied to 8*8 Wallace tree multiplier with full adders the static power dissipation is reduced drastically

IV. RESULTS AND COMPARISONS

A. Results

The sleep pass gate technique was implemented and tested on 8*8Wallace tree multiplier with full adders and they were sized to fit in to 180-nm, 100-nm, 90-nm Berkeley Predictive Technology Models. Simulations were carried out using T-Spice of Tanner EDA tool in the standby mode of operation and the total leakage power was calculated. The proposed sleep pass gate technique provides exact logic levels and higher leakage savings as process technology shrinks in the 8*8 Wallace tree multiplier with full adders. The below Table-I shows the results of CMOS gates with sleep pass gate.

Table I: Experimental results for basic gates and full

Leakage power for 100nm Technology with VDD =		
CMOS Gate	Base case	Proposed
2 input AND	6.40E-08	4.85E-10
2 input OR	6.95E-08	5.26E-10
2 input NOR	5.4830 E-08	3.20E-10
2 input NAND	5.1700 E-08	2.87E-10
2 input XOR	1.24E-07	8.28E-10
1-bit Full Adder	8.90E-07	3.4900 E-09

From the above Table-I, it is shown that by using sleep pass gate the static leakage power of full adder is reduced. Hence the total leakage power of full adder is reduced. So it is shown that static leakage power of 8*8 Wallace tree multiplier with full adders is reduced upto half of its magnitude.

*B. Comparison with 8*8 Wallace multiplier with full adders*

In this section, sleep pass gate method is compared with the base case. First the simulation result of the 8*8 Wallace multiplier with full adder is shown in figure-10.From the simulation result, it is observed that the static leakage power of full adder for 100nm process technology with VDD=1 Volt is 8.9000E-07.So the static leakage power of 8*8 multiplier with full adder is 16.8000E-07.After using sleep pass gate in the 8*8 Wallace tree multiplier for same technology the obtained static leakage power for full adder is 3.49600 E-09 as shown in figure-11.And the static leakage power of 8*8 Wallace tree multiplier with full adders is 8.2000E-09.Hence half of the static power dissipation is reduced by this proposed method.

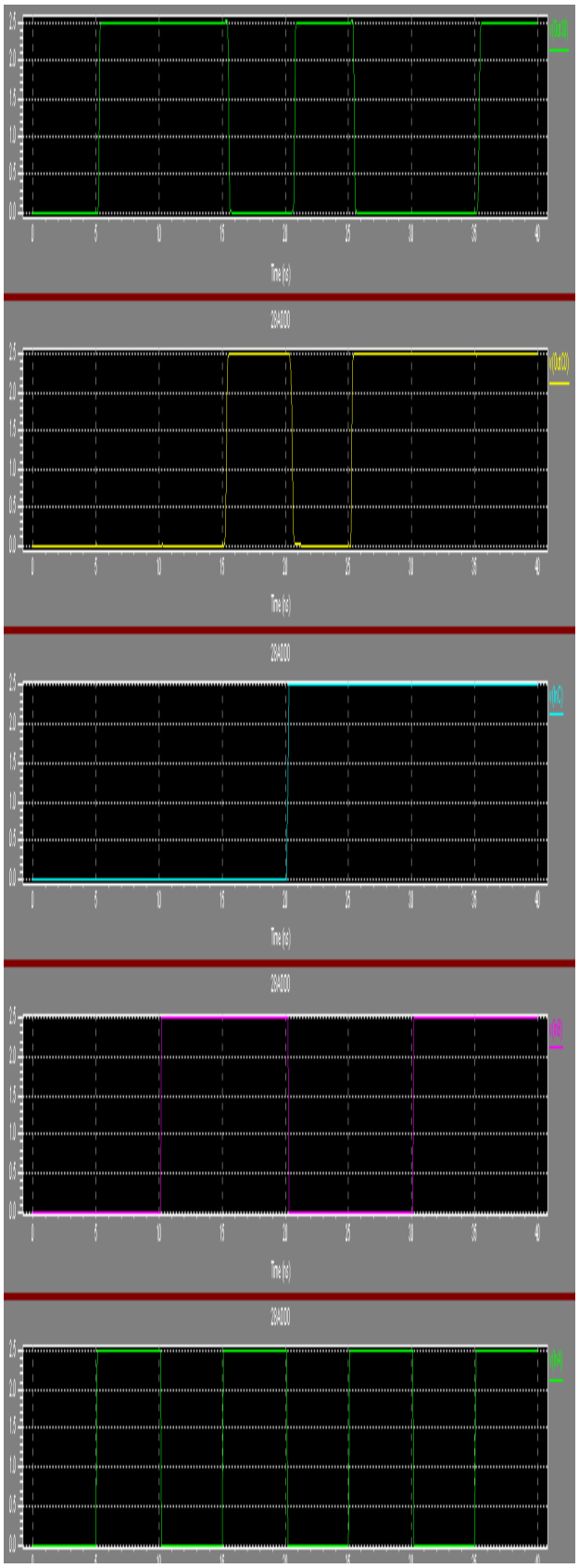

Figure 10: Simulation result of 8*8 Wallace tree multiplier with full adders

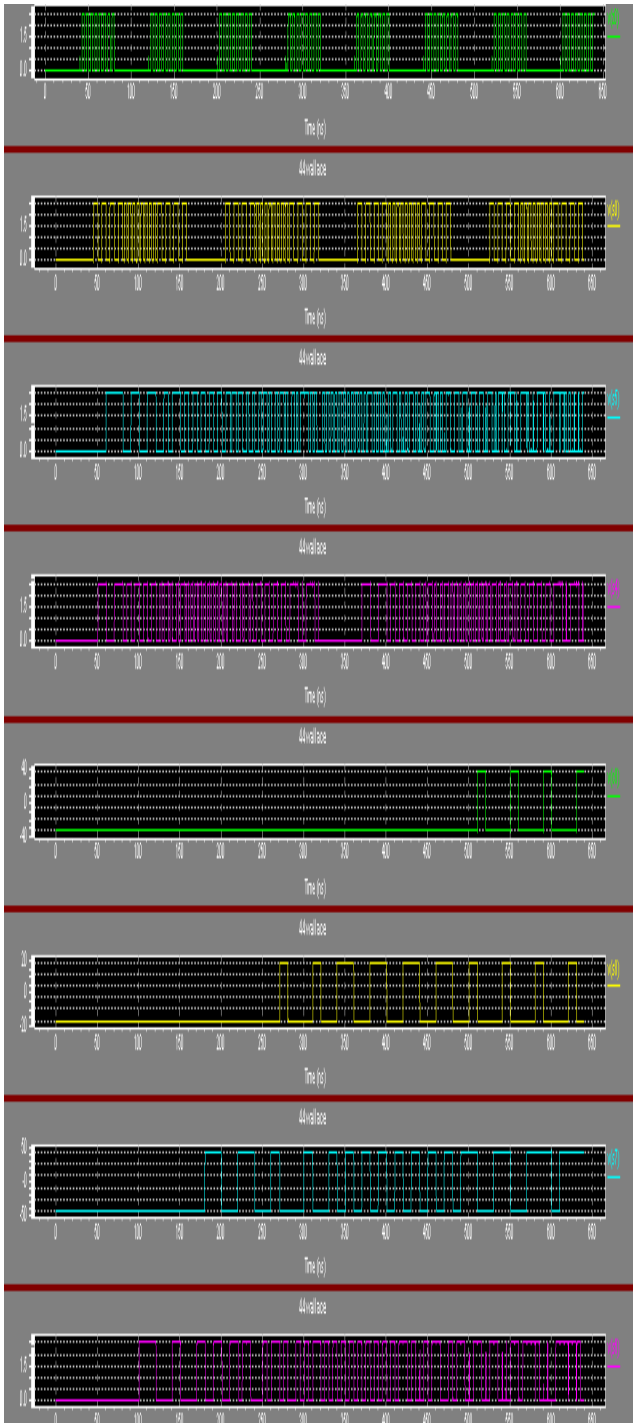

Figure 11: Simulation result of 8*8 Wallace tree multiplier with sleep pass gate

V.CONCLUSION AND FUTURE WORK

The leakage power of Wallace tree multiplier was reduced by replacing half adders by full adders. But the leakage power is comparatively high during the standby mode of operation. In order to reduce this leakage power, we present a sleep pass gate method which reduces leakage power during standby mode of operation upto half of its magnitude. And the designers can add the sleep pass gate cells in non-critical paths thereby not affecting the overall circuit delay, while significantly saving the leakage power.

In future the signal which is required to differentiate the Wallace multiplier in active or standby mode can be eliminated by observing the timing of inputs and outputs of the multiplier.

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