Abstract – NOC means network on chip is a new method for on chip communication to solve a problem that challenges system on chip. Arbiter is used in network on chip when number of input are requested for same output port, the arbiter has generate the grant signal on the basis of that number of input port getting a priority and the input port transmit a packet to output port. In this paper we have design round robin arbiter for NOC architecture. After design of round robin arbiter we analyze the area and power.

Keywords – Network on-Chip, Round Robin Arbiter.

I. INTRODUCTION

As the area and speed on a single chip now faces the big challenge on a single chip, more and more processing elements now are placed on System on chip. Network-on-chip (NoC) is a new method for on chip communication to solve the problem that challenges the system on chip. The physical interconnection on a chip becomes a primary factor which limits the performance and power consumption. As the switch speed of crossbar switch increases rapidly, a big problem we should resolve is to implement a fast and fairness arbiter to maximize the switch throughput and timing performance for Network-on-chips.

NoC has advantages on architecture, performance, reusability and scalability than traditional bus-based system-on-chip. Among these basic modules, the data flow control of virtual channel play an important role to alleviate the package congestion. The architecture and dataflow control will affect the design of arbiter of NOC significantly. The arbitration should guaranteed the fairness in scheduling, avoid starvation, and provide high throughput [1].

The NoC's switches should provide high speed and cost-effective contention resolution scheme when multiple packets from different input ports compete for the same output port. A fast arbiter is one of the most dominant factors for high performance NoC switches [4]. For the above reasons, the analysis of the performance of the arbiters are significantly meaningfulness in the design of Network-on-chips.

Fig 1: Block diagram of NOC Router

The heart of an on-chip network is the router, which undertakes crucial task of coordinating the data flow. The router operation revolves around two fundamental regimes: (a) the data path and (b) the associated control logic. The data path consist of number of input and output channels to facilitated packet switching and traversal. Generally 5 input X 5 output routers is used. Out of five ports four ports are in cardinal direction (North, South, East, West) and one port is attached to its local processing element.

Like in any other network, router is the most important component for the design of communication back-bone of a NoC system. In a packet switched network, the functionality of the router is to forward an incoming packet to the destination resource if it is directly connected to it, or to forward the packet to another router connected to it. It is very important that design of a NoC router should be as simple as possible because implementation cost increases with an increase in the design complexity of a router.

The design of router mainly consists of three parts:
1. FIFO
2. Arbiter
3. Crossbar

In this paper we have design arbiter block and used priority based Round robin arbitration techniques.
III. ARBITER

The arbiter trap the source and destination address from the output of buffer and generate the control signal so that input data from source side sending to the output port.

Fig: 2

Arbiter controls the arbitration of the ports and resolve contention problem. It keeps the updated status of all the ports and knows which ports are free and which ports are communicating with each other. Packets with the same priority and destined for the same output port are scheduled with a round-robin arbiter. The arbiter will release the output port which is connected to the crossbar once the last packet has finished transmission. So that other waiting packets could use the output by the arbitration of arbiter. In proposed work, round robin arbitration algorithm use to assign priorities when many input ports request the same output. Output signal generated by arbiter is read, external clock, three bit select lines for crossbar switch to select output channel. External clock signals which is indication for next connecting router that data is now available on output port of source router. When it is high, it means data is now available on output port of that router. Read signal generated by considering current status of signal of that port only. Read signal is high only when FiFo empty. Signal is low it means buffer is not empty, some data is store in Arbiter generates three bit select lines to select output channel for outputting data out of router. Steps follow to generate three bit select lines to properly route incoming packet out of router given as below. First compare three bit destination address to select output channel for dataflow out of router. Next three bit are source address indicate the input channel from where packet is transmitted.

IV. ROUND ROBIN ARBITERATION

Packets with the same priority and destined for the same output port are scheduled with a round-robin arbiter. Supposing in a given period of time, there was many input ports request the same output or resource, the arbiter is in charge of processing the priorities among many different request inputs. The arbiter will release the output port which is connected to the crossbar once the last packet has finished transmission. So that other waiting packets could use the output by the arbitration of arbiter. A round-robin arbiter operates on the principle that a request which was just served should have the lowest priority on the next round of arbitration. Depending upon the control logic arbiter generates select lines for multiplexer based crossbar and read or write signal for FIFO buffers.

V. SIMULATION RESULT

A) Without contention

<table>
<thead>
<tr>
<th>S.No</th>
<th>I/p Port</th>
<th>Source Address</th>
<th>DA</th>
<th>Select line</th>
<th>O/p port</th>
</tr>
</thead>
<tbody>
<tr>
<td>1)</td>
<td>Port a</td>
<td>000</td>
<td>001</td>
<td>Selb(000)</td>
<td>Port b</td>
</tr>
<tr>
<td>2)</td>
<td>Port b</td>
<td>001</td>
<td>010</td>
<td>Selc(001)</td>
<td>Port c</td>
</tr>
<tr>
<td>3)</td>
<td>Port c</td>
<td>010</td>
<td>011</td>
<td>Seld(010)</td>
<td>Port d</td>
</tr>
<tr>
<td>4)</td>
<td>Port d</td>
<td>011</td>
<td>100</td>
<td>Sele(011)</td>
<td>Port e</td>
</tr>
<tr>
<td>5)</td>
<td>Port e</td>
<td>100</td>
<td>000</td>
<td>Sela(100)</td>
<td>Port a</td>
</tr>
</tbody>
</table>

Fig No. 3 without contention Table

Here input port source addresses requested for different output port destination address so there is no contention in this case there is no role of arbiter the inputs are getting the control signal so that they transmit the packet to the destination.

B) With contention

<table>
<thead>
<tr>
<th>S.No</th>
<th>I/p Port</th>
<th>SA</th>
<th>DA</th>
<th>Select line</th>
<th>O/p port</th>
</tr>
</thead>
<tbody>
<tr>
<td>1)</td>
<td>Port a</td>
<td>000</td>
<td>001</td>
<td>Selb(000)</td>
<td>Port b</td>
</tr>
<tr>
<td>2)</td>
<td>Port b</td>
<td>001</td>
<td>001</td>
<td>Selb(001)</td>
<td>Port b</td>
</tr>
<tr>
<td>3)</td>
<td>Port c</td>
<td>010</td>
<td>001</td>
<td>Selb(010)</td>
<td>Port b</td>
</tr>
<tr>
<td>4)</td>
<td>Port d</td>
<td>011</td>
<td>001</td>
<td>Selb(011)</td>
<td>Port b</td>
</tr>
<tr>
<td>5)</td>
<td>Port e</td>
<td>100</td>
<td>001</td>
<td>Selb(100)</td>
<td>Port b</td>
</tr>
</tbody>
</table>

Fig.4. With contention Table
In above table all the input port are request for same output Port b. here Round Robin Arbiter Assign the Priority. On the basis of that port a has highest priority and port e has lowest priority. First port a transmit the data so arbiter generate the control signal & packet transmitted from source to destination. Same way for all port. Below waveform shows the simulation result of all input port request for same output port.

![Waveform Image]

**Fig: 4: Contention waveform**

In this paper after synthesize we found the area gate count is 33,489 and power consumption is 7mW.

**VI. CONCLUSION**

In this paper we propose that Round Robin Arbitration scheme, which grants that all input request are treated fairly. Hence our proposed arbiter is suitable for NoC design which needs high speed cross bar switches and router in them.

**REFERENCES**

2. Gao Xiaopeng, Zhang z.he, Long Xiang, Round Robin Arbiter for Virtual Channel Router, IMACS Multiconferences on “Computational” Engineering in System application”1610-1614
3. Li-shiuan Peh, William J.Dally ,A.Delay Modeland Speculative Architecture for Pipe line Router[J], the 7th International Symposium on High Performances Computer Architecture.255-266
4. Eung S.Shih, Vincent I.Mooney III and George f.Riley, Round Robin arbiter Arhiter Design And Generation, ISSS’02