Ring Oscillator Comparative Analysis at 22nm with bulk And High-K Metal Gate CMOS Technology and frequency impact

Shobha Sharma

Abstract—As we progress toward higher technology nodes there are improvement in density, frequency of operation and low power dissipation along with increase in leakage current and power. This paper examines a CMOS 11 stage ring oscillator implemented at 22nm node with bulk technology and High K metal Gate technology. Supply voltage increase results in increase in oscillation frequency in both the technology as expected. The simulation result shows the average power dissipated is more in High K Metal Gate technology compared to Bulk technology but the output frequency is more in High K metal gate technology. This results in lower energy/cycle in High K metal gate technology Ring Oscillator comparatively and hence shows that for advanced technology nodes this technology is a better option with reduced leakage due to High K material used. The experimental set up uses Predictive Technology models of Arizona State University at the two technology node and HSPICE simulator is used to carry out simulations

Index Terms— bulk CMOS,, high K, Ring Oscillator, PTM.

I. INTRODUCTION

Ring oscillator is a very common element of Voltage controlled oscillator. It is widely used but still has difficulties and is evident from the design, analysis and modeling. The design of ring oscillator includes many dimensions such as power, area, speed and the application it is designed for.

Semiconductor industry is actively researching into high K dielectrics to reduce the leakages and so as to replace the present SiO_2. .

The International Technology Roadmap Semiconductor [1] predicts that with scaling gate dielectric should be less than 1nm with low leakage current. And for this requirement to be fulfilled, high K dielectrics need to be searched.

Initially Silicon Nitride and Silicon oxynitride [2, 3] were proposed. And this research continues till date. The reports with high K dielectric talks of low gate leakage current but there are several other researchable area such as thermal instability, control of EOT, reactions with metal gate and reactions with poly Si gate etc.

Initially it was suggested that HfO_2 and ZrO_2 dielectrics are thermally stable [4] on silicon. But they are also replaced by TiO_2 and TaO_3 as the better option. The gate dielectric and High K interface capabilities are also researchable areas that are pursued.

The bulk of High K material should also be stable. And whether high K dielectric material be amorphous or single crystalline, is a researchable area.

Scaling down to advanced technology nodes results in low power, high performance and dense system but with leakages and process variation effect in sub nanometer range. So it is necessary to examine the high K metal gate and Bulk CMOS technology both.

This paper does this by observing ring oscillator circuit at the two technologies. The models are taken from Arizona State University (USA)'s Predictive Technology Model of 22 nano meter cmos technology for BULK (Beta version) and High K Metal gate.

II. EXPERIMENTAL SETUP AND RESULTS

A. The following circuit is implemented at 22nm node

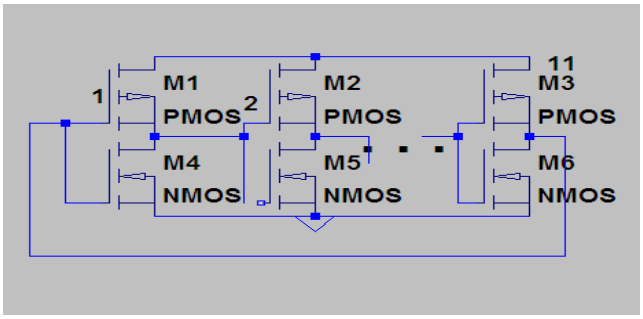

Fig 1. 11 Stage cmos ring oscillator at 1v supply voltage

B. Simulation Result

The two circuits at the different technology are identical in every aspect viz- transistor sizes, supply voltage etc except the obvious difference in the models. Below are the frequency output diagram of the Hspice [5] simulator showing the higher frequency of High K metal Gate technology.

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Shobha Sharma, ECE, Indira Gandhi Institute of Technology, GGSIP university, Delhi, India.

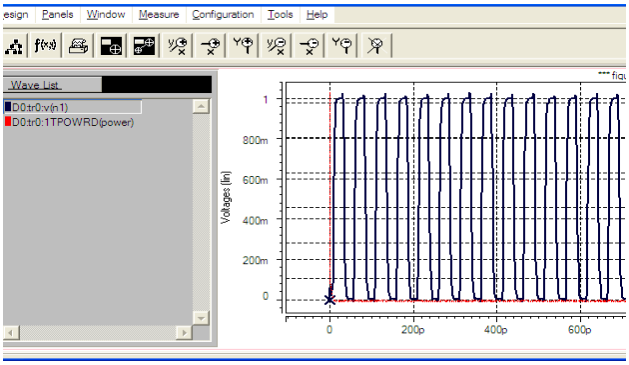

Fig 2 Frequency output of High K metal Gate Ring Oscillator

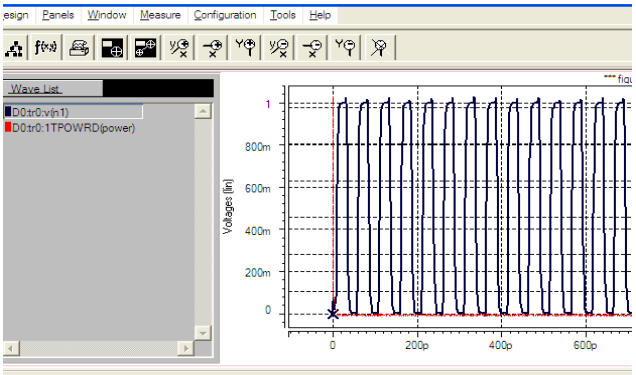

Fig 3 Frequency output of High K metal Gate Ring Oscillator

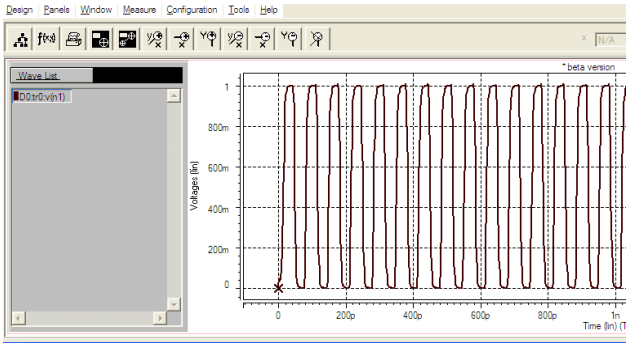

Fig 4 Frequency output of BULK cmos Ring Oscillator

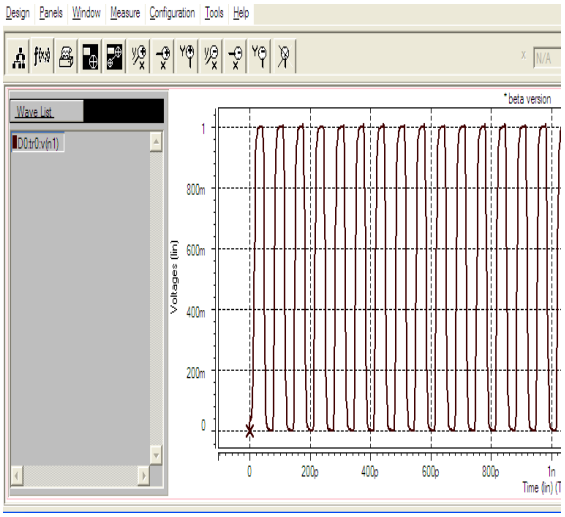

Fig5. Power wave form of High K metal Gate Ring Oscillator

C. Below is the comparison table of two technology 11 stage ring oscillator

Table I. Comparison table of Ring oscillator at High K Metal Gate and Bulk Technology

parameter	Hik Mg CMOS	Bulk CMOS
Avg power micro watt	346	287
Freq peta hertz	16.45	15
Vdd volt	1	1
toxe meter	1.05e-009	1.2e-9
toxp meter	8e-010	0.9e-9
toxm meter	1.05e-009	1.2e-9
Temp o C	25 C	25 C
Vth Nmos V	0.50308	0.5118
Vth pmos V	-0.4606	-0.372
vsat pmos m/sec**2	210000	78000
Vsat nmos m/sec**2	250000	200000
Rdsw nmos ohm	145	130
Rdsw pmos ohm	145	130
Rsw ohm	75	75
Rsw ohm	72.5	65
Rdw nmos ohm	75	75
Rdw pmos ohm	72.5	65

The table shows the higher average power of High K metal gate technology along with higher frequency as well. This results in lower energy per cycle and is a better option in sub nanometer range compared to BULK cmos technology.

III. CONCLUSION

Comparison is made of 11stage cmos ring oscillator at two different technologies. The two technology models of Arizona state University USA, demonstrate that High K metal gate technology has higher frequency which ultimately would lead to lower energy per cycle\. It is inspite of the fact that average power consumed is more in High K metal gate technology. Greater Clock rate leads to reduced energy per cycle, making it more energy efficient.

IV. FUTURE SCOPE

The circuit can be further studied for process variation effect to know the better technology in nano meter range.

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AUTHORS PROFILE

Shobha Sharma She has done M.E from Bits pilani and is IEEE member. Her research interest are nano cmos low voltage and high performance design. She hHas several research publications in international Journals and conferences