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A Survey - Power Management in Multicore System On-a-Chip (SOC)

V.Radhika, K.Baskaran, N.Krithika

Abstract—Multi core systems running multiple process, needs a power management technique which is able to provide tradeoff between power and performance. Power management refers to the generation and control of regulated voltages required to operate an electronic system. With growing power management concern there is necessity to develop an efficient voltage regulation technique to improve the performance of any system. In the present scenario power supply design must be integrated within the system to improve the efficiency. Integrated components like switching regulator, linear regulators, and voltage reference are typical elements of power management.

Index Terms— Linear regulator, power management, power converters, switching regulator.

I. INTRODUCTION

As the size of transistors scales from one generation to the next billions of transistors can be integrated on a single SOC. The future multi core SOC's utilizing the high computing power of billions of transistor is expected to integrate heterogeneous components on a single semiconductor chip. Integrating billions of transistors in a single IC results in larger power dissipation and also frequency of operation of system get increased due to device scaling [5]. An important factor with increase in frequency, is that the chip operating at higher frequency perform faster computations. But, consumes more power and the load transitions also have been increased due to high frequency. So a voltage regulator with higher efficiency and faster transient response with minimum power dissipation is needed to be used in multi-core SOC'S.

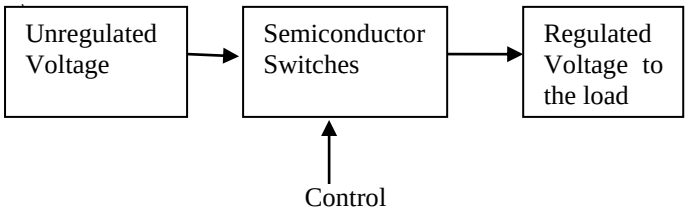

Fig.1 Voltage regulator operation

This paper is to investigate the different techniques available for voltage regulation in SOC design and to synthesize a suitable technique which can be utilized in a future multi core SOC's.

II. OFF-CHIP VOLTAGE REGULATION

A. Synchronous Buck Converter

There are several off chip voltage regulators available in market out of which the buck converter is the crucial one in delivering power to any processor. Low voltage power Supplies require a synchronous buck converter where diode in the conventional converter is replaced with MOSFET to improve the efficiency fig [2]. In the synchronous buck converter conduction losses and switching losses get increased with increase in frequency which limits its application to high frequency application [42].

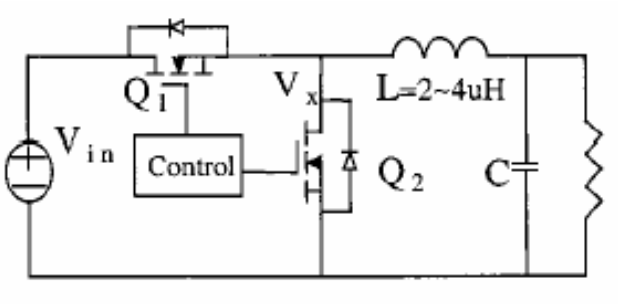

Fig.2 Synchronous buck converter [1]

B. Multiphase Buck Converter

Multi phase converter [8] as shown in fig[3] is another form of buck converter consisting of several phases in order to minimize the ripple of the output current caused by the large inductor. It uses small inductors that minimizes the output ripple and improves the transient response but the efficiency gets reduced due to small size inductors.

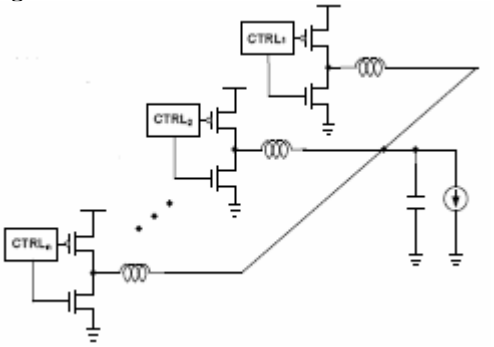

Fig.3 Multi phase buck converter [2]

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***** Correspondence Author (s)
V.Radhika, Department of Electronics & Instrumetation Engineering,Sri Ramakrishna Engineering College, Coimbatore, India,
Dr.K.Baskaran, Department of Computer science &Engineering, Government College of Technology,Coimbatore, India.
N.Krithika, Department of VLSI Design Sri Ramakrishna Engineering College,Coimbatore, India,.

C. *Voltage Regulation with Swap Controller*

A controller is placed off chip between load and power supply to limit the inrush current by decreasing the on-resistance of N-channel MOSFET [10]. It also provides protection against high voltage transients, over and under voltage defects.

The off chip voltage regulators generally operates at low frequency which make them difficult to respond to sudden voltage change. Also there are parasitic elements (inductance and capacitance) in the power delivery network between the voltage regulator module and the load, which affect the voltage variation problem [3].

III. SINGLE STAGE ON-CHIP VOLTAGE REGULATION

Regulators that are integrated on the chip provide the benefit of per-core voltage control and also faster voltage switching as the voltage regulator is placed close to the load and reduces the effect of parasitic inductive and capacitive elements (that lie between regulator and load) on the transient response .

Even though there are variety of topologies available for on chip voltage regulation the linear regulators and switching regulators are commonly used.

A. *Linear Regulator*

Linear regulator shown in fig[4] is the fundamental building block of every power supply unit. The linear regulator uses the MOSFET to sense the change in output voltage [27]. The most efficient linear regulator is low drop out linear voltage regulator and the dropout refers the amount of voltage drop out to maintain a stable output voltage. Due to their small size they can be used to create multiple supply voltages, it has higher conversion efficiency if difference between input and output voltage is small. It also has high quiescent current value at no load conditions.

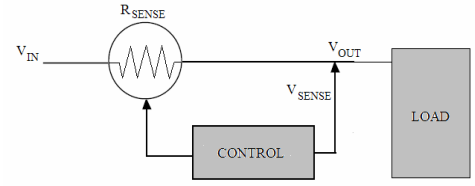

Fig.4 Linear voltage regulator[16]

Low dropout voltage regulators which can be used for portable electronic products are explained in low dropout voltage regulators for wireless application [16] [20]. In this low dropout voltage regulators Pmos pass transistor is used to reduce quiescent current under no load conditions [31]. Two stage error amplifier is used to sense the change in output voltage relative to the voltage reference (Vref). Frequency compensation circuit is imparted to maintain the stability and the value of capacitor also decreased to pico farad due to frequency compensation circuit so that load capacitance can be imparted in the on-chip. The important characteristic of this type of LDO is that it has a faster transient response so that when there is a step change in load current, the output voltage reaches a stable value in a short duration of time. The response time depends on closed loop band width of LDO regulator.

B. *External capacitor less LDO*

Conventional LDO regulator for stability requirement uses a large external capacitor (microfarad range). Large microfarad capacitor cannot be realized on-chip so the capacitor has to be connected externally. A capacitorless LDO is proposed (32) to remove large external capacitor which reduces board real estate and overall cost. In the design of large external capacitor less LDO a differentiator is used which provides fast transient response as well as internal ac compensation.. The trade off that exists between stability and transient response is the most difficult design problem and several iterations of design procedure is needed further the size of the capacitor C_f increases the area.

C. *Switching Regulators*

Switching regulators can be used on-chip and it needs an oscillator, pass elements, inductors, capacitors and diodes [28]. The response time of switching converters depends on frequency of oscillators and it is much smaller than linear regulators.

Switched capacitors regulators [17][25][26] shown in fig[5]are easier to implement but the capacitors are periodically charged and discharged through the resistive switches so that converter cycles through number of switched networks which leads to losses. Two oppositely phased switches are used in one clock phase capacitors are charged with a constant current and in other phase all the capacitors are connected in series with input source and connected to the output load. The output voltage is sensed through a feedback network and it controls the amount of charging current and the output much depends on the input. Switched capacitor regulators suffers from several drawbacks i) efficiency depends on Vout to Vin ratio ii) conversion ratio is predetermined by circuit topology iii) switched capacitor provide a solution for eliminating the inductor in power converters but it needs a large capacitor to deliver large currents. The efficiency of switched capacitor converter can be improved by selecting the conversion ratio based on loading conditions and input voltage [25].

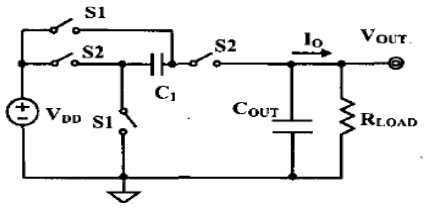

Fig.5 Switched capacitor voltage regulator [17]

D. *Integrated Inductor MEMS Approach*

MEMS approach [29][30] can be used to realize the inductors and the main drawback of this approach is the process incompatibility with fabrication process. It is difficult to interface this type of dc/dc converters on- chip in CMOS process. The MEMS inductors has low Q value at high inductance values, product cost is also high. Further research can be done on these MEMS inductors so that it can be used in power supply circuit

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E. Virtual Inductor Op-amp Realization

Integrated inductor can be realized through gyrator given in Fig [6]. An inductor can be replaced with assembly containing resistors, capacitor, transistor or Op-Amp[24]. The circuit works by inverting and multiplying the effect of the capacitor in an RC differentiating circuit, where the voltage across the resistor behaves through time in the same manner as the voltage across an inductor. The op-amp follower buffers this voltage and applies it back to the input through the resistor R_L. The desired effect is an impedance of the form of an ideal inductor L wit'h a series resistance R_L. Gyrators can be used to realize inductors from the range of micro Henry to mega Henry but the simulated inductors do not have inherent storage capacity as real inductors and does not respond to sudden input change as real inductor do. Since, gyrator uses active elements it can function as gyrator up to the power supply range of active circuits and furthermore transient response depends on the bandwidth of the active element.

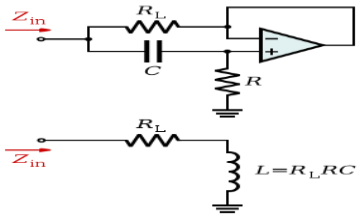

Fig.6 Gyrator [24]

F. Inductor multiplier Technique

Inductor multiplier technique developed uses a small inductor [6], fig [6] its value is multiplied several times as required by on chip clusters. In this realization effective inductance between two points is increased by allowing the current ripple in the inductor to increase with voltage across the inductor constant.

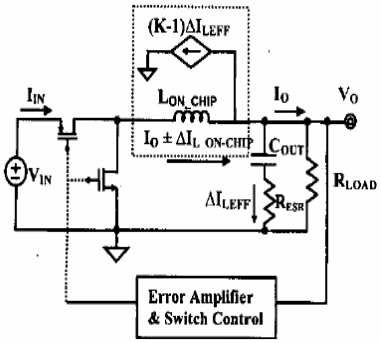

Fig.7 Switching regulator with inductor multiplier [6]

This novel concept maximizes the use of integrated inductors for SOC implementation of voltage regulators .The drawback of this technique is that it has higher power dissipation which reduces the efficiency of the converter.

G. Hysteric control Buck Converter

In hysteric control buck converter [8] given in fig[7], PMOS and NMOS transistors are used to form an inverter that Switches on–off.

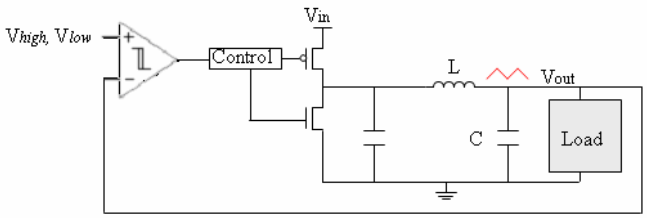

Fig.8 Hysteric control buck converter [8]

When switch is in on position the input voltage is applied to inductor is removed when switch is in off position input voltage applied to inductor is removed. The output voltage Vout to the load is given back as input to the hysteric comparator, compares the regulated output voltage with threshold voltage .If the regulated output voltage is smaller than lower threshold value then PMOS transistor is turned on, if it is greater than higher threshold value then NMOS transistor is turned on. Since Vout is sensed directly by the comparator hysteric control can react quickly to sudden load transients.

H. Adaptive Supply Regulator

Power dissipation in digital circuit is dominant by dynamic power. To reduce the dynamic power dissipation in digital circuit energy efficient adaptive power supply regulator is proposed (22). A digital controller for adaptive supply regulator has been described which utilizes feedback loop to minimize output transients (23). Integral component in this design is a buck converter and the regulated output of this converter is average voltage of a PWM. In the feedback loop a voltage controlled oscillator is used which monitors the variation in circuit performance and scales the regulated voltage of a buck converter via loop controller (PID controller). This loop compensates for any variations and provides a stable constant output voltage to the load. Both the fixed frequency and variable frequency loop controller has been designed. In the fixed frequency controller the conversion efficiency decreases as regulated output voltage decreases, the efficiency is also limited by fixed overhead power consumption. These difficulties can be overcome with a variable frequency controller were a high conversion efficiency can be obtained over a dynamic voltage level but the efficiency will be degraded for the low load conditions. In low load conditions loop enters a non linear mode and buck converter operates discontinuously.

I. On-chip Switching Regulator using Current Staggering

Current staggering technique is used in an on chip voltage regulator for multi-core processors [4].The current staggering is a architectural technique applied to a multiphase buck converter which minimizes the voltage variations during current transients. In conventional techniques voltage variations can be reduced by increasing switching frequency, but increasing the switching frequency leads to conduction losses and switching losses. Increasing the number of phases will reduce the conduction losses but increases switching losses.

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This current staggering will be an efficient technique in reducing the voltage variation problems due to current transients. The change in voltage dv can be minimized by reducing the ratio di/dt .The dt value can be increased to reduce the value of di/dt so that the inductance value can be reduced. But reducing the inductance value results in larger voltage variations problems when current consumption increases during short time intervals. The current staggering technique will be effective only when sudden variations of current occur in small value, also the staggering requires the processor to turn on and off circuits gradually. There is significant power leads to performance loss.

Both linear and switching regulators are analyzed were the linear regulators has faster transient response and provide clean output but the main drawback is that output depends on input which reduces the efficiency. The power dissipation is also very high when the output voltage is much lower than the input voltage. Switching regulators has higher conversion efficiency but duty cycle determines the amount of charge delivered to the load .Further the size of capacitor and inductor is large .If the value capacitor and inductor is reduced then it reduces the response time. The other major difficulty is the fabrication of inductor on chip and output voltage is also noisy.

The above discussed single stage regulators faces challenges from both input and output side .The regulator suffers from input voltage variations and severe load transients from output side. Since it is difficult for the single stage regulator to face the challenges from both input and output side a two stage regulator is designed were the first stage consists of a switching regulator and second stage consists of linear regulator .

TABLE I
Comparative Evaluation [6]

	SOC Feasibility	Output Power	Area	Efficiency
Switched Capacitor	Worst	Low	High	Good
External Inductor	Worst	Highest	Highest	Best
Linear Regulator	Better	Low	Lowest	Worst
MEMS	Good	Medium	High	Poor
Virtual Inductor	Best	Medium	Low	Moderate
Inductor Multiplier	Best	Medium	Low	Moderate

IV. TWO STAGE ON-CHIP VOLTAGE REGULATION

A . Hybrid Switching Regulator

On-chip two stage approach consisting of switched capacitor regulator as first stage for high voltage conversion and second stage consists of linear regulator for low voltage conversion however this approach has low efficiency [11].An alternative method of two stage voltage regulation technique shown in fig[9] is the use of buck type switching regulator placed off-chip [3] as a first stage to step down the input voltage and the duty cycle of switching regulator is modulated by pulse width modulation to control the amount of power delivered to the load. Switching regulators are placed off chip due to the presence of large size inductors to ensure clean output voltage.

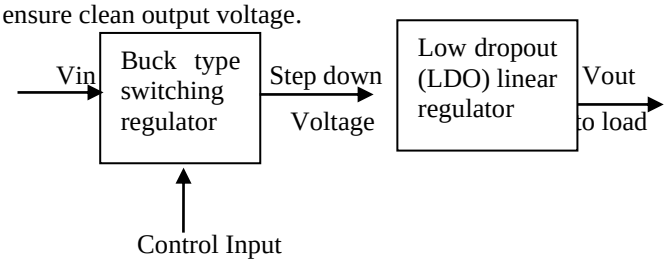

Fig.9 Two stage voltage regulator [3]

Before going to the load the supply will go undergo the second level of regulation by the linear regulator placed on chip to the bring the voltage level close to different load requirements which minimizes the package level fluctuations The main drawback with this technique is the presence of low pass filter in switching regulator stage attenuates the high frequency square wave and furthermore the efficiency of regulator depends on duty cycle and there is high quiescent current at no load conditions. The transient response will also be reduced when there is a larger change in load conditions and further the output of switching regulator exhibits ripple due to filter inductor and inherited by linear regulator placed on-chip. An alternative filter design can be used in this technique to improve the efficiency and isolation scheme can be used between the two stages to prevent the irregularities inheriting one another.

B.3D Switching & Linear Regulator

Linear and switch mode conversion technique for 3D circuits is proposed [1]. In 3D linear converter the current is distributed within the interconnect network. The RLC transmission lines are connected by 3D vias. Different switching events occur at different time for relative long periods of times, producing DC current load fluctuations. A distributed filter[2] is used instead of conventional LC filter in 3D switching regulator. This type of filter can be utilized as low pass filter in buck converter. The filter is composed of transmission lines terminated by lumped capacitance. The inter plane structure is connected by 3D vias. At the n plane load is represented as periodic current load and a reference clock signal. Switching 3D circuits exhibits a higher efficiency as compared to other on chip switching regulator due to the low resistance of distributed filter .The primary advantage of this technique is that it is able to provide large amount of current to the load and further the large size inductor is removed. The average power consumed by power MOSFETs and driving buffers is composed of resistive and dynamic power losses. Increasing the width of power MOSFET reduces the resistive losses and increases the dynamic losses .To Minimize the power dissipation of the entire network differently sized power MOSFETs are needed. The switching converter with a distributed filter is an iterative approach since effective output resistance of power MOSFETS affects the magnitude of duty cycle which determines the output voltage. Due to heavy losses at higher switching range switching converter with a distributed filter can be used up to a critical conversion ratio above that value linear filter has to be used.

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TABLE II
Comparative Evaluation

	Hybrid Regulator	3D Switching & Linear Regulator
SOC Feasibility	Medium	Better
Output Power	Good	Medium
Area	High	Low
Efficiency	Good	Medium

V.CONCLUSION

In this paper survey on the regulator topologies that have been used for system on a chip as well as their benefits and drawbacks were discussed. Off-chip regulators occupy a significant portion of the PCB area and make it costly. Furthermore off-chip voltage regulators operate at low frequencies, which prevent them from adjusting to new voltages rapidly. Also there are parasitic elements (inductance and capacitance) in the power delivery network between the voltage regulator module and the load which affect the voltage variation problem. Single stage on-chip voltage regulators operating at high switching frequencies avoids bulky filter components such as inductors and capacitors and allows filter capacitor to be integrated entirely on-chip and enable fast voltage transients. But the single stage voltage regulator suffers from severe input voltage variations and load transients so it is difficult for a single stage voltage regulator to face challenges from both input side and output side. Hybrid two stage voltage regulation techniques has proposed with buck type switching regulator as first stage to step down voltage serves as the input for the linear regulator connected as second stage to deliver the different voltage levels according load requirements.

In linear and switching regulators proposed for 3D integrated circuit uses distributed filters instead of conventional LC filter which makes the filter to be placed in the chip which improves the transient response but to reduce the power dissipation the size of the MOSFET should be varied according to different load requirements and further more the size of output capacitor is large enough which increases the area of the chip.

In multi core systems dynamic power management techniques [5] [11] [20] [21] such as clock gating, power gating, variable frequency, variable voltage supply, variable device threshold can be implemented to a chip as a whole or it can be implemented individually to each core and advanced pulse width modulation techniques [41] can be used to improve the performance .These techniques can improve the efficiency, minimize the power dissipation and provide a better voltage control. Optimization techniques and isolation techniques or alternative filter design [37] can also be added to the above mentioned power management schemes to improve the efficiency.

TABLE III Comparative Evaluation

	SOC Feasibility	Output Power	Area	Efficiency
Off-Chip	Worst	Low	High	Poor
Single stage	Medium	Better	High	Better
Two Stage	Better	High	Medium	Best

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V.Radhika received her B.E degree from R.V.S College of Engineering &Technology, Dindigul and M.E degree from Kumaraguru College of Technolgy,Coimbatore.She is currently working as Assistant Professor in Sri Ramakrishna Engineering College, Coimbatore. Her area of interest includes low power VLSI,ASIC.She is a member of ISTE & IEEE.

Dr.K.Baskaran is with the Department of Computer Science Engineering in Government College of Technology,Coimbatore. He is a member of IEEE, ISTE and his research areas include mobile computing and wireless communication and VLSI.

N.Kirthika received the Bachelor of Engineering degree in Electronics and Communication Engineering from Avina shalingam University, coimbatore,India, in 2009 and received Master of Engineering degree from the Department of VLSI Design, Anna University of Technology,Coimbatore, India. She is currently working as Assistant Professor at Sri Ramakrishna Engineering College,Coimbatore. Her area of interest includes solid statedevices, VLSI fabrication & VLSI architecture.Her area of interest includes solid state devices, VLSI fabrication & VLSI architecture.

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