# Design of Low Power Double Data Rate 3 Memory Controller with AXI compliant.

**Vijaykumar, R K Karunavathi, Vijay Prakash**

***Abstract — As system bandwidths continue to increase, memory technologies have been optimized for higher speeds and performance. The next generation family of Double Data Rate (DDR)RAMs are DDR3 RAM. DDR3 RAMs offer numerous advantages compared to DDR2. These devices are lower power, they operate at higher speeds, offer higher performance (2x the bandwidth), and come in larger densities. DDR3 memory devices provide a 30% reduction in power consumption compared to DDR2, primarily due to smaller die sizes and the lower supply voltage (1.5V for DDR3 vs. 1.8V for DDR2). This paper represents the overall design and architecture of Low power Double Data rate 3(DDR3) memory controller. In this paper clock gating is used as a low power technique .***

## I. INTRODUCTION

This low power DDR3 controller is the AXI compliant which permits access of DDR3 memory content through AXI Bus interface. The handshaking mechanism is mainly used to meet the requirement of AXI bus protocol. DDR3 RAM is a modern kind of dynamic random access memory (DRAM) with a high bandwidth interface. It is one of several variants of DRAM and associated interface techniques used for DDR3 RAM and is not directly compatible with any earlier type of random access memory (RAM) due to different signaling voltages, timings, and other factors. The DDR3 controller works as an important bridge between the AXI host and DDR3 memory. It takes care of the DDR3 initialization and various timing requirements of the DDR3 memory. It is the 3rd generation of DDR memories, featuring higher performance and lower power consumption with earlier generations. The actual DRAM arrays that store the data are similar to earlier types, with similar performance. The primary benefit of DDR3 RAM over its immediate predecessor, DDR2 RAM, is its ability to transfer data at twice the rate (eight times the speed of its internal memory arrays), enabling higher bandwidth or peak data rates. The DDR3 controller performs multiple schemes to increase the effective memory throughput. These schemes include combining and reordering the Read/Write commands.

**Manuscript Received June 25, 2012.**

**Vijaykumar,** M.Tech, VLSI DESIGN & ESD, Dept. of E & C, BIT, Bangalore.
**R K Karunavathi,** Asstociate Professor, Dept. of E & C, BIT, Bangalore.
**Vijay Prakash,** Asstociate Professor, Dept. of E & C, BIT, Bangalore.

For attaining the maximum throughput from the memory, It perates all the memory banks in parallel and minimizes the effect of precharge/refresh and other DDR3 internal operations.

## II. BLOCK DIAGRAM OF LOW POWER DDR3 MEMORY CONTROLLER

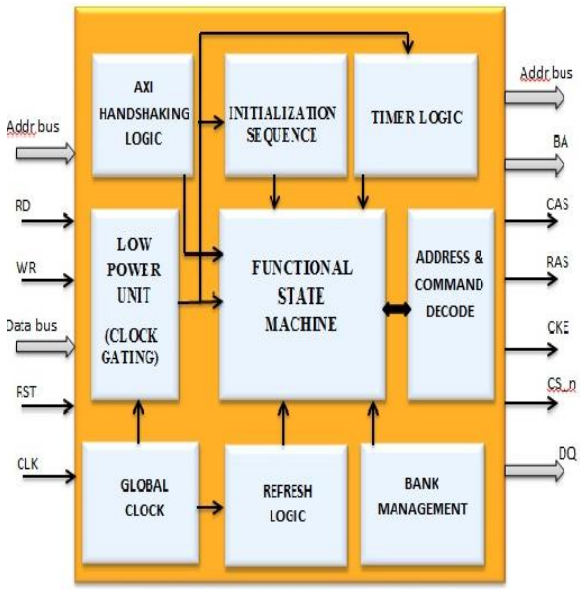



**Fig .1: Block diagram of low power DDR3 controller.**

The Low power DDR3 memory controller has following blocks.

- AXI Handshaking Logic.
- Initialization sequence state machine.
- Functional state machine.
- Address & Command decode .
- Bank management.
- Refresh Logic & timers.
- Low power unit.

Handshaking mechanism The handshaking logic has two main sub blocks , one is Device Ready and other one is Command acknowledgement signal generation block.

Device Ready signal is high when the device is ready to accept any command. The device is will generate a low signal under following conditions.

-Initialization is not done.
-Write process is in progress.
-Read process is in progress.
-Refresh process is in progress.

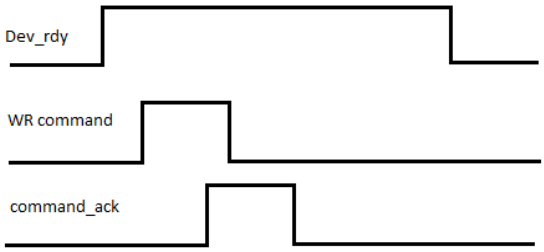



**Fig.2: Command acknowledgment signal**

- Command should be sent only when device is ready.
- When device accepts command it issues command acknowledgement signal.

### A. Functional state machine

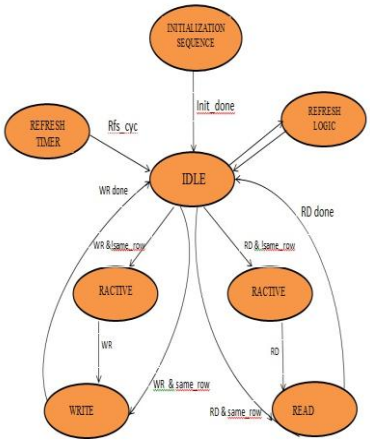



**Fig.3: Functional state machine**

- The DDR3 memory must be initialized before proceeding to read or write process.
- After initialization it memory must be in IDLE state .
- Refresh is done continuously by refresh logic.
- Then pre-charge is done, to open and closing the rows.
- Then commands are performed according to the priorities.
- Once the commands are served the memory must brought into IDLE state.

### B. Address and command decode logic

- The input address comes along with the AXI command.
- Then the address is stored into the lat_addr when the command is received.
- The row address is derived at the time of row active (RACTIVE) command is issued.
- The column address is derived at the time of write command is issued.
- This address mapping is defined by the memory vendors, here we designed according to the specification of micron DDR3 memory.

*Address mapping* - Address line is of 28 bit.
[27:25] – Bank address.
[24:11] – Row address.
[10:0] - Column address.

### C. Bank management.

The DDR3 memory supports up to eight memory banks. The bank selection is done by using BA[0:2] signal. The selection of bank is as shown in table 1.

**Table 1. Bank selection**

| BA[0:2] | BANK |
|---|---|
| 000 | BANK 0 |
| 001 | BANK 1 |
| 010 | BANK 2 |
| 011 | BANK 3 |
| 100 | BANK 4 |
| 101 | BANK 5 |
| 110 | BANK 6 |
| 111 | BANK 7 |

### D. Refresh logic and timer.

The DDR3 memory controller is designed in such a way that it will send the refresh signal to the DDR3 memory after every 7.8usec. Refreshing is required to keep the data alive in DDR3 memory.

### E. Low power unit.

In VLSI design there are two power dissipations. One is static power dissipation and other is dynamic power dissipation. Static power dissipation is due to leakage current and tunneling current through the gate oxide. Dynamic power dissipation is due to charging and discharging of load capacitances( i,e switching activities). In RTL coding we can reduce the dynamic power using some low power technique schemes . One of the popular technique is the clock gating. The clock gating scheme is shown below.

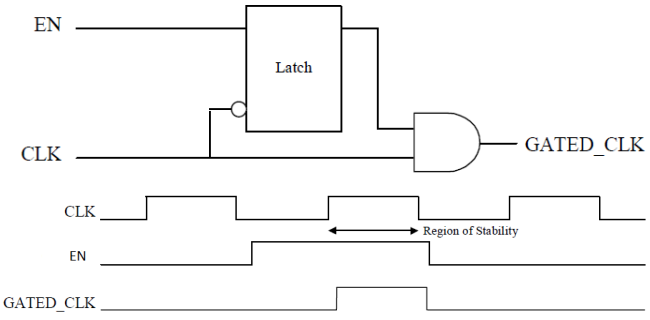



**Fig. 4: Clock gating**

Whenever the clock enable signal is low then it blocks the Clock signal and if the enable signal is high then it allow clock signal .Whenever the system enters in sleep mode , then it disable the clock enable signal so this saves some power .

## III. AXI COMPLIANT DDR3 MEMORY CONTROLLER

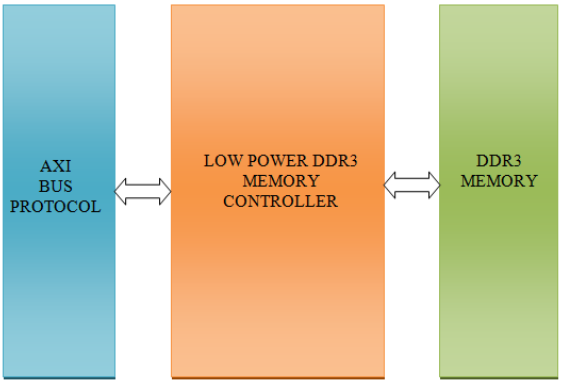



**Fig.5:AXI compliant ddr3 controller interface.**

The AMBA AXI protocol is targeted at high-performance, high-frequency system design and includes a number of features that make it suitable for a high-speed submicron interconnect.

The key features of the AXI protocol are:

- Separate address/control and data phase
- Support for unaligned data transfers using byte strobes
- Burst-based transactions with only start address issue
- Separate read and write data channels to enable low-cost *Direct Memory Access* (DMA)
- Ability to issue multiple outstanding addresses
- Out-of-order transaction completion
- Easy addition of register stages to provide timing closure.

## IV. IMPLEMENTATION

This DDR3 memory controller is mapped to the XC3S400 Field Programmable Gate Array(FPGA). The synthesized details of the design is as shown in Table 2 &3.

**Table 2: Target device(XC3S400)**

| Device Utilization Summary | | | |
|---|---|---|---|
| **Logic Utilization** | **Used** | **Available** | **Utilization** |
| Number of Slice Flip Flops | 111 | 7,168 | 1% |
| Number of 4 input LUTs | 242 | 7,168 | 3% |
| Number of occupied Slices | 177 | 3,584 | 4% |
| Number of Slices containing only related logic | 177 | 177 | 100% |
| Number of Slices containing unrelated logic | 0 | 177 | 0% |
| Total Number of 4 input LUTs | 286 | 7,168 | 3% |
| Number used as logic | 242 | | |
| Number used as a route-thru | 44 | | |
| Number of bonded IOBs | 83 | 141 | 58% |
| Number of BUFGMUXs | 3 | 8 | 37% |

**Table 3: Device utilization summary.**

| ddr3_controller Project Status (06/19/2012 - 23:13:57) | | | |
|---|---|---|---|
| **Project File:** | ddr3.xise | **Parser Errors:** | No Errors |
| **Module Name:** | ddr3_controller | **Implementation State:** | Placed and Routed |
| **Target Device:** | xc3s400-5pq208 | **•Errors:** | No Errors |
| **Product Version:** | ISE 12.1 | **•Warnings:** | 5 Warnings (0 new) |
| **Design Goal:** | Balanced | **•Routing Results:** | All Signals Completely Routed |
| **Design Strategy:** | Xilinx Default (unlocked) | **•Timing Constraints:** | All Constraints Met |
| **Environment:** | System Settings | **•Final Timing Score:** | 0 (Timing Report) |

The Table 2 shows the Module name and target device used ( i,e XC3S400) . It also shows the place and route status and number of errors & warnings.

Table 3 shows the device utilization . i,e how many flip flops , LookUpTables , Input ouputs(IOBs) and number of slices used.

## V. RESULTS

The below figures are showing snapshot of the DDR3 Controller operation in various modes. The design has been coded in "Verilog HDL" language simulation is done using Modelsim by Mentor graphics tool.

### A. Initialization

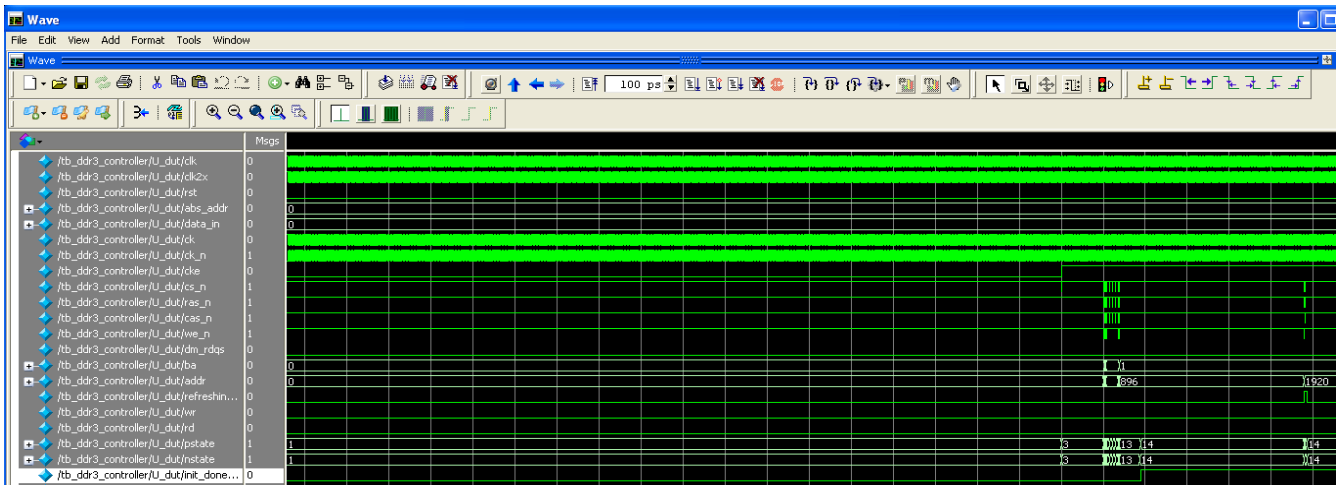



**Fig.6: simulation waveform of initialization sequence.**

## B. Refresh

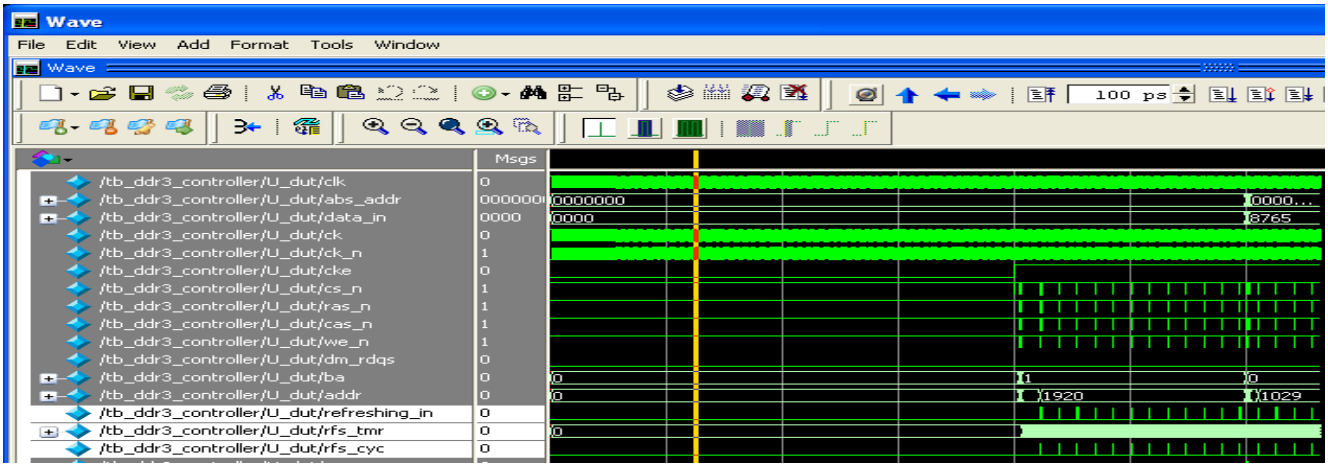
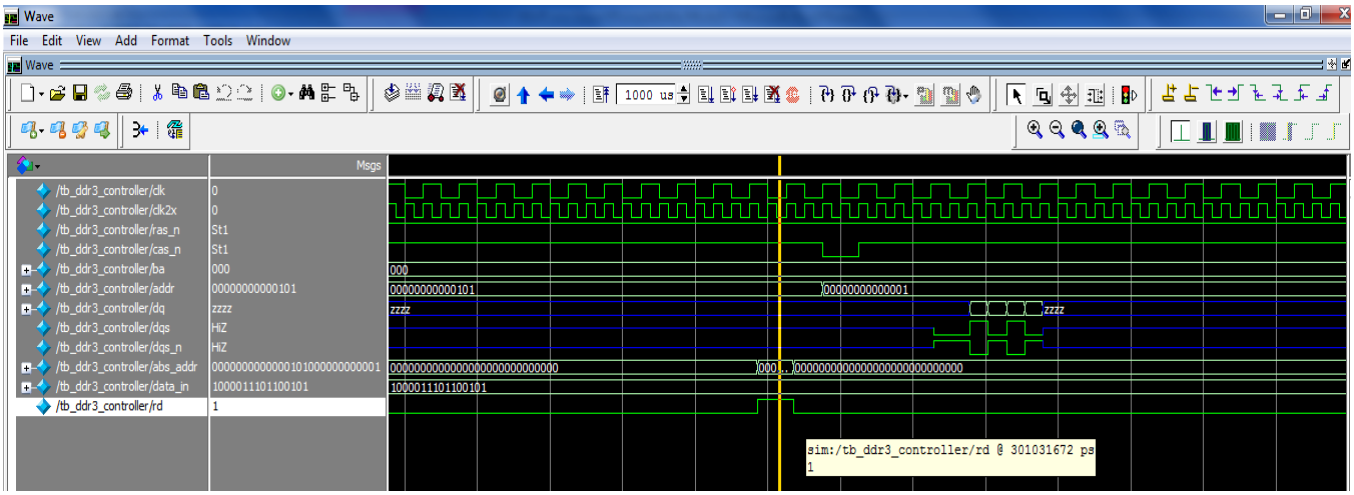



**Fig.7: simulation waveform of Refreshing logic.**




## C. Write

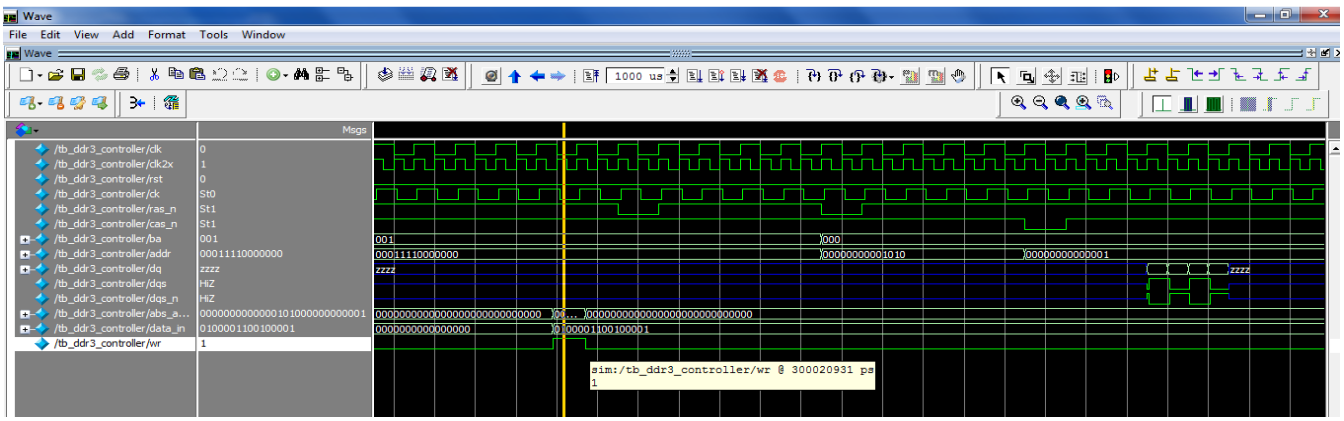



**Fig.8: simulation waveform of write process.**

### D. Read

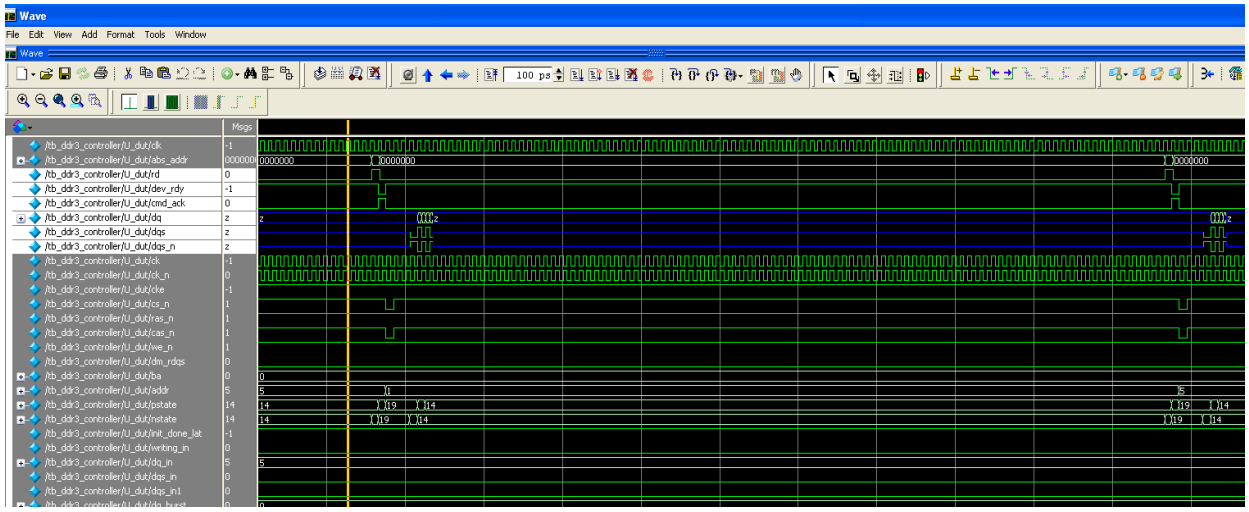


**Fig.9: simulation waveform of read.**

### E. Device Ready and command Acknowledgment

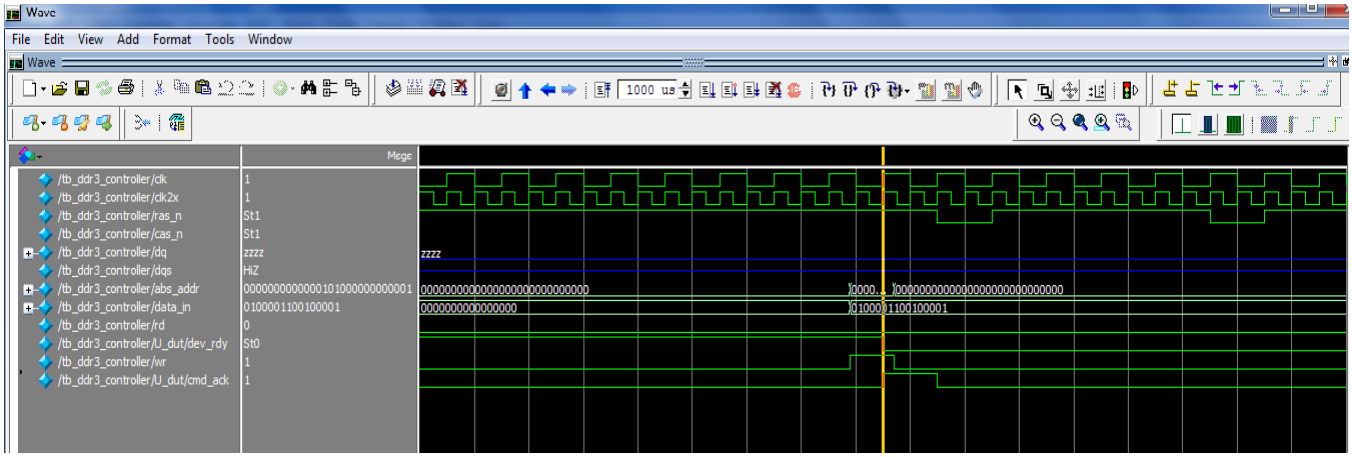


**Fig.10. simulation waveform of dev_rdy & cmd_ack**

### F.Sleep mode.

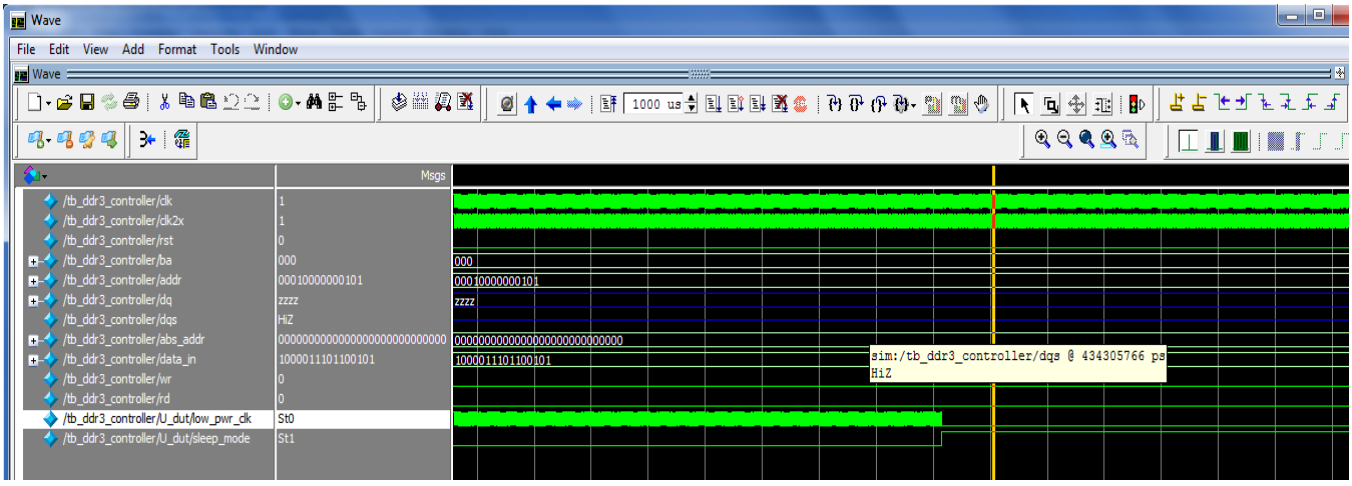


**Fig.11. simulation waveform of sleep mode**

## VI. POWER ANALYSIS

Here the power analysis is done using XPower analyzer tool. The dynamic power with clock gating and without clock gating is summarized as follows.

### A. With clock gating.


**Fig.12: Power Report with clock gating.**

**Simulation run time is 0 to 1000u seconds.**

**Table 4 : With clock gating**

| | |
|---|---|
| Vin | 1.2V |
| Frequency | 200Mhz |
| Supply power | 0.138W |
| Dynamic power | 0.077W |

### B.Without clock gating.

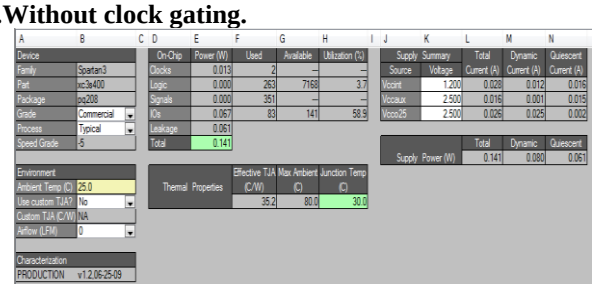



**Fig.13: Power Report without clock gating**

**(Simulation run time is 0 to 1000u seconds)**

**Table 5: without clock gating.**

| | |
|---|---|
| Vin | 1.2V |
| Frequency | 200Mhz |
| Supply power | 0.138W |
| Dynamic power | 0.080W |

From above power reports it is clear that the dynamic power is reduced from 0.080W to 0.077W if we use the clock gating. The power analysis done based on the switching activity took inside the ddr3 memory controller . We have simulated the design from 0 to 1000u seconds , under this simulation time the device has entered only once into the sleep mode.

## VII. CONCLUSION

In this paper the DDR3 controller is designed using Verilog HDL . This design is simulated in Modelsim by Mentor graphics tool and successfully synthesized in Xilinx tool , also in RTL compiler by Cadence EDA tool. The power is analyzed using Xilinx Xpower analyzer tool.

## REFERENCES


1. A High Performance DDR3 SDRAM Controller. International Journal of Electrical and Electronics Engineering (IJEEE),Volume-1,Issue-1,2011.
2. H. Song et al, "A 1.2 Gbs/pin double data rate SDRAM with on die-termination", in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, 2003, pp. 31
3. "High-Performance DDR3 SDRAM Interface in Virtex-5 Devices", *Xilinx, XAPP867 (v1.0)*, Sept 24, 2007.
4. DDR3 SDRAM Specification (JESD79-3A), *JEDEC Standard, JEDEC Solid State Technology Association*, Sept. 2007.
5. http://micron.com/parts/dram/ddr3-sdram/~/media/Documents/Products/Data%20Sheet/DRAM/4242Gb_DDR3_SDRAM.ashx
6. Implementation of AXI Design Core with DDR3 Memory Controller for SoC. IJCST Vol. 2, Iss ue 4, Oct . - Dec. 2011.
7. www.altera.com/literature/ug/ug_altmemphy.pdf, External DDR Memory PHY Interface Megafunction User Guide (ALTMEMPHY), accessed on 23 Feb. 2009
8. Implementing High-Speed DDR3 Memory Controllers in a Mid-Range FPGA A Lattice Semiconductor White Paper March 2010 http://www.latticesemi.com/documents/WP-ImplementingDDR3.pdf


## AUTHORS PROFILE

**VIJAYKUMAR** has received his Bachelor of Engineering degree in ECE from PDA college of Engineering Gulbarga affiliated to Visvesvaraya Technological University Belgaum , Karnataka in the year of 2010. Currently pursuing MTech in VLSI Design & Embedded system from Bangalore Institute of Technology, Bangalore.

**R K KARUNAVATHI** has received her Bachelor of Engineering degree in ECE from UVCE Bangalore affiliated to Bangalore University in the year of 1987 and received her Master of Engineering degree from Bangalore University , Bangalore Karnataka. She is Currently working as associate Professor in Bangalore Institute of Technology , Bangalore. She has been actively guiding UG and PG students.

**VIJAYAPRAKASH A.M** has graduated B.E from UVCE Bangalore, of Bangalore University in the year 1992, Post graduated in M.E from SDMCET Dharward of Karnataka University in the year 1997 . He has been actively guiding PG and UG students in the area of VLSI and Image Processing. He has published more than 8 National/International Papers. Currently he has been working as Associate Professor in Electronics and Communication Engineering Department, BIT, Bangalore. His research interests are Low Power VLSI, Image Processing, Synthesis and Optimization of Digital Circuits. He is a member of IMAPS and ISTE.