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Development, Integration and Verification of VHDL code for FPGA based Beam Position Measurement Board

Priti Trivedi, Sudeep Baudha

Abstract*— Continuous increase in FPGA capacity, architectural features and performance, along with decrease in cost, results in an ideal solution to hardware system designers. The embedded designer who is serious about increasing performance must consider the FPGAs ability to accelerate the processor performance with dedicated hardware. Although this technique consumes FPGA resources, the performance improvements can be extraordinary. Thus FPGA based VME Bus compatible four channels ADC card is used to acquire the Beam Position Indicator (BPI) electrode data, and calculate the beam position using an intelligence device (FPGA) on board. This card is having on-board 4-channel ADC (with signal conditioning electronics) and 8-channel Opto-coupler inputs. Additionally there is a memory available on-board to save calculated beam position. In all, the system is VME based so this card is a VME slave board where VME CPU card will be able to control the card and read the calculated beam position whenever it is available in memory.

Keywords*-- FPGA, VME, 4-channel ADC, e-beam position and BPI.

I. INTRODUCTION

The goal of this project is to develop, integrate and verify a VHDL[5] code for FPGA[2] based Beam position measurement board. ADC is interfaced with VME bus and FPGA. The necessary signals are drawn from VME bus for interfacing. Signals from VME bus are interfaced to FPGA through buffers and logic level converters. SN74LS245D transceiver is used for bidirectional bus (data bus) is used, whereas SN74LS244D buffer IC is used for interfacing them to FPGA. 24 VME address lines are directly compared with board address (from DIP switches) and the two are compared to generated CS (board select signal) which is then passed to FPGA through buffer. This board has 4 channels for analog to digital conversion. Objective of this board is to digitize the four electrode signals received from BPI front end electronics at a sampling rate of 1Msps. This board also contains a CPLD (XC95108) from Xilinx®, which was incorporated to take care of interfacing with external RAM. CPLD will perform the objective to provide a RAM (external) based FIFO [8]. An external RAM is used to store the calculated beam position, and it is indirectly interfaced to FPGA through CPLD. For programming FPGA is used as a programmable device. FPGA based designed card provide several advantages over custom designed IC based cards such as reduced cost, reduction in components, reduction in size ,easily coded . It is flexible because its parameters can be changed at any time by reprogramming the device.

II. VME BUS

The VME bus[1] specification defines an interfacing system used to interconnect microprocessors, data storage, and peripheral control devices in a closely coupled hardware configuration. The system has been conceived with the following objectives:

a. To allow communication between devices on the VME bus without disturbing the internal activities of other devices interfaced to the VME bus.

b. To specify the electrical and mechanical system characteristics required to design devices that will reliably and unambiguously communicate with other devices interfaced to the VME bus.

c. To specify protocols that precisely defines the interaction between the VME bus and devices interfaced to it.

d. To provide terminology and definitions that describes system protocol.

e. To allow a broad range of design latitude so that the designer can optimize cost and/or performance without affecting system compatibility.

f. To provide a system where performance is primarily device limited, rather than system interface limited[3].

III. HARDWARE

On board FPGA is identified as the central intelligent unit to manage most of the interfaces, process the raw data received through ADCs[6] and process them to calculate beam position. In addition to this, FPGA[4] is also responsible for communication with VME interface and give appropriate response and data for read/write commands received from VME master. FPGA will also have indirect interface (through on board CPLD) to on board static RAM, which will contain calculated beam position values.

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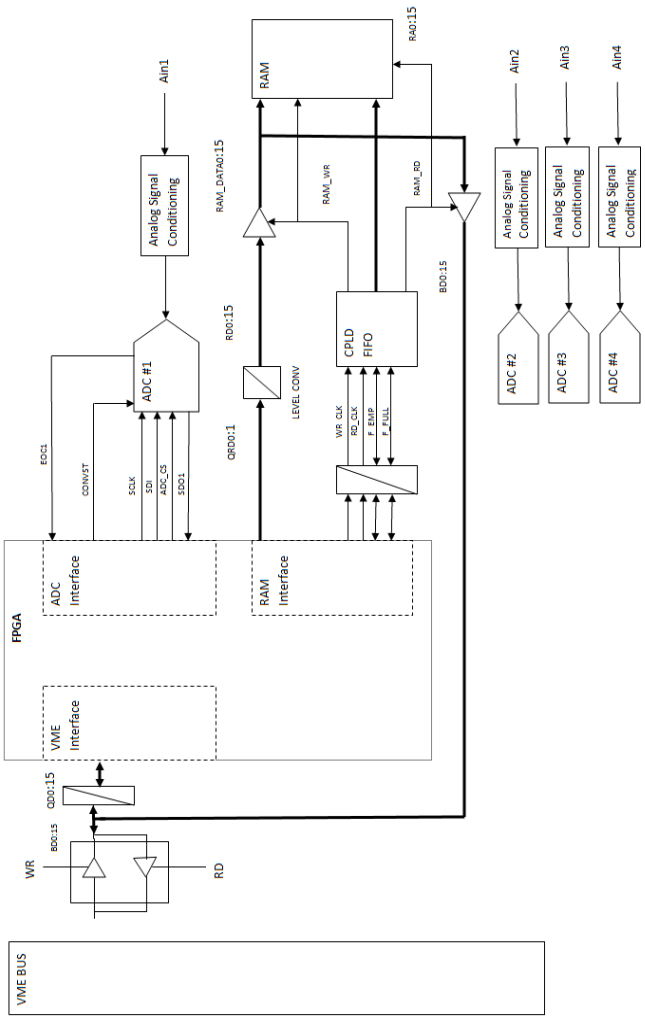

Figure 1 : Block Diagram of the VME Slave Card

IV. FEATURES OF THE CARD

1) Fully compatible with existing Accelerator Controls architecture i.e. it will be VME based.
2) BPI electrode signals (analog) are taken and simultaneously sampled through four 1MSPS, 16 bits ADC.
3) FPGA will use 16-bits fixed point arithmetic to calculate beam position.
4) On board 64K word (16 bits) memory will be available to store calculated beam position.
5) Board also has 8-channels for optocoupler isolated inputs.
6) Spartan-3 based XC3S200-4TQ144 FPGA from Xilinx® is mounted on the board to carry arithmetic for calculating beam position from electrode data.
7) VME Interrupt logic is integrated to interrupt CPU card as and when the memory with beam position data is full. Interrupt logic may be configured for any other purpose through VHDL coding.
8) All the power requirements supplies for FPGA (1.2V, 2.5V and 3.3V), supplies for ADC and opamps (+-15V, +5V) are generated on board using linear regulators and switching regulators.
9) FPGA configuration solution is provided on board so that FPGA can be reprogrammed at any time in future. For this purpose JTAG port is provided onboard and Xilinx® ISP EPROM is also available on board to keep configuration data when power is OFF.
10) Signal conditioning of electrode signal (analog) is done before feeding it to the ADC.

V. FORMULA FOR CALCULATION OF BEAM POSITION

Let the four button voltages of a BPI read by the ADC are V_A, V_B, V_C, and V_D. $V1 = K_1.V_A - V_{A0}$, $V2 = K_2.V_B - V_{B0}$, $V3 = K_3.V_C - V_{C0}$, $V4 = K_4.V_D - V_{D0}$, Where,K_1,K_2,K_3,K_4 are equalizing coefficients (default value = 1.0)V_{AO}, V_{BO}, V_{CO}, V_{DO} are the offset values. (default value = 0.0 V)

$$\delta H = \frac{V1 - V3}{V1 + V3} + \frac{V4 - V2}{V4 + V2}$$

$$\delta V = \frac{V1 - V3}{V1 + V3} + \frac{V2 - V4}{V2 + V4}$$

$X_{mech} = a1*\delta H + b1*\delta H^2 + c1*\delta H^3 + d1*\delta V^2 + e1*\delta H^4 + f1*\delta H^2*\delta V^2$

$Z_{mech} = a2*\delta V + b2*\delta V^2 + c2*\delta V^3 + d2*\delta H^2 + e2*\delta V^4 + f2*\delta H^2*\delta V^2$

$X\ (mm) = X_{mech}\cos\theta - Z_{mech}\sin\theta + Xo$

$Z\ (mm) = X_{mech}\sin\theta + Z_{mech}\cos\theta + Zo$

VI. TOOLS USED

- Xilinx ISE Design Suite 12.4
- ModelSim 6.4
- EASy68K EDITOR/ASSEMBLER V5.6.

VII. TEST PROCEDURE

1) Continuity test between different probable test points.
2) Check the supply voltage.
3) Setting of different Jumper to make connection path between analog input source and ADC input pin.
4) Download VHDL program into FPGA.
5) Open HyperTerminal software and apply necessary settings and then load EASy68K program.
6) Analog input of range from 0V to 5V is given to all four ADC's.
7) Execute assembly program from HyperTerminal using 'GD' (Go Direct).
8) Record different waveforms (SCLK, CS_ADC, CS_FPGA, SDI, SDO, CONVST, EOC) using CRO and Compare it with standard result.

Open HyperTerminal with following settings:-

Bits per second : 38400
Data bits : 8
Parity : None
Stop bits : 1
Flow Control : None

VME Crate is connected to Serial Port of the Computer. Monitor program is started through hyper terminal and then EASy68K program is loaded in the OS-9 Operating System. VME crate is connected with the CPU card which also connect 4-channel ADC card. Input to FPGA is provided from VME BUS.

The chip select of FPGA is shown by channel 1 and serial clock which is given to ADC is shown by channel 4. Whenever send configuration and read command is to ADC the chip select of FPGA becomes low for 0.5 us and 16 serial clocks (SCLK) are send to ADC.

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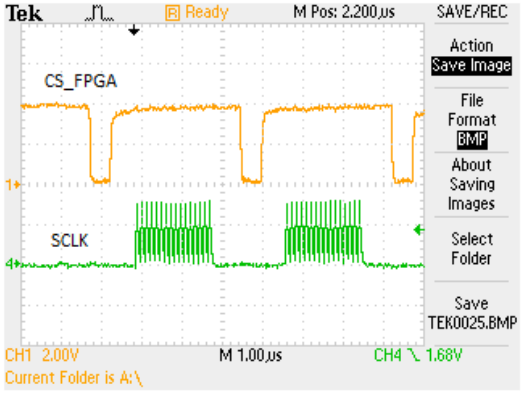

Figure 2 : Waveform of CS_FPGA and SCLK

After issuing send configuration command settings which is to be done in ADC is sent through serial data in (SDI) pin of ADC with 16 serial clocks.The serial clock (SCLK) is shown by channel 1 and serial data in (SDI) which is given to ADC is shown by channel 4 in figure 3. Conversion start command is given to ADC. After 780 ns when conversion is over end of conversion signal is given by ADC then by issuing a read command converted data can be read through serial data out(SDO) pin of ADC with 16 serial clocks.The serial clock (SCLK) is shown by channel 1 and serial data out (SDO) which is given to ADC is shown by channel 4 in figure 4.

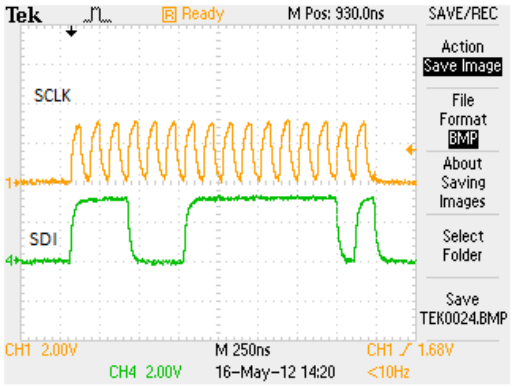

Figure 3 : Waveform of SCLK and SDI

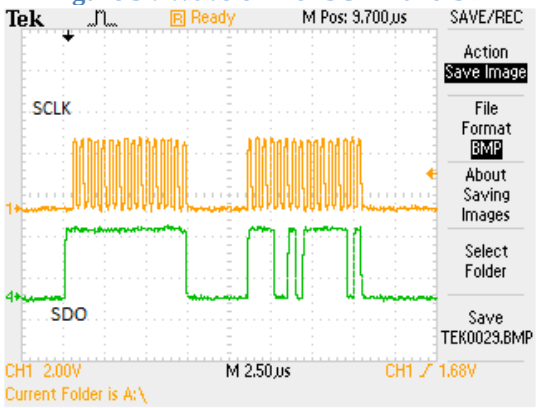

Figure 4 : Waveform of SCLK and SDO

Channel 2 shows serial data in (SDI) pin of ADC which gives send configuration command and read command. Channel 1 show 16 serial clocks given to ADC at the time of sending and reading data. Channel 4 shows serial data out (SDO) which gives converted data from ADC.

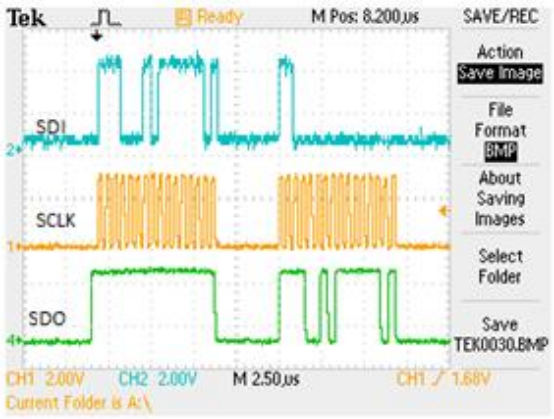

Figure 5 : Waveform of SCLK, SDI, SDO

When converted data is given to VME data bus to read through HyperTerminal a Data Acknowledge signal (DTACK) is given by VME to ensure that valid data is available in Bus.

Figure 6 : Waveform of DTACK

VIII. DEVICE UTILIZATION SUMMARY

Table 1 : Device Utilization for VME Interfaced with ADC

	Used Capacity	Whole Capacity	Percentage of Capacity
Slices	1,248	3,840	32%
Lookup Tables	1,626	3,840	42%
Flip Flop	1,053	1,248	84%
IO Signals	65	97	67%

IX. RESULT

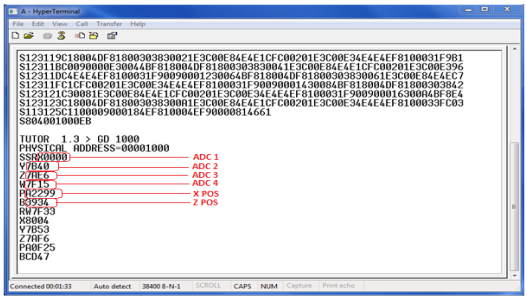

Figure 7 : HyperTerminal window showing ADC data and calculated positions in HEX Format

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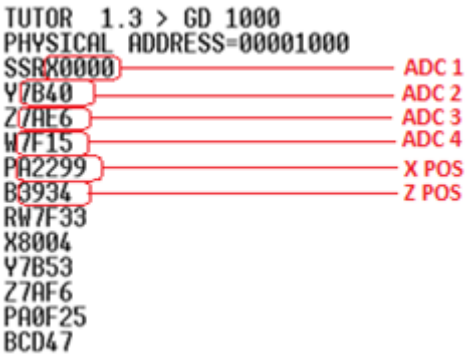

Figure 8 : Magnified View of HyperTerminal window showing ADC data and calculated positions in HEX Format

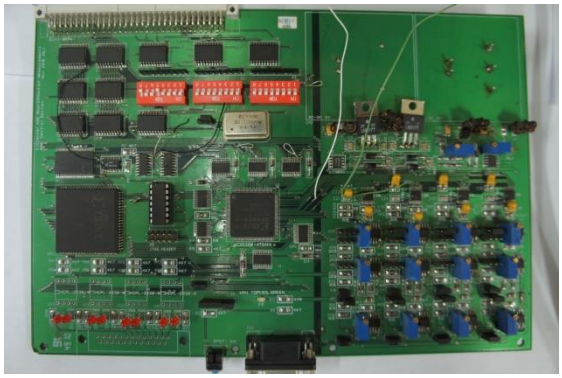

Figure 9 : Four Channel ADC Card

Figure 10 : ADC Card Attached in VME Crate

X. CONCLUSION

The 4 channel ADC Card is used for calculating beam positions according to four analog voltages applied. The four digitized voltages and the calculated positions can be stored in RAM using FIFO logic. This board can also be used as general purpose board.

XI. ACKNOWLEDGMENT

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