# 22nm PTM Model Low Power yet High Speed CMOS High K Metal Gate Strained Silicon Technology Inverter

**Shobha Sharma**

***Abstract— This paper analysis four inverter configuration with low power and high performance PTM models of Arizona State University, USA at 22nm technology with High K metal gate strained silicon technology. The effect of stacked transistor is analysed to show the reduced average and peak power dissipation. This stack effect is utilized in combination with forward biasing of a transistor to have low power but high speed inverter without loosing the maximum and minimum voltage swing at the output. Average power dissipated by low power stacked forward biased inverter is reduced by 4% compared to HP inverter. Peak power reduction is 64% in case of this new inverter compared to traditional High Performance inverter. The propagation delay is more compared to a HP inverter but is reduced by almost 18.2% compared to Low Power stacked inverter.***

***Index Terms—About four key words or phrases in alphabetical order, separated by commas.***

## I. INTRODUCTION

With decrease in gate oxide thickness to 3nm. and lesser, direct tunneling becomes the important components of gate leakage current. The tunneling is between the gate and silicon under oxide. The only way to reduce this leakage into oxide is to use high k dielectric to replace silicon dioxide of cmos bulk. Many layers of dielectric stack are recommended to have good inference with substrate. BSIM4 tunneling model is applicable to layer (many dielectric) as well. The carrier can be either electron or hole or both, or the carriers can be from the conduction band and or valence band and this is depended on the bias as well as the gate type.

BSIM4 (1)gate tunneling components are

= I gate_substrate + Igate_channel + Igate_source + Igate_drain (1)

Whereas Igate_channel = Igate_channel_source + Igate_channel_drain

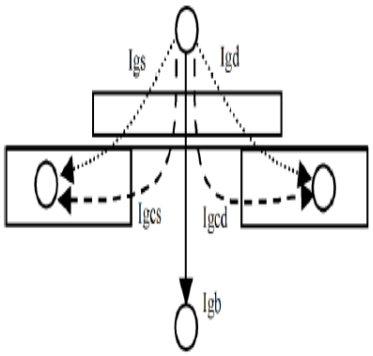


**Fig.1 Gate tunneling current componenets**

The giant Semiconductor Companies all over the globe agree together on one or many issues e.g. physical gate length. For this, formation of International Roadmap Semiconductor Organization (ITRS) (2)is done.

With scaling the power consumption increases (3), problems due to short channel effect increases and parasitic capacitance has dominant role. With scaling, the traditional physic is unable to explain the phenomena on sub 45nm system /circuit and device(4,5). There are problem due to small sizes, due to extra ordinary fields inside the small devices or circuits(4-9). The solution to these problems is to reduce supply voltage and thresh hold voltage and it is not possible, which leads to chaos / issues to be researched and resolved(7-10). At the same time reduction in thresh hold voltage would lead to excessive leakage and sub thresh hold conduction with device getting very sensitive noise and any other undesired parameters.

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## II. CIRCUIT SETUP

There are four circuits to be analysed and compared at 22nm technology node.First and second column of the table I gives the results of High performance model (Fig. 1)and Low power model inverter (Fig.1) at 22nm technology node of High K metal gate silicon Technology. The third column is the CMOS LP inverter with PMOS stacking and normal body biasing (Fig. 3) whereas the fourth column is the CMOS LP inverter with pmos stacking and forward body biasing (Fig. 4) of PMOS near to OUT terminal.

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**Shobha sharma**, ECE Dept, Indira Gandhi Institute of Technology, GGSIP university, Delhi, India.

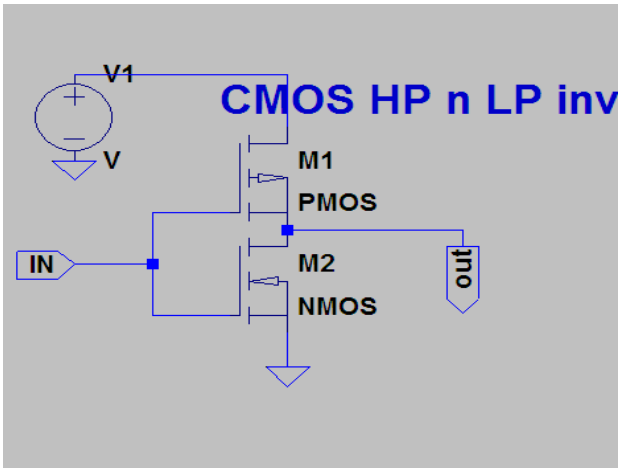


**Fig. 1 High performance and Low power CMOS inverter**

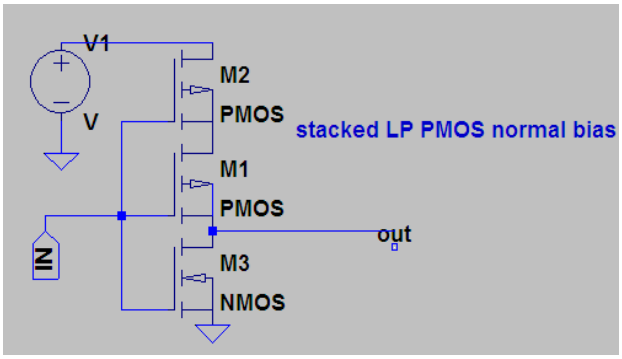


**Fig. 2 Stacked PMOS LP inverter with normal body Bias**

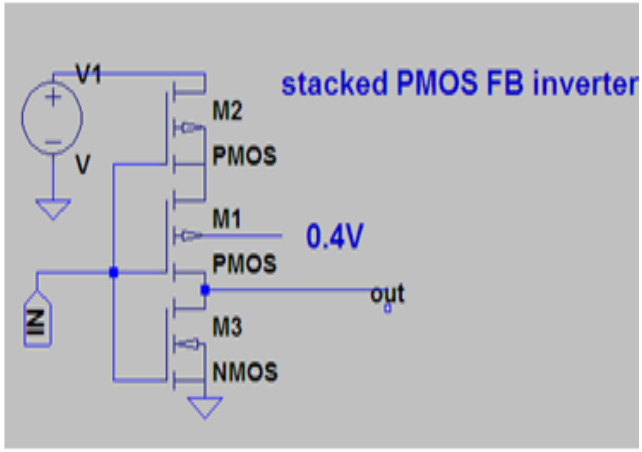


**Fig. 3 Stacked PMOS LP inverter with one PMOS Forward Bias**

## III. ANALYSIS

The results of High Performance model at 22nm High K metal gate technology inverter shows the average and peak power to be 4.93 µ and 53 µ whereas that of Low power shows the reduction in these values(Column II of Table I) by 2% and 33% respectively as expected without loosing the maximum output voltage swing to be that of supply voltage and ground voltage at 25 degree C. Also rise time , fall time and propogation delay at the OUTPUT of an inverter is more in LP model inverter compared to HP model inverter.

**Stacking effect on Low Power inverter**

With stacking the power consumption/dissipation reduces down due to increase in the resistance of the inverter . The rise time of an stacked pmos is doubled due to two pmos in series and fall time remained same. The propagation delay for input low to output high increased to two times as PMOS is responsible for high output.

**Effect of Forward Biasing of a Stacked inverter**

The forward biased inverter (Fig. 3) results in high speed yet low power due to use of low power models in the inverter without loosing the maximum output voltage swing. Increasing the forward bias more than +0.4V results in output 'high level 'voltage degradation and is the reason to not to go beyond this voltage.

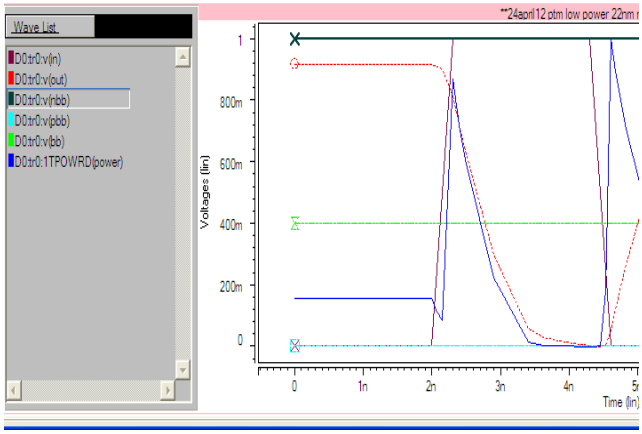


**Fig. 4 Input output and substrate biases of the new low power and high speed inverter along with power waveform**

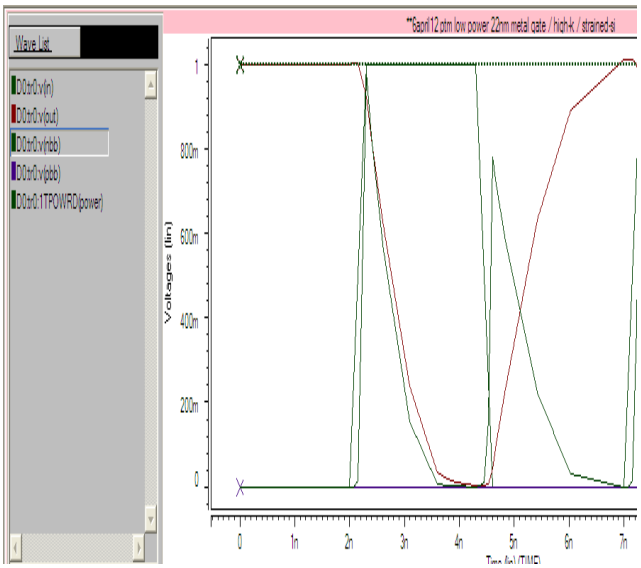


**Fig. 5 Input output and substrate biases of the LP stacked with normal biased inverter along with power waveform**

Comparison table I below shows the comparison of all the four inverters.

**Table I.Comparison table to compare various parameters of new LP forward biased stacked inverter to HP and LP normal as well as stacked inverter**

| | High performance Inverter Fig.1 | Low power inverter Fig.1 | Stacked PMOS Low power Fig.2 | Stacked PMOS low power inverter with forward biasing Fig. 3 |
|---|---|---|---|---|
| **Average Power W** | **4.9277E-06** | **4.8178E-06** | **4.2462E-06** | **4.6703E-06** |
| **Peak power W** | **5.3214E-05** | **3.5470E-05** | **2.0471E-05** | **1.9393E-05** |
| **Rms value** | **7.3108E-01** | **7.2873E-01** | **6.8052E-01** | **6.3708E-01** |
| **O/P RISE TIME** | **2.8133E-10s** | **7.2698E-10s** | **1.4192E-09s** | **1.3088E-09s** |
| **O/P FALL TIME** | **3.7282E-10s** | **1.0946E-09s** | **1.0896E-09s** | **1.2116E-09s** |
| **Propogation Delay** Low to High | **9.6260E-11 s** | **3.5440E-10 s** | **7.8458E-10 s** | **6.7803E-10 s** |
| **Propogation Delay** High to Low | **4.1996E-10 s** | **1.3137E-09 s** | **1.3203E-09 s** | **1.2461E-09 s** |
| **Nodal Cap:input** | 173.9228af | **204.6066af** | **383.6994af** | **382.0584af** |
| **Nodal Cap:output** | 20.1993ff | **20.2108ff** | **20.2108ff** | **20.2052ff** |
| **Nodal Cap:Vdd** | 160.5529af | **171.2185a** | **171.2187af** | **184.3647af** |

## IV. CONCLUSION

The comparison shows the decreased average , peak and rms value of the power of the new inverter compared to normal HP and LP inverter due to stacking effect. Average power dissipated is more for the new inverter due to forward biasing of one of the PMOS as compared to stacked and normal reversed biased inverter. The forward bias of stacked LP inverter shows the reduced propagation delay compared to normal stacked LP inverter.

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