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Design of Low Power Zigzag 8T SRAM array with Differential Write Back Scheme

J. Suganthi, N. Kumaresan, K. Anbarasi

Abstract—*Static random access memory (SRAM) has been widely used as the representative memory for logic LSIs. This is because SRAM array operates fast as logic circuits operate, and consumes a little power at standby mode. array. Therefore, the good design of SRAM cell and SRAM cell array is inevitable to obtain high performance, low power, low cost, and reliable logic LSI. Various kinds of SRAM memory cell has been historically proposed, developed and used. Nanometer SRAM cannot achieve lower VDDmin due to read-disturb, half-select disturb and write failure. This paper demonstrates quantitative performance advantages of a zigzag 8T-SRAM (Z8T) cell over the decoupled single-ended sensing 8T-SRAM (DS8T) with write-back schemes, which was previously recognized as the most area-efficient cell under large supply voltage variations. In this paper, we propose a new compact z-shape cell layout to prioritize symmetric device placement while providing high area efficiency.*

Keywords*-Low supply voltage, SRAM, read disturb, static voltage, SRAM, read disturb, static noise margin, write margin.

I. INTRODUCTION

LOW-POWER and high-stability has been the main themes of SRAM designs in the last decade. The explosion of the portable electronic market constantly urges for less power-hungry architectures. Thus, many techniques have been employed to deliver this requirement such as scaling the supply voltage, using multi-threshold CMOS process to minimize the leakage, dividing the SRAM macro into multiple
Sub-macros to enhance its stabilities and to reduce dynamic power. Among these, supply voltage down scaling offers the highest effectiveness since the dynamic power is a quadratic function of voltage. Furthermore, it also exponentially reduces
the leakage current which dominates the active current in the Sub-100 nm CMOS processes.

To achieve lower VDD operation for 6T SRAM, SRAM designers have tried enlarging the size of the transistors to improve read stability (SNM) and write margins. Upsizing-6T (U6T) reduces and improves read and write margins, but designers have still been unable to meet lower VDDmin requirements in the sub threshold or near sub threshold regions.

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Several VDDmin design solutions for 6T SRAM have been proposed in recent years. Various bias controls for the terminals of 6T SRAM, such as cell VDD (CVDD), cell VSS (CVSS), wordline (WL), bitline (BL), or bulk bias has been used to solve the low VDD issues. The bias circuit is either row based or column based to control these terminals. These schemes usually induce unwanted instability issues or performance degradation in unselected cells in corresponding rows or columns. In addition, boosting circuits or voltage suppression circuits require extra area and power for voltage regulation. Hence, previous design solutions for 6T SRAM are still limiting the improvement of VDDmin. For this reason, several 7T to 10T SRAM circuits with decoupled read ports have been proposed. The decoupled read ports eliminate bitline charge sharing with the SRAM internal storage nodes. It prevents read disturb issues while the word-line is turned on.

The decoupled read scheme can be categorized into single-ended and differential-ended decoupled read ports. The single-ended read port suffers from poor bitline noise immunity and reduced bitline swing sensing margins due to bitline leakage and noise. Single-ended sensing requires a pMOS keeper to compensate for bitline leakage from unselected rows. Bitline pMOS keepers induce data contention issues between cell current and pMOS keepers. In addition, the read speed for the single-ended sensing is very slow due to its full rail logic gate sensing.

The decoupled differential read port 9T (D9T) and 10T (D10T, CP10T) cell improve read speed but require large area. These SRAM cells consume approximately 1.7x 2.1x the area of conventional 6T cells, because they require extra devices and comprise dead space within their layout. The larger area limits improvements in speed and margins. Poorer area-cost effective cells lead to an increase in σVth due to limitations in resorting to transistor upsizing. For the write access, one can use either write-back
(WB) or cross-point (CP) access to solve half-select disturb issues. In previous write-back designs, the decoupled single-ended with WB SRAM suffers from slower read speeds and WB due to their single-ended read sensing. CP10T and CP8T cells, require an row signal and a column signal to turn on the serial access-gates. Cross-point (CP) cells suffer from degraded Write ability due to their serial access-gates. Hence, the CP cells require an additional write assist circuit to compensate for weak writ ability. The 6T with self-WB reduces the probability of disturb failure but fails to completely solve half-select disturb issues. A failure may still occur before the self-WB sense amplifier is activated.

Previous low VDDmin SRAMs suffered from many obvious drawbacks such as large area, slow read sensing, weak write margins, imperfect layout patterns, and half-selected solutions for low VDD applications. It would be safe to say that the ultimate cell would require a "decoupled faster differential read first and write back" without an increase in cell area, compared with DS8T, which was previously recognized as the most area efficient cell at large σVth/VDD.

The objective of my paper is to to design an efficient cache system using 8 MOS transistors in the basic cell and to achieve low power consumption. This increases the stability though noise margin and the Read/Write accessing speed.

The remainder of this paper is organized as follows. Section II describes the operation of the proposed Z8T SRAM cell and layout. Section III presents its macro structure and implementation. Section IV analyzes the performance and compares it to the performance of other SRAMs. Section V presents the results of the experiments. Section VI summarizes our conclusions

II. 8T SRAM CELL

a) Differential Sensing 8T (DS8T) SRAM CELL

The proposed SRAM cell consists of 8 transistors, N1–N5 and P1–P3, with all having minimum size of 120 nm/60 nm to save area. Four transistors N1, N2, P1 and P2 form a cross-couple structure to store data. Four transistors P3 and N3–N5 are used to access to the internal nodes D and /D of the cell. N3 and N4 connect the cell internal node to the CS while P3 and N5 form an inverter to control the voltage of node.

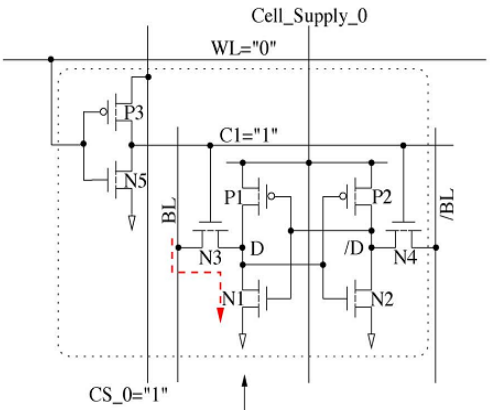
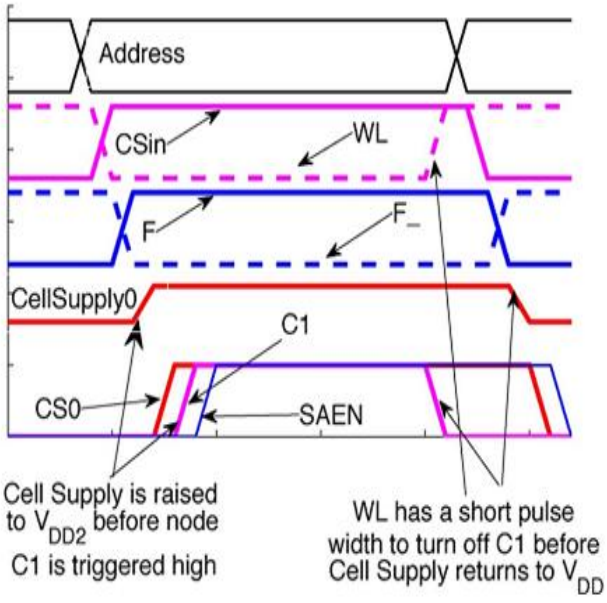


Fig.1 8T Differential SRAM cell

The source terminal of P3 is connected to a column select line while the gates of P3 and N3 are connected to the word line. As a result, N4 and N3 are turned on if and only if both the transistors are triggered. Unlike the conventional design, the sources of P1 and P2 are connected to a dynamic cell supply line which is raised to the higher voltage during the read operation to obtain a higher noise margin.



. Fig.2 Timing diagram for DS8T design

b) The ZIGZAG 8T (Z8T) SRAM

Z8T cell comprises a standard 6T cell and 2T decoupled differential read-port (D RP), decoded by a virtual logic-swing read-wordline (RWL). Two decoupled read-port transistors (2T), NR0 and NR1, are used to transfer the storage data (Q and QB) to the read bitline (RBL, RBLB). Because the storage nodes and RBL/RBLB are isolated by NR0 and NR1, the storage nodes (Q and QB) are entirely decoupled from RBL and RBLB, and read static noise margins are similar to hold static noise margin. The decoupled differential read port solves the read disturb issue, as well as enabling differential read operation employing small swing high speed sensing.

In this Z8T design, the RWL of the selected row is pulled to VSS and RWLs remain VDD for the unselected rows during read operation. The full swing control allows the RWL to be shared across columns without any data collisions between columns. Thus, the VDD-driven unselected RWL eliminates the need for extra switches as in previous decoupled RP and enables DD RP with only 2T. Differential sensing reduces the read BL (RBL) swing, which also helps to avoid data collisions between columns. The Z8T cell has better read static noise margins to the equivalent of hold SNM of conventional 6T SRAM. The Z8T-SRAM also has a faster read speed for long bitline applications due to its small swing differential read sensing.

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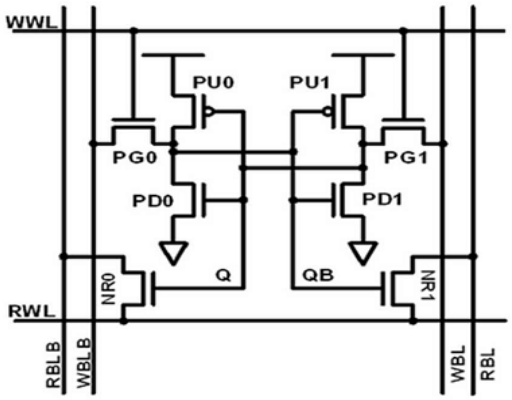

Fig.4 Zigzag 8T SRAM cell

c) Zigzag layout of Z8T cell

The cross-coupled inverter latches with two write pass transistors PG0 and PG1 (6T), which have the same layout placement as in a conventional 6T SRAM cell. The poly gate of NR0 and NR1 are directly extended from the nMOS gates of the two inverters.

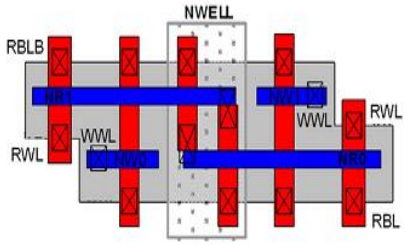

Fig.4 Layout of Z8T cell

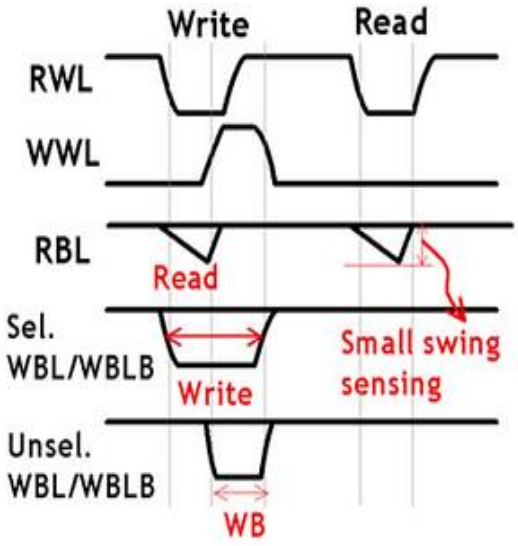

Fig. 5 Read and Write cycles

Therefore, extra poly to contact spacing for connecting in the X-direction of the DS8T layout is not required. In write operation, theWWL is activated and turned to a high oltage (VDD), which turns on the pass gate transistors PG0 and PG1. The driving write data at the complementary write bitline pair (WBL and WBLB) will be passed to the storage nodes of the cross-coupled latch, to overcome the original states stored thereon.

d) Differential Read and Write-Back Sense Amplifier (DRWB)

Differential read and write-back sense amplifiers (DRWB-SA) are placed at the bottom of each column. They are connected directly to the RBL/RBLB and WBL/WBLB to perform read sensing only for read and write operations for the selected columns; and a differential read with subsequent write-back for the unselected columns.

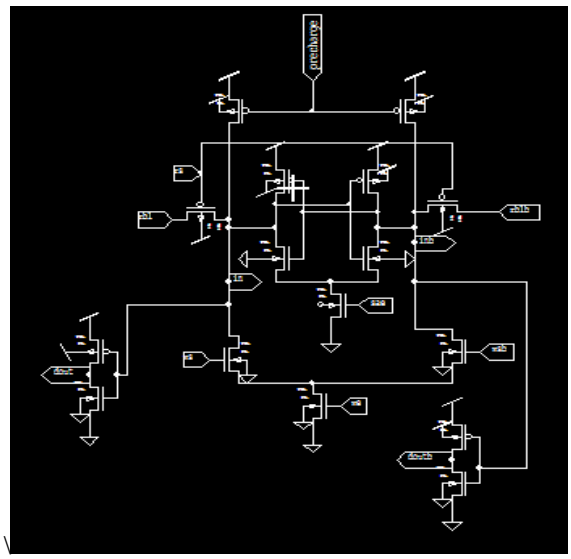

Fig.6 Schematic of the proposed DRWB-SA

To perform the read first and write-back procedure during the write cycle, the read word-line is also activated, even during the write cycle. The column decoder MUX output buffer is in the last stage of the data sense amplifier. Compared with the previous single-ended sensing DS8T with a WB scheme, Z8T can provide much faster secure read-first and WB operation. The DRWB-SA comprises one pair of read control lines (RS and complementary write control lines (WS/WSB) for control of the read and write, respectively. Fig. 3(a) shows a block diagram and data path of the DRWB-SA for read and write operations. The truth table of the switch control signals (RS and WS/WSB) is listed in Table I.

Table.1 Truth table of DRWB SA switches

	Selected-column		Unselected-column	
Switches	Read	Write	Read	Write
RS	On	Off	Off	On
WS	Off	On/Off	Off	Off
WSB	Off	Off/On	Off	Off

Prior to the operation, the PR0 and PR1 PMOSs precharge both WBL/WBLB and IN/INB to VDD. During the sensing period, the latch-type SA is activated by the sense-amplifier-enable (SAE) signal.

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By enabling the RS signal, the two pMOS pass-gates, PG0 and PG1, connect the RBL/RBLB with the IN/INB of the SA. NW0 and NW1 form a write buffer and transfer the write data to the internal nodes (IN and INB). The write buffers are activated by the write enabled (WE) signal.

During the read operation, the RS signal is set to low, to turn on the pMOS transistors PG0 and PG1, so that the signal on the RBL and RBLB will pass into the sense amplifiers IN and INB. After the RBL and RBLB have developed an adequate difference in voltage, the SAE will be activated and will amplify the complementary IN and INB nodes to their full logic swing level. The resulting full logic swing signal is then sent to the MUX and output buffer to perform a read operation.

III. MACRO IMPLEMENTATION

a) Macro structure

RWLs are activated both for read and write operations. The WWL is activated after the RWL cycle during a write operation and is not activated during the read operation.

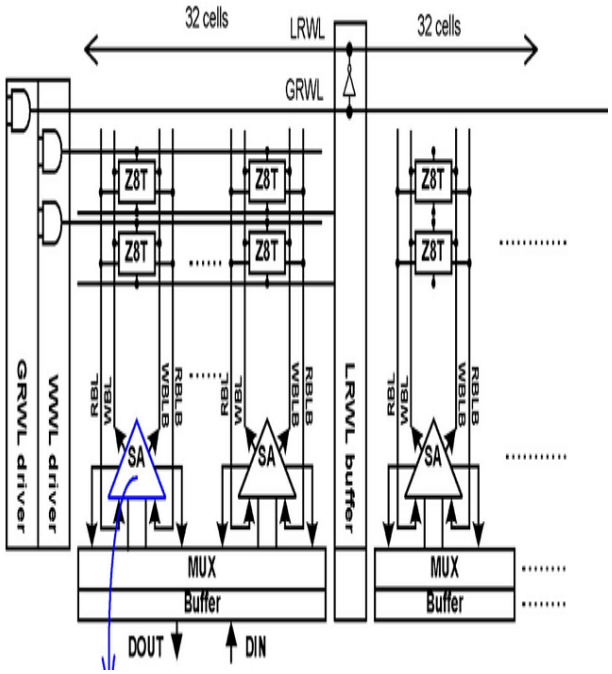

Fig .7 SRAM array structure

The cell current simultaneously sinking across columns causes an IR drop and ground bounce on the selected RWL,degrading RBL access speed. To reduce the RWL driver size and prevent speed degradation due to RWL ground bounce,this work employs a segmented structure for the read word-line (RWL). Two metal layers are used for RWL signals, metal-5 layer for the global RWL (GRWL), and a metal-3 layer for the local RWL (LRWL). The GRWL is connected to the LRWL buffers. There are only 64 cells on a LRWL in this work. The GRWL requires a small-size driver, thanks to its light loading. The LRWL buffer is placed at the center of a cell array.

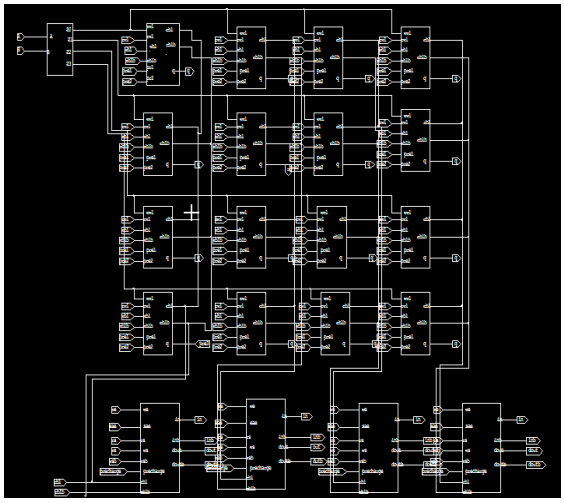

Fig.8 **SRAM** Macro architecture

IV. PERFORMANCE AND COMPARISON

a) Power consumption

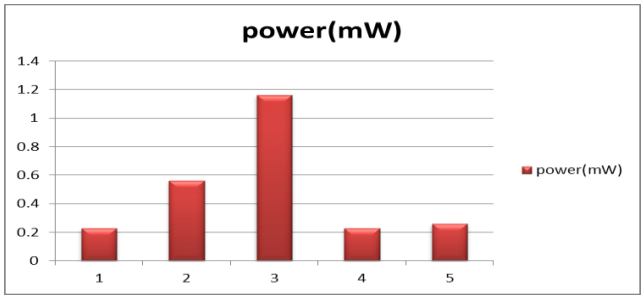

Fig.9 **P**ower consumption comparison chart

The fig.9 shows that significant power reduction that can be achieved when using Z8T SRAM cell in an array. Almost 75.93 percentage of power reduction is achieved while using Z8T cell

b) Accessing speed

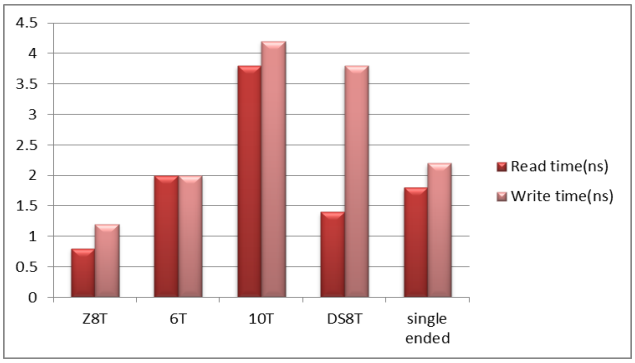

Fig .10 Read and Write speed comparison

This fig.10 shows that the accessing time of Z8T cell is small when compared to the other SRAM cells. The Read and Write speed of Z8T cell is high because of its Differential Decoupled Read Port (D^2RP)

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C) Cell area

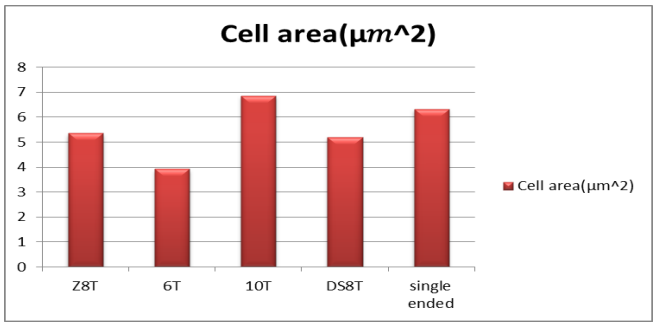

Fig .11 Cell area comparisons

This fig.11 shows that the area of Z8T cell is similar to that of DS8T cell. Since Z8T uses only 1T for each decoupled read-port, faster 2T differential sensing can be implemented within the same area as the single ended DS8T..

Table 3 Performance comparison of SRAM cells

parameter	Z8T	6T	10T	DS8T	SINGLE ENDED
AREA (μm²)	5.4	3.9	6.86	5	6.32
READ TIME(ns)	0.8	2	3.8	1	1.8
WRITE TIME(ns)	1.2	2	4.2	4	2.2
POWER(mw)	0.2	0.6	1.16	0	0.26
HALF SELECT	WB	NO	WB	WB	NO

IV. Conclusion

In this paper the Z8T SRAM is proposed, which comprises an area efficient 2T differential decoupled read port with a pseudo RWL for cell stability during read operations. The proposed Z8T cell is realized using a zigzag shape layout to achieve compact area and fully symmetric device placement for lithe friendly layout.Z8T SRAM cell has been designed and the macro architecture has been implemented. Analysed the cell performance in terms of power consumption, accessing speed, cell area and noise margin. Z8T cell leads to reduction of power consumption. Because of differential decoupled read port the cell accessing speed is increased. For the macro implementation, this work uses zigzag placed DRWB-SA to achieve fast read and write-back speed. The work can be extended to further reduction of power consumption and to reduce the read and write disturbances. For this various power reduction approaches have to be implemented. Different SRAM cell structures have to be proposed to enhance the reliability

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