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Design and Implementation of Low-Power High-Performance Carry Skip Adder

Santanu Maity, Bishnu Prasad De, Aditya Kr. Singh

ABSTRACT- The most timing critical part of logic design usually contains one or more arithmetic operations, in which addition is commonly involved. In VLSI applications, area, delay and power are the important factors which must be taken into account in the design of a fast adder. The carry-skip adder reduces the time needed to propagate the carry by skipping over groups of consecutive adder stages, is known to be comparable in speed to the carry look-ahead technique while it uses less logic area and less power. In this paper, a design of 8-bit Carry Skip Adder by various existing logic styles are to be compared quantitatively and qualitatively by performing detailed transistor-level simulation using T-Spice v13.0.

Key words: Low power, High performance, Carry Skip adder, Logic design style, CMOS, CPL, DPL, Reversible Logic.

I. INTRODUCTION

With the increasing level of device integration and the growth in complexity of microelectronic circuits, power dissipation, delay and area has come the primary design goal. The failure mode of high-power circuits relates to the increasing popularity of portable electronic devices. Laptop computers, pagers, portable video players and cellular phones all use batteries as a power source, which by their nature provide a limited time of operation before they require recharging. To extend battery life, low power operation is desirable in integrated circuits. Furthermore, successive generations of applications often require *more* computing power, placing greater demands on energy storage elements within the system. Power dissipation limitations come in two flavors. The first is related to cooling considerations when implementing high performance systems. High speed circuits dissipate large amounts of energy in a short amount of time, generating a great deal of heat as a by-product. This heat needs to be removed by the package on which integrated circuits are mounted. Heat removal may become a limiting factor if the package (PC board, system enclosure, heat sink) cannot adequately dissipate this heat, or if the required thermal components are too expensive for the application [1].

Addition is the most basic arithmetic operation and adder is the most fundamental component of any digital processor.

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Depending on the area, delay and power requirements, several adder configurations such as ripple carry carry look ahead, carry-skip and carry select are available in the literature. The ripple carry adder (RCA) is the simplest adder, but has the longest delay because every sum output needs to wait for the carry-in from the previous adder cell. It uses O(n) area and has a delay of O(n), for an n-bit adder. The carry look-ahead adder has delay $O(\log n)$ and uses $O(n\log n)$ area. On the other hand, the carry skip and carry select adders have $O(\sqrt{n})$ delay and uses $O(n)$ area . Carry skip adders also dissipate less power than other adders due to their low transistor counts and short wire lengths [2].

II. LITERATURE SURVEY

Much of the research efforts of the past years in the area of digital electronics have been directed towards increasing the speed of digital system. Recently the requirement of portability and the moderate improvement in battery performance indicates that the power dissipation is one of the most critical design parameter.

The three most widely accepted metrics to measure the quality of a circuit or to compare various circuit styles are area, delay and power dissipation. Portability imposes a strict limitation on power dissipation while still demands high computational speeds. Hence, in recent VLSI Systems the power-delay product becomes the most essential metric of performance. The reduction of the power dissipation and the improvement of the speed require optimizations at all levels of the design procedure. Since, most digital circuitry is composed of simple and/or complex gates; we study the best way to implement adders in order to achieve low power dissipation and high speed.

A detailed review of the existing CMOS circuit design styles and Reversible logic style is given, describing their advantages and limitation. Also, various design and implementation of Carry Skip Adder were analyzed in the terms of delay and power consumption using T-Spice.

Conventional Static CMOS has been a technique of choice in most Processor design. Alternatively, Static Pass Transistor circuit has also been suggested for Low Power applications [2]. Dynamic circuit, when clocked carefully, can also be used in Low Power, High speed Systems [3]. Reversible logic has received great attention in the recent years due to its ability to reduce the power dissipation. Quantum arithmetic components need reversible logic circuits for their construction. Reversible logic circuits find wide application in low power digital design, DNA computing, quantum

computing and nanotechnology. In 1960 R.Landauer demonstrated that high technology circuits and systems constructed using irreversible hardware results in energy dissipation due to information loss. According to Landauer's principle, the loss of one bit of information dissipates kTln2 joules of energy where k is the Boltzmann's constant and T is the absolute temperature at which the operation is performed [4]. Later Bennett, in 1973, showed that in order to avoid kTln2 joules of energy dissipation in a circuit it must be built from reversible circuits [5].

III. ARCHITECTURE OF CARRY SKIP ADDER

The carry skip adder provides a compromise between a ripple carry adder and a CLA adder. The carry skip adder divides the words to be added into blocks. Within each block, ripple carry is used to produce the sum bit and the carry.

The Carry Skip Adder reduces the delay due to the carry computation i.e. by skipping over groups of consecutive adder stages [6].

• If each Ai # Bi in a group, then we do not need to compute the new value of Ci+1 for that block; the carry-in of the block can be propagated directly to the next block.

• If Ai = Bi = 1 for some i in the group, a carry is generated which may be propagated up to the output of that group.

• If Ai = Bi = 0, a carry, will not be propagated by that bit location.

The basic idea of a carry-skip adder is to detect if in each group all Ai # Bi and enable the block's carry-in to skip the block when this happens as shown in figure1. In general a block-skip delay can be different from the delay due to the propagation of a carry to the next bit position [7][8].

With carry skip adders, the linear growth of carry chain delay with the size of the input operands is improved by allowing carries to skip across blocks of bits, rather than rippling through them.

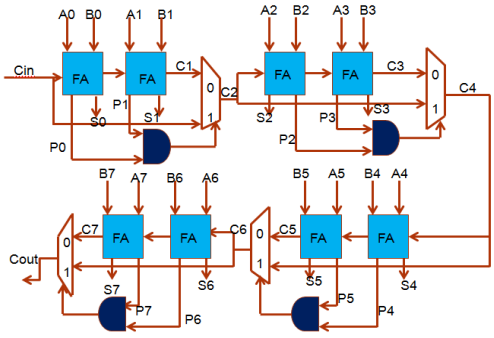

Fig..1 Architectural block of 8-bit Carry Skip Adder (CSKA)

IV. LOGIC DESIGN STYLES

The increasing demand for low-power VLSI can be addressed at different steps of VLSI design cycle, such as the architectural, circuit, layout, and the process technology level. At the circuit design step, considerable potential for power savings exists by means of proper choice of a logic style for implementing circuits. This is because all the important parameter governing power dissipation-switching capacitance, transition activity, and short-circuit currents—are strongly influenced by the chosen logic style. Depending on the application, circuit can be implemented in different logic style.

A. Standard CMOS Logic:

Standard CMOS is the most common and widely utilized digital logic in almost any application field. Still, other digital logic styles exist and are utilized in the industry as well. Since we aim in this thesis work for special design characteristics, such as very low power consumption and very small sized designs, it is fair to have a look at other digital logic design styles as well. The schematic diagram of a conventional static CMOS full adder cell is illustrated in figure 2.The signals noted with '-'are the complementary signals. The p-MOSFET network of each stage is the dual network of the n-MOSFET.

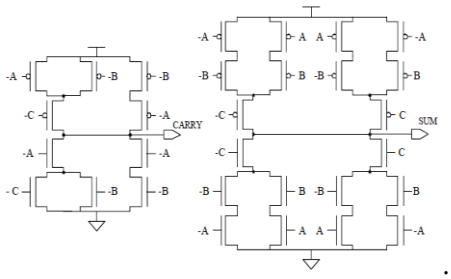

Fig.2 CMOS Logic Full Adder

The implementation of CSKA using CMOS logic is shown in Fig.3 and its corresponding simulated waveform in fig.4.

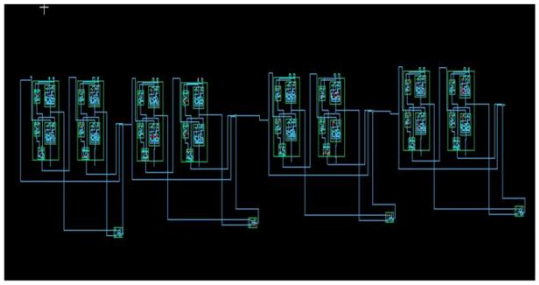

Fig.3: Schematic diagram of CSKA byCMOS logic.

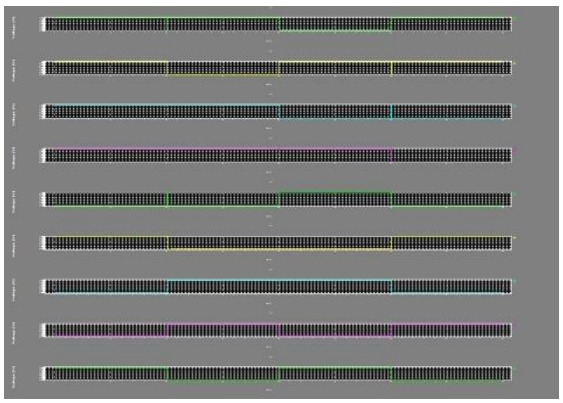

Fig.4: Simulation waveform of CSKA by CMOS Logic.

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B. Complementary Pass Transistor (CPL)

CPL [6] uses only an n-MOSFET network for the implementation of logic functions, thus resulting in low input capacitance and high-speed operation [8]. The schematic diagram of the CPL full adder circuit is shown in figure 5. Because the high voltage level of the pass-transistor outputs is lower than the supply voltage level by the threshold voltage of the pass transistors, the signals have to be amplified by using CMOS inverters at the outputs.

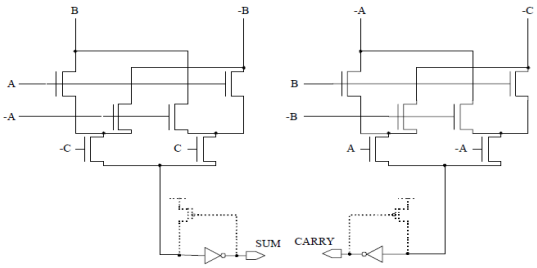

Fig.:5 Full Adder using CPL logic

The implementation of CSKA using CPL logic is shown in Fig. 6 and its corresponding simulated waveform in fig.7.

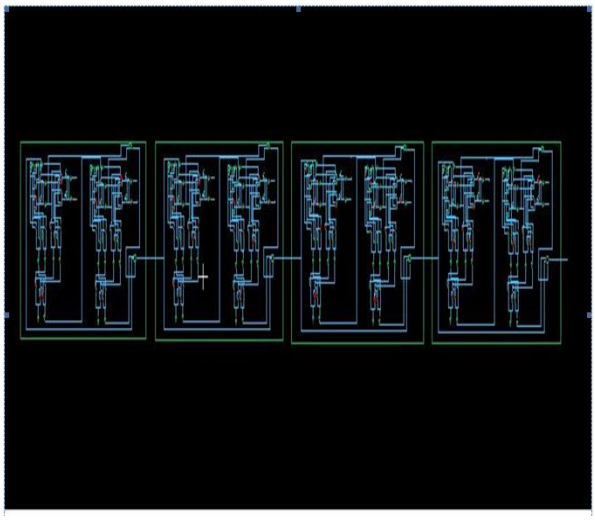

Fig.6 Schematic diagram 8-bit CSKA using CPL logic.

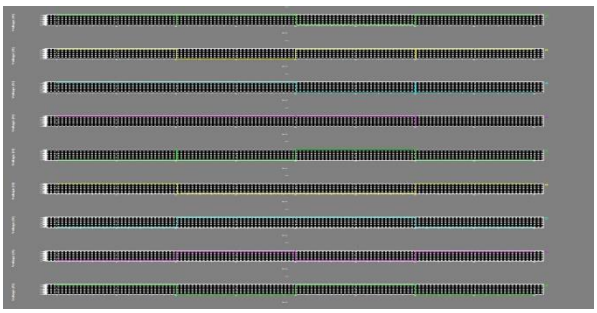

Fig.7 Simulated Waveform of CSKA using CPL logic

C. Double -Pass Transistor Logic (DPL)

DPL [6][7] is a modified version of CPL. The circuit diagram of the DPL full adder is given in figure 8. In DPL circuit full-swing operation is achieved by simply adding p-MOSFET transistors in parallel with the n-MOSFET transistors. Hence, the problems of noise margin and speed degradation at reduced supply voltages, which are caused in CPL circuits due to the reduced high voltage level, are avoided [9].

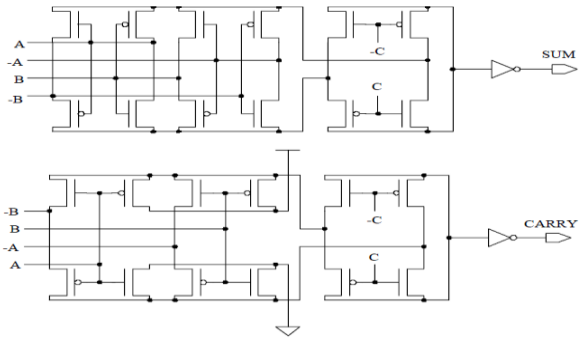

Fig.8 Full Adder using DPL logic

The implementation of CSKA using DPL logic is shown in Fig 9 and its corresponding simulated waveform in fig.10.

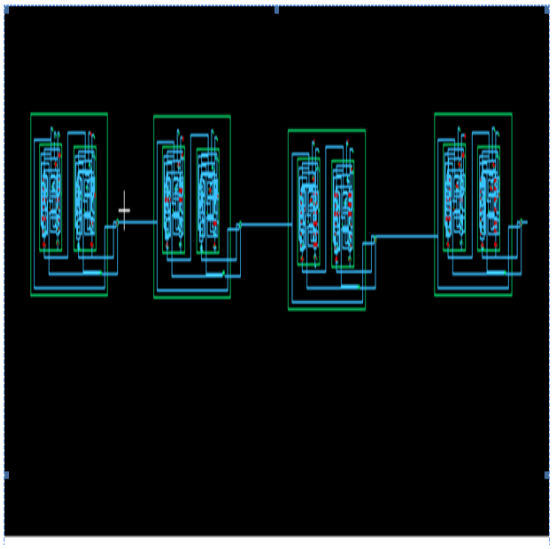

Fig.9 Schematic diagram of 8-bit CSKA using DPL logic

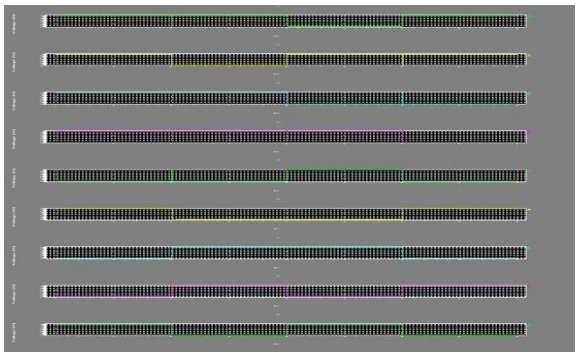

Fig.10 Simulated Waveform of 8-bit

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D. REVERSIBLE LOGIC

Reversible logic has received great attention in the recent years due to its ability to reduce the power dissipation. Quantum arithmetic components need reversible logic circuits for their construction. Reversible logic circuits find wide application in low power digital design, DNA computing, quantum computing and nanotechnology. In 1960 R.Landauer demonstrated that high technology circuits and systems constructed using irreversible hardware results in energy dissipation due to information loss. According to Landauer's principle, the loss of one bit of information dissipates kTln2 joules of energy where k is the Boltzmann's constant and T is the absolute temperature at which the operation is performed [4]. Later Bennett, in 1973, showed that in order to avoid kTln2 joules of energy dissipation in a circuit it must be built from reversible circuits [5]

A reversible logic gate is an n-input, n-output logic device with one-to-one mapping. Reversible circuits are constructed using reversible logic gates. These reversible circuits not only produce unique output vector from each input vector but also the input can be reconstructed from the outputs. A reversible circuit should be designed using a minimum number of reversible gates. Fan-out and loops are not allowed in reversible logic circuits [10]. However fan-out and feedback can be achieved by using additional gates.

The complexity and performance of the circuit is decided on the following parameter [11][12][13].

(i) Garbage outputs: The number of unused outputs present in the reversible logic circuit.

(ii) Number of reversible gates: Total number of reversible gates used in the circuit.

(iii) Delay: Maximum number of unit delay gates in the path of propagation of inputs to outputs. It represents the total number of reversible gates used between the primary inputs and the outputs of a reversible logic circuit.

(iv) Constant inputs: The number of inputs which are maintained constant at 0 or 1 in order to get the required function. They are necessary to synthesize a reversible function.

Fredkin gate: A Fredkin gate [14] in Figure.11 is a conservative-logic gate which maps 3 inputs (X2, X0, and X1) onto 3 outputs (Y2, Y0, Y1). The truth table of a Fredkin gate is given in Tab.1. Roughly speaking, the input *X2* is directly mapped to output*Y2*.

When *Y2* =1, inputs *X0* and *X1* are mapped to outputs Y0 andY1, respectively. When X2 =0, on the other hand, the outputs Y0 and Y1 are swapped such that X0 (X1) is mapped to Y1 (resp. Y0). The output is defined by Y2=X2, Y0=X2X0+X2X1 and Y1=X2X1+X2X0. Quantum cost of a Fredkin gate is 5[15].The two input AND gate(AND2) was generated by the FG by grounding one terminal as shown in fig.12.

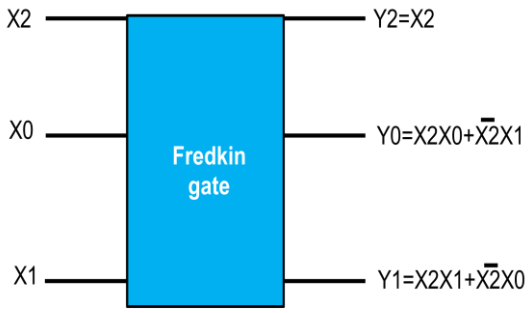

Fig. 11 Block diagram of Fredkin Gate

Table 1: Truth Table of Fredkin gate

Truth Table

X2	X0	X1	Y2	Y0	Y1
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

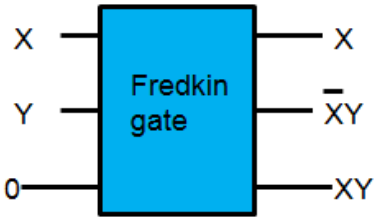

Fig.12 Fredkin gate implementation of AND2 gate.

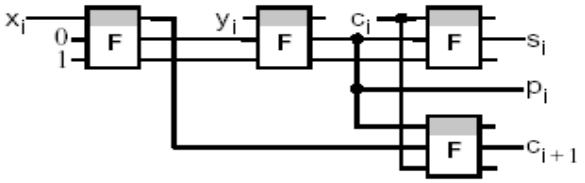

Fig.13 Fredkin gate Full Adder.

The implementation of CSKA using reversible logic (fredkin gate) is shown in Fig 14 and its corresponding simulated waveform in fig.15.

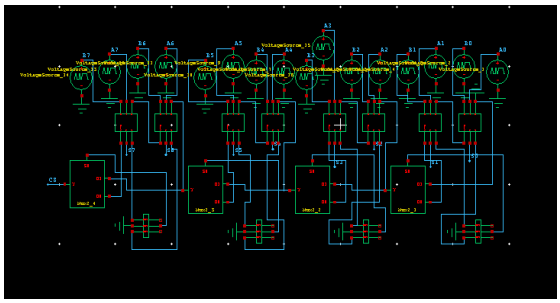

Fig.14 Schematic diagram of 8-bit

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CSKA using Fredkin gate Full Adder.

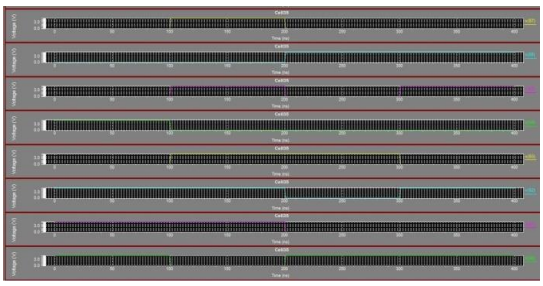

Fig.15 Simulated Waveform of 8-bit CSKA using Fredkin gate Full Adder.

The Fredkin gate full adder is been improved by avoiding fan-out as shown in fig.16.

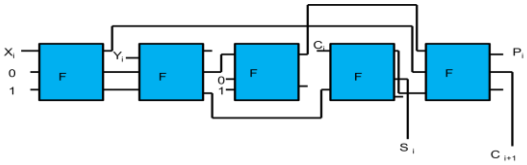

Fig.16 Block diagram of Fredkin gate Full adder avoiding fan-out

The implementation of CSKA using improved Fredkin gate full adder logic is shown in Fig.17 and its corresponding simulated waveform in fig.18.

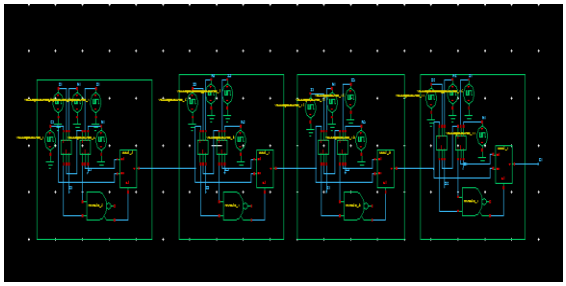

Fig.17. Schematic diagram using 8-bit CSKA using Fredkin gate Full Adder avoiding fan-out.

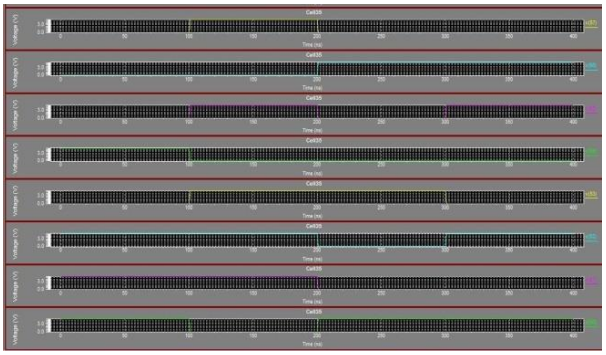

Fig.18. Simulated Waveform of CSKA using Fredkin gate Full Adder avoiding fan-out.

V. PERFORMANCE PARAMETERS AND SIMULATION SET UP

The 8-bit Carry Skip Adder is compared based on the performance parameters like propagation delay, number of transistors and power dissipation. To achieve better performance, the circuits were designed using CMOS process and Reversible logic process. The channel width of the transistors is 450nm for the NMOS and 900nm for the PMOS and channel length is 150nm with operating frequency is 10 GHz. All the circuits have been designed using TANNER EDA [16] with model file as dual.md. The power estimation is a difficult task because of its dependency on various parameters and has received a lot of attention [17]. Direct Simulation method [18] is used in order to analyse the results. Table:2 and Table:3 .Shows Comparative Experimental results of Carry Skip Adder using different Logic Styles in terms of area, power and delay.

Table: 2. Comparison of performance parameters for different logic style.

Logic style	No. of transis-tors	Power dissipation (mW)	Propaga-tion delay (ns)	Power delay product (pJ)
CMOS	260	0.22	200.44	44.474
CPL	128	4.48	99.77	479.89
DPL	208	5.67	31.4	178.038

Table: 3. Comparison of designs using reversible logic.

Reversible logic style	No. of Transistor	Garbage Output	Power Dissipation(mW)	Propagation Delay (ns)	Power Delay Product (PDP)
Fredkin gate	272	48	0.34 mW	16.6ns	5.644 pJ
Improved Fredkin gate avoiding fan-out	320	32	0.18 mW	17.2ns	3.096 pJ

Comparison of 8 bit CSKA using different logic Style in terms No. of Transistor, Power and delay Constraints and PDP are shown in Fig.19.

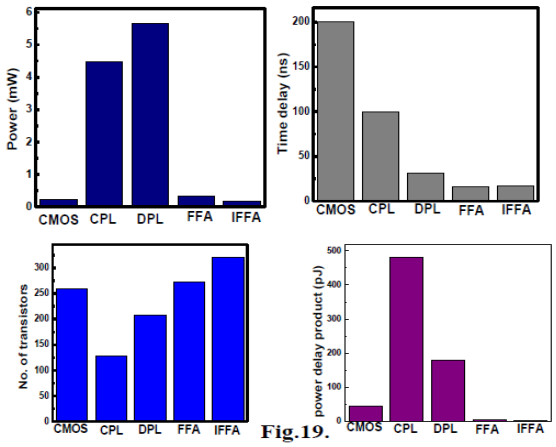

Fig.19. Comparison between different logic style in terms of power, delay, No. of transistor and PDP.

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VI. RESULT ANALYSIS

It has been observed that Reversible logic using Fredkin gate Full Adder (FFA) exhibit better characteristics (speed and Low-Power) as compared to other design styles. So, Reversible logic style can be used where portability and high speed is the prime aim. Where, Reversible logic using Improved Fredkin gate Full Adder (IFFA) consumes the lowest power among the five. With the reduction of Garbage Output, the Improved Fredkin gate Full Adder (IFFA) Reversible logic can be considered best logic design style with respect to all parameters of 8-bit Carry Skip Adder architectures as shown in Table 2.and Table.3.

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VII. VII. IMPLEMENTATION IN XILINX 7.0

A. CSKA Simulation Result

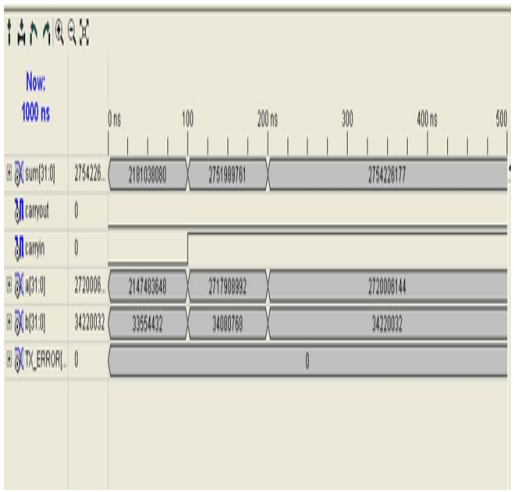

Fig.20. Test bench waveform of 32 bit CSKA

B. Device Utilization Summary:

Table: 4. Summary of device utilization.

logic utilization	used	available	utilization
No. of Slices	62	768	8%
No. of 4 input LUTs	108	1536	7%
No. of bonded IOBs	98	97	100%

Delay: 53.537ns.

VIII. HARDWARE IMPLEMENTATION IN CPLD KIT

A. Assigning Pin Location Constraints

1. Verify that source file is selected in the Sources window.
2. Double-click the Floor plan Area/IO/Logic - Post Synthesis process found in the User Constraints process group. The Xilinx Pin out and Area Constraints Editor (PACE) opens.
3. Select the Package View tab.
4. In the Design Object List window, enter a pin location for each pin in the Location column.

B. Package pin location of XC9536.PC44.10 CPLD Kit

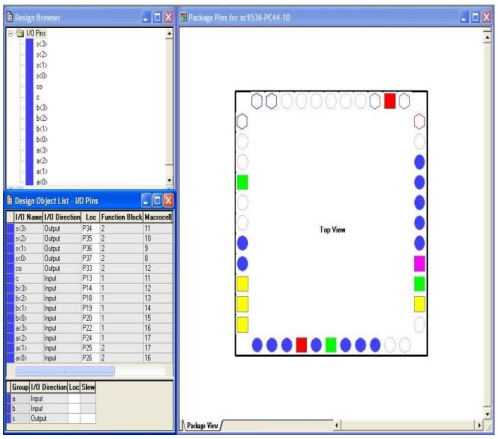

Fig.21 Input –Output Pin allocation

B. Dumping Programming Procedure in the CPLD

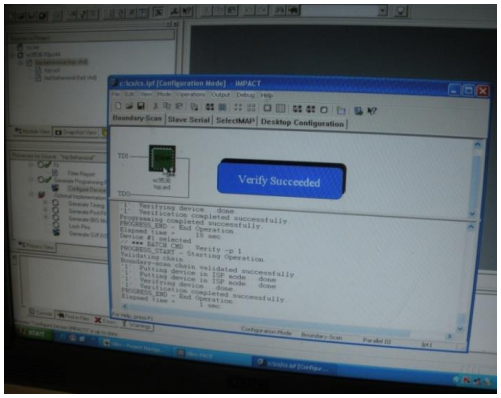

Fig. 22 Program verification

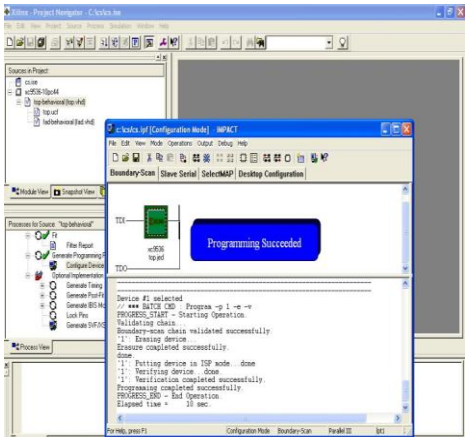

Fig.23 iIMPACT Programming Succeeded, CPLD's DONE Pin is HIGH.

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D. OUTPUT DISPLAY

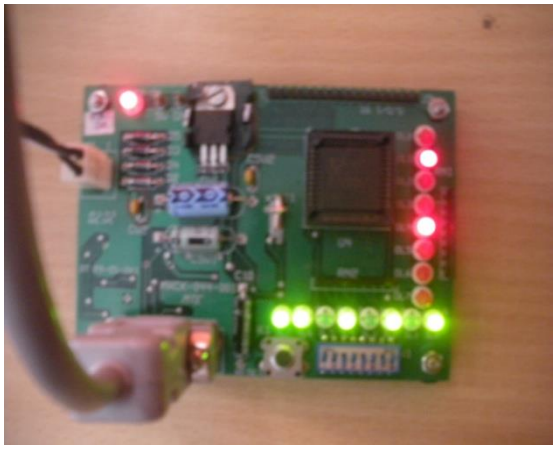

Fig.24 Output Display of CPLD with Inputs (A=0101, B=1101) and Output (Y) =0010 with Carryout =1.

IX. CONCLUSION

In this paper we have designed and simulated 8bit CSK adder using different logic style. The novelty of our approach is been justified by the calculated comparison made with that of the results obtained by SPICE simulations.

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